Introduction
Heterogeneous parallel systems have been recently exploited for a wide range of application domains, for both the dedicated (e.g. embedded) and the general purpose products. Such systems can include different processor cores, memories, dedicated ICs and a set of connections between them. They are so complex that the design methodology plays a major role in determining the success of the products.

Goals
The main goals of this demo are to describe the proposed System-Level Methodology for HW/SW Co-Design of Heterogeneous Parallel Dedicated Systems and to show its application to some basic examples.

Demo description
This demo addresses the problem of the electronic system-level HW/SW co-design of heterogeneous parallel dedicated systems. In particular, it shows an enhanced CSP/SystemC-based design space exploration step (and related ESL-EDA prototype tools), in the context of an existing HW/SW co-design flow that, given the behavioral system specification and related NF requirements, is able to automatically suggest to the designer:
- a custom heterogeneous parallel architecture
- an HW/SW partitioning of the system specification
- a mapping of the partitioned entities onto the proposed architecture

HEPSYCODE HW/SW Co-Design Flow

The focus is on the tools that compose the DSE step:
- HW/SW Partitioning, Mapping and Architecture Definition
- HW/SW Timing Co-Simulation
Some basic examples show the possible support to designers during the system development.