I. XbarGen: a tool for design space exploration of memristor based crossbar architectures

Due to the lack of an automated process of translation from a given boolean function to a memristor based crossbar architecture, deeply investigating about memristor based crossbar circuits turns out to be really hard to accomplish. Therefore, in order to overcome these problems, we developed XbarGen.

XbarGen is a command line tool written in C++ which, starting from a boolean function described in the Synopsys equation format - EQN - (fig 1), executes the mapping to a memristor based crossbar architecture i.e., the Fast Boolean Logic Circuit of each level are translated into a given memristor based crossbars depending on how many subsets it finds. Mapping to a crossbar means that inputs, outputs and related minterms are produced, they must be connected together in series, as proposed by Snider in [2] and depicted in figure 3.

![Snider Boolean Logic Circuit](image)

Consequently, the latency of the circuit grows proportionally to the number of serially connected crossbars.

Moreover XbarGen is useful in order to perform a formal design space exploration that aims to calculate interesting circuits attributes avoiding simulation campaigns. It implements an algorithmic method to estimate both workload independent attributes (e.g. performance, area, etc.) and workload dependent ones. In particular, it estimates the power consumption of the given architecture (FBLC [1]) providing both a lower and an upper bound for the power consumption and an error estimation.

Finally, taking a boolean function as input, the tool is able to produce a VHDL implementation of the resulting circuit. The entire Synthesis flow is reported in figure 4.

![Synthesis flow](image)

REFERENCES
