

Reconfigurable Self-timed Dataflow Accelerator & Fast Network Analysis in Silicon

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RECONFIGURABLE SELF-TIMED DATAFLOW ACCELERATOR

Many real-life applications require dynamically reconfigurable pipelines to handle incoming data items differently depending on their values or the current operating mode. Reconfigurable synchronous pipelines are known since 1980s and are well supported by formal models and EDA tools. Reconfigurable asynchronous pipelines on the other hand, have neither a formal behavioural model, nor mature automation support, making them unattractive to industry.

We will demo an asynchronous accelerator for ordinal pattern encoding [1] with reconfigurable pipeline depth. The hardware system has been designed, verified and synthesised using the *dataflow structure* model [2] in WORKCRAFT [3]. This approach has been then validated with the fabrication of an ASIC (TSMC 90nm technology) via Europractice.

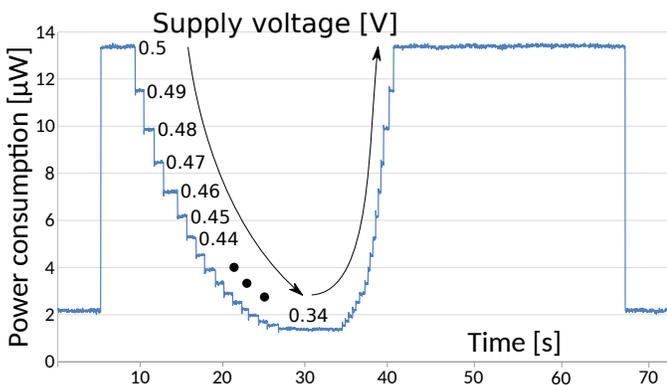


Fig. 1. Voltage variation resilience.

The chip has been equipped with a testing infrastructure to collect statistics for future research. The most interesting results are:

- High resilience of self-timed circuit to voltage variation (0.3 - 1.6V), see Figure 1 for sub-threshold measurements. This enables another degree of optimisation for energy/time interplay.
- Accuracy of the results regulated by the depth of the pipeline.
- The cost of reconfigurability, in terms of area, computation time and energy consumption is negligible compared to the non-reconfigurable reference design.
- The *dataflow structure* plugin of WORKCRAFT supports the design, simulation, verification of asynchronous reconfigurable pipelines.

FAST NETWORK ANALYSIS IN SILICON

The importance of having a fast and flexible approach to the analysis of networks is given by the high number of applications that rely on underlying graph-based models. In our case study, biological systems are modelled by graphs, and drugs can disconnect some of the connections within them. Parameters such as the average shortest path gives the resilience to a particular drug, and help analyse the effectiveness of a medicine. In software, graph analysis is computationally expensive: the internal paths should be explored one at a time. The maximum performance can be obtained by mapping the whole network into a piece of silicon and exploiting the hardware parallelism completely. In our demo, a network (defined as an XML file) can be automatically converted into a HDL design where the nodes are modelled with registers, and connections with wires. The network is then placed into a pre-designed system for the analysis, Figure 2. The whole design is synthesised into Altera FPGA-based board. FPGAs fit this application well, providing the right tradeoff between speed and flexibility. The developed accelerator is to be integrated into the drug discovery flow of our industrial partner.

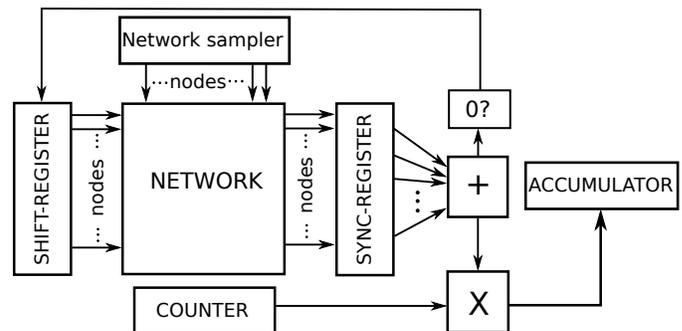


Fig. 2. Hardware system for fast network analysis.

The demo will include:

- The flow from the network conversion to the analysis.
- The comparison between the C++ software implementation of the analysis algorithm and the hardware counterpart (thousands times faster).
- Statistics gathered from different networks.

REFERENCES

- [1] C. Guo et al. "Pipelined reconfigurable accelerator for ordinal pattern encoding". ASAP, 2014.
- [2] D. Sokolov et al. "Analysis of static data flow structures". Fundamenta Inf., 2008.
- [3] WORKCRAFT homepage. <http://www.workcraft.org/>.