A Voltage-Scalable Fully Digital On-Chip Memory for Ultra-Low-Power IoT Processors

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I. Introduction

With the rapid development of Internet of Things (IoT), embedded processors with low power consumption is highly required. On-chip memories are the primary bottlenecks in these processors, thus achieving low power consumption of these memories is a must.

This work presents a voltage-scalable RISC processor fabricated in a 65-nm FD-SOI process technology. Unlike conventional processors, the processor has Standard-Cell based Memories (SCMs) as an alternative to conventional SRAM macros. Since only standard-cells are used for SCMs, custom design effort for SCMs can be reduced to the level of fully automated cell based design with keeping their stability even at a 0.3 V single supply voltage. The SCMs also achieve the power consumption of less than 20 μW at a 0.4 V supply voltage when 1.0 V reverse body bias is applied, enabling them to operate with ambient energy sources only. The results imply that we can reduce the design cost of low-supply-voltage embedded processors since assist circuits or peripheral circuits for on-chip memories are no longer required.

II. Demonstration Circuit

Figure 1 shows a photograph of the proposed processor fabricated in a 65-nm FD-SOI process technology. The processor has i) 4-kB I-Cache, ii) 8-kB I-SPM, and iii) 16-kB D-SPM as on-chip memories. Standard-Cell based Memories (SCMs) are implemented for all the on-chip memories. The SCM has a fully digital structure depicted in Fig. 2.

Figure 3 shows a demonstration circuit of the low-power SCM. A block RAM in the FPGA is interconnected with the processor to act as a main memory where a DCT loop program is stored. All the circuits but the SCM operates with the external power source. A lemon battery is connected to the SCM as a power source. The demonstration circuit shows that the processor can operate with a clock frequency on the order of kilohertz. The results imply that the SCM is suitable for low-power IoT processors since it can operate with ambient energy sources only without any assist circuits or peripheral circuits.

Acknowledgment

This work has been partly supported by KAKENHI Grant-in-Aid for Scientific Research 16H01713, 26280013 and 16J08694 from JSPS. This work is also supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc. and Synopsys, Inc..

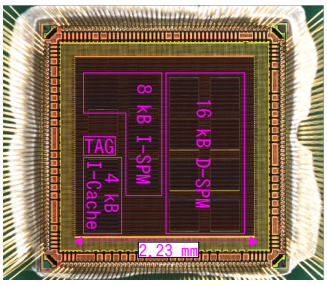

Fig. 1. Chip photograph of the fabricated RISC processor in a 65-nm FD-SOI process technology.

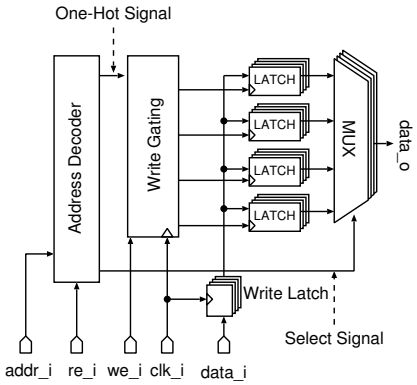

Fig. 2. Standard-Cell based Memory (SCM) structure.

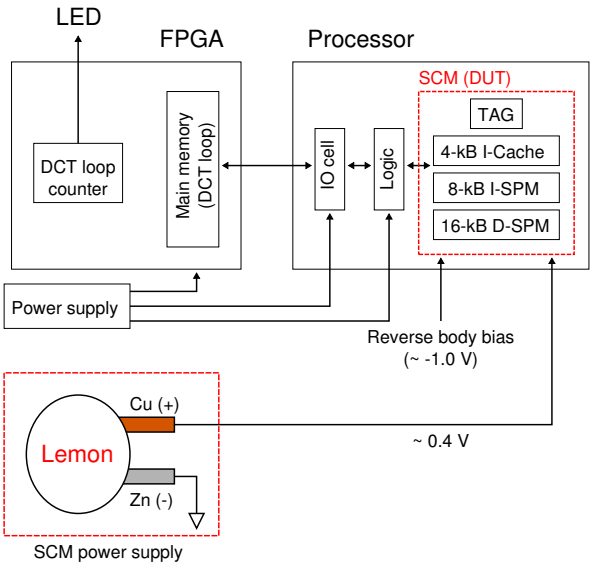

Fig. 3. Demonstration circuit.