NETFI-2: An Automatic Method for Fault Injection on HDL-Based Designs

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Abstract—Fault injection is a well-known technique to evaluate the susceptibility of integrated circuits to the effects of radiation. In this demo, we present a methodology to emulate Single Event Upsets (SEUs) and Single Event Transients (SETs) in a Field Programmable Gate Array (FPGA).

I. INTRODUCTION

In recent years, FPGA-based fault injection became an interesting and popular method to emulate the radiation effects in HDL-based designs. The advantages of this approach are controllability, observability and speed-up of simulation. NETList Fault Injector (NETFI) was proposed in [1] and extended in [2] as a method to inject faults at the Register-Transfer Level (RTL) by modifying Xilinx library components. In this demo, the original methodology of NETFI is extended and improved in several aspects in its version called NETFI-2.

II. NETFI-2 DESCRIPTION AND DEMO

Figure 1 illustrates the workflow proposed in the extended version NETFI-2. Initially, the Hardware Description Language (HDL) of the DUT is used to obtain the first synthesis in step 1. This first step does not require any modification to the original design. In step 2, the first obtained netlist is then used as input for the MODNET tool described in [1]. The second netlist is then synthesized in an Electronic Design Interchange Format (EDIF) using a modified version of the sensitive components, which include signals to access them to fault injection. In step 3, the EDIF file obtained in step 2 is then attached to the MicroBlaze and the last synthesis is performed to generate the bitstream based on the target FPGA. Finally, in the step 4 the experiment is executed in a hardware-based FPGA platform. In this demo, we use a Nexys 4 board equipped with a Xilinx Artix-7 XC7A100T-CS324.

Figure 2 illustrates the general architecture of NETFI-2 comprising both the fault inject campaign controller and the DUT instantiated in the same FPGA. In this demo, The DUTs are a LEON3 processor and a Bayesian Machine [3]. The DUT is contained within an Advanced Extensible Interface (AXI) Lite protocol slave managed by the Xilinx MicroBlaze processor. The AXI interface allows communicating the DUT with the processor with minimal FPGA area usage. NETFI-2 uses this communication channel to configure both the fault injection in the components already intervened by MODNET as well as the input and output values of the DUT. The MicroBlaze control makes use of standard interfaces like UART or Ethernet to report the progress of the experiment as well as its final results.

REFERENCES