Demonstration of fast HW/SW co-processing for rover navigation on Mars

George Lentaris, Konstantinos Maragos, Dimitrios Soudris
National Technical University of Athens, School of ECE, Microprocessors Laboratory and Digital Systems Lab
Contact: {glentaris, komaragos, dsoudris}@microlab.ntua.gr

1. Introduction

Rover missions in space seek to optimize the autonomy, power, accuracy and speed of the navigation. The optimization of these factors will allow the rover to explore more areas in the planets, extract more scientific results and protect itself from potential threats such as obstacles during the path. However, one of the main bottlenecks of the system's performance is the extremely slow on-board space-grade CPU. To surpass this limitation and assist the operation of the space-grade CPU, researchers and engineers have turned to novel solutions such as the space-grade FPGAs. The FPGAs have found their way in industry due to the remarkable performance per watt ratio; they enable the acceleration of very computational intensive algorithms, such as the sophisticated computer vision tasks being employed for navigation, while at the same time provide increased power efficiency.

In this demonstration, we present a SW/HW co-processing solution to accelerate basic functions of computer vision algorithms such as Mapping and localization. Mapping refers to the process of reconstructing a 3D map while localization to visual odometry. Both functions are used to solve the SLAM (Simultaneous Localization and Mapping) problem, i.e., the construction of a map of an unknown environment while simultaneously keeping track of the rover’s location within this environment. The demonstration showcases a proof-of-concept system tailored to the needs of future Mars exploration missions being scheduled by the European Space Agency.

2. Demonstrator

The demonstration presents the HW/SW co-processing on FPGA (Xilinx Kintex-7 XC7K325T-2FFG900C) and CPU (Intel Atom N455). The FPGA-CPU communication is performed via Ethernet port. The visual odometry algorithms process successively the stereo images acquired by a hypothetical rover moving on the Martian surface to estimate the pose of the rover (position and orientation) at each time instant. The images (512x384px) are input to the CPU, sent to the FPGA for feature detection, feature description, and feature matching, while the CPU performs filtering and egomotion estimation with absolute orientation. The rover’s path in this test is 100m long and the positional error of the HW/SW system remains around 1%. The following image depicts a screenshot of the system while running a synthetic dataset. The upper-right window shows the current image (supposedly captured by the camera), the upper-left window shows the packets exchanged between the CPU and FPGA, the bottom window shows the results reported at each frame (detected corners, matched features, rover’s pose), while the plot compares the ground truth path to the estimated path of the rover (updated every second).

![Figure 1: Screenshot of the demonstrator at run-time showing input and results.](image URL)