Generating Asynchronous Circuits from Catapult

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Demonstration Description

In order to spread asynchronous circuit design to a large community of designers, High-Level Synthesis (HLS) is probably a good choice because it requires limited design technical skills. HLS usually provides an RTL description, which includes a data-path and a control-path. The desynchronization process is only applied to the control-path, which is a Finite State Machine (FSM). This method is sufficient to make asynchronous the circuit. Indeed, data are processed step by step in the pipeline stages, thanks to the desynchronized FSM. Thus, the data-path computation time is no longer related to the clock period but rather to the average time for processing data into the pipeline. This tends to improve speed when the pipeline stages are not well-balanced. Moreover, our approach helps to quickly designing data-driven circuits while maintaining a reasonable cost, a similar area and a short time-to-market.

The demonstration presents the software performing the desynchronization flow. It starts from a RTL description of a circuit generated with Catapult from Mentor Graphics. Once the control-path has been extracted, the corresponding FSM is analyzed and generated into an asynchronous control circuit thanks to a formal model of the FSM. The data-path is kept as it is. The resulting circuit is an asynchronous bundled-data circuit.