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WELCOME
GENERAL INFORMATION
KEYNOTE SPEAKERS
Philippe Magarshack, STMicroelectronics, FR
Luca Benini, ETH Zurich, CH
Catherine Schuman, Oak Ridge National Laboratory, US
Jim Tung, MathWorks Fellow, US
Joachim Schultz, German Center for Neurodegenerative Diseases, DE
Philippe Quinio, STMicroelectronics, FR
EXECUTIVE SESSIONS
Giovanni De Micheli, EPFL, CH
Marco Casale-Rossi, Synopsys, IT
SPECIAL DAY „Embedded Artificial Intelligence” – Wednesday
Bernabé Linares, IMSE-CNMI, ES
Li-C Wang, University of California, Santa Barbara, US
SPECIAL-DAY „Silicon Photonics” – Thursday
Gabriela Nicolescu, École Polytechnique de Montréal, CA
Luca Ramini, Hewlett Packard Labs, US
SPECIAL & EU SESSIONS
Giovanni De Micheli, EPFL, CH
Marco Casale-Rossi, Synopsys, IT
Autonomous Systems Design (ASD) Initiative
Rolf Ernst, TU Braunschweig, DE | Selma Saidi, TU Dortmund, DE
Dirk Ziegenbein, Robert Bosch GmbH, DE
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Imprint
The DATE organisation and sponsors would like to extend their warmest gratitude to all press journalists who give DATE coverage in the editorial pages. Listed below are the media houses and publications who generously agreed to form a media partnership with DATE.

57th Design Automation Conference (DAC)
19 – 23 July 2020

Get ready for the 57th DAC to be held in San Francisco, California, July 19 – 23, 2020. Continuing the tradition of being in the forefront of electronic design, the 57th DAC will offer outstanding training and education as well as superb networking opportunities.
www.dac.com

Asia and South Pacific Design Automation Conference (ASP-DAC)
13 – 16 January 2020

ASP-DAC 2020 is the 25th annual international conference on VLSI design automation in Asia and South Pacific regions, one of the most active regions of design and fabrication of silicon chips in the world. The conference aims at providing the Asian and South Pacific CAD/DA and Design community with opportunities of presenting recent advances and with forums for future directions in technologies related to Electronic Design Automation (EDA). The format of the meeting intends to cultivate and promote an instructive and productive interchange of ideas among EDA researchers/developers and system/circuit/device designers. All scientists, engineers, and students who are interested in theoretical and practical aspects of VLSI design and design automation are welcomed to ASP-DAC.
www.aspdac.com

AUTOCAD & Inventor Magazin

AutoCAD & Inventor Magazin covers more than just IT subjects – we report on all aspects of professional life that are important for constructing engineers and planners. We focus especially on innovations in drive technology, automation technology, connectivity, construction components, fluid technology, electrical engineering and materials.
www.autocad-magazin.de

EDACafé

EDACafe.Com is the #1 EDA web portal. Thousands of IC, FPGA and System designers visit EDACafé.com to learn the latest news and research design tools and services. The sites attract more than 75,000 unique visitors each month and leverages TechJobsCafé.com to bring you job opportunities targeted to engineering and design. And daily e-newsletters reach more than 40,000 engineering professionals.
For more details visit www.EDACafe.com and www.TechJobsCafe.com

SEMICON Europa 2020
SEMICONDUCTORS DRIVE SMART
10 – 13 November 2020

SEMICON Europa is the annual premier event for the global electronics industry in Europe. The event covers new products and technologies for electronics design and manufacturing, and features technologies from across the electronics supply chain, from electronic design automation to device fabrication (wafer processing) to final manufacturing (assembly, packaging, and test). SEMICON Europa also features emerging markets and technologies, including MEMS and flexible electronics, and a wide range of products, including power electronics, sensors, organic and flexible electronics, imaging devices, bioelectronics, automotive, and other exciting new technologies.
www.semiconeuropa.org

3D & Systems Summit
EXPANDING APPLICATION SPACE
27 – 29 January 2020

The 3D & Systems Summit will address the most relevant and advanced topics related to the 3D roadmap, Heterogeneous Integration and System-In-Package manufacturing.
The brand new agenda will focus on disruptive applications like Mobile IoT, High Reliability and High Performance. Invited high-caliber speakers, an exhibition area, B2B matchmaking, unique networking and business opportunities await all participants and exhibitors.
www.semi.org/eu/connect/events/3d-and-systems-summit

MEMS & Imaging Sensors Summit
22 – 24 June 2020

MEMS, imaging and sensors devices are driving innovation and causing demand to explode in transportation, medical, mobile, industrial and other Internet of Things (IoT) applications. Join the summit to boost your business opportunities, discover more about system integration success stories and responses to demand for data analytics, in particular Artificial Intelligence, being enabled by sensor data collection.
www.semi.org/eu/connect/events/mems-imaging-sensors-summit
Dear Colleague,

We proudly present the Advance Programme of DATE 2020. DATE combines the world’s favourite electronic systems design and test conference with an international exhibition for electronic design, automation and test, from system-level hardware and software implementation right down to integrated circuit design.

The DATE conference will take place from 9 to 13 March 2020 at the Alpexpo Congress Centre in Grenoble, France. Grenoble has a great number of assets such as its manufacturing companies, renowned higher-education institutions and internationally-recognised research laboratories, that make it one of the largest technology and research centres in Europe. Grenoble is the key European semiconductor site with more than 200 companies in micro/nano technologies and embedded software, including 100 start-ups and 90 SMEs, offering the working environment for 38,000 people.

Out of a total of 748 paper submissions received, a large share (39%) is coming from authors in Europe, 27% of submissions are from the Americas, 33% from Asia, and 1% from the rest of the world. Submissions involved more than 2400 authors from 45 different countries, a distribution that clearly demonstrates DATE’s international character, global reach and impact.

For the 23rd year in a row, DATE has prepared an exciting technical programme. With the help of the 328 members of the Technical Programme Committee, who carried out 3014 reviews (mostly four reviews per submission), 194 papers (26%) were finally selected for regular presentation and 82 additional ones (cumulatively 37%, including all papers) for interactive presentation.

On the first day of the DATE week, six in-depth technical tutorials on the main topics of DATE as well as one industry hands-on tutorial will be given by leading experts in their respective fields. The topics cover Early Reliability Analysis in Microprocessor Systems, AI Chip Technologies and DFT Methodologies, Data Analytics for Scalable Computing Systems Design, Security in the Post-Quantum Era, HW/SW codesign of Heterogeneous Parallel Dedicated Systems, Evolutionary computing for EDA, and the Deployment of deep learning networks on FPGA (Mathworks).

The first day of the conference will close with the PhD Forum, where 32 selected students, who have completed their PhD thesis or are about to, can showcase their work to the academia and the industrial community.

During the Opening Ceremony on Tuesday, plenary keynote lectures will be given by Philippe Magarshack, Corporate Vice President at STMicroelectronics, and Luca Benini, Chair of Digital Circuits and Systems at ETH Zurich and Professor at University of Bologna. On the same day, the Executive Track offers hot-topic presentations given by executive speakers from companies leading the design and automation industry. Furthermore, a talk by Catherine Schuman from Oak Ridge National Laboratory, will give an overview of the history of neuromorphic computing and will present the current state of research in the field.

The main conference programme from Tuesday to Thursday includes 55 technical sessions organised in parallel tracks from the four areas

- **D** – Design Methods & Tools
- **A** – Application Design
- **T** – Test and Dependability
- **E** – Embedded and Cyber-physical Systems

and from several special sessions on Hot Topics, such as Memories for Emerging Applications, Architectures for Emerging Technologies (Quantum Computing, Edge Computing, Neural Algorithms, In-Memory Computing, Bio-Inspired Adaptive Hardware), Hardware Security, 3D Integration and Logic Reasoning for Functional Engineering Change Order, as well as results and lessons learned from European Projects. Additionally, there are numerous Interactive Presentations which are organised into five IP sessions.

Two Special Days in the programme will focus on areas bringing new challenges to the system design community: Embedded Artificial Intelligence and Silicon Photonics. Each of the Special Days will have a full programme of keynotes, panels, tutorials and technical presentations.

The Special Day on Embedded AI will cover new trends in cognitive algorithms, hardware architectures, software designs, emerging device technologies as well as the application space for deploying AI into edge devices. The topics will include technical areas to enable the realization of embedded artificial intelligence on specialized chips, such as bio-inspired chips, with and without self-learning capabilities, special low-power accelerator chips for aiding in vector/matrix-based computations, convolution and deep-net chips for possible machine learning, cognitive, and perception applications in health, automotive, robotics, or smart cities applications. A particular highlight of the day will be the luncheon keynote given by Jim Tung, who will present MathWorks’ vision on how to leverage Embedded Intelligence in Industry.

The Special Day on Silicon Photonics will focus on data communication via photonics for both data centre/high-performance computing and optical networks on chip applications. Industrial and academic experts will highlight recent advances on devices and integrated circuits. The sessions will also feature talks on design automation and link-level simulations. Other applications of silicon photonics such as sensing and optical compute will also be discussed. As a highlight of the special day, Joachim Schultz from DZNE will talk about bottlenecks and challenges for HPC in medicinal and genomics research during his luncheon keynote.
A timely Special Initiative on “Autonomous Systems Design - Automated Vehicles and Beyond” is held on Thursday and Friday, consisting of reviewed and invited papers as well as working sessions.

To inform attendees on commercial and design-related topics, there will be a full programme in the Exhibition Theatre, which will combine presentations by exhibiting companies, best-practice reports by industry leaders on their latest design projects and selected conference special sessions. A special industrial keynote will be given by Philippe Quinio, STMicroelectronics. The conference is complemented by an exhibition, running for three days (Tuesday – Thursday), including exhibition booths from companies, and collaborative research initiatives among which, also EU project presentations. The exhibition provides a unique networking opportunity and is the perfect venue for industries to meet university professors to foster university programmes and especially for PhD students to meet future employers.

On Friday, eight full-day workshops cover several hot topics in the areas of Autonomous Systems Design, Optical/Photonic Interconnects, Computation-In-Memory, Open-Source Design Automation, Stochastic Computing for Neuromorphic Architectures, Hardware Security, Quantum Computing and Imaging Solutions.

We wish you an exciting and memorable DATE 2020, a successful exhibition visit and an entertaining DATE Party on Wednesday evening.

DATE 2020 General Chair
Giorgio Di Natale
TIMA Laboratory (CNRS, Université Grenoble Alpes, Grenoble INP), FR

DATE 2020 Programme Chair
Cristiana Bolchini
Politecnico di Milano, IT

This printed programme is intended to provide delegates with an easy reference document during their attendance at DATE 2020. Full conference information including all technical programme details, information on awards, conference registration costs, information about accommodation, travel offers and social events is available on the conference website www.date-conference.com.

Dates and Venue
The conference will take place in the two buildings “Espace 1968” and “Alpes Congrès” of Alpexpo in Grenoble, FR, from 9 to 13 March 2020.

Alpexpo
2 Avenue d’Innsbruck
38100 Grenoble, FR
www.alpexpo.com

The accompanying exhibition is scheduled from 10 to 12 March 2020 and will take place in “Salon des Médailleurs” of Espace 1968, which will also host the coffee breaks.

Online Programme
The conference programme is available on the website www.date-conference.com, where you will be able to view the entire details of the programme and plan your attendance.

Internet Access
Free wireless internet access is available on-site throughout the whole congress centre during the entire DATE week. The login information will be provided at the registration desk upon arrival (entrance foyer of Espace 1968).

Proceedings
The conference proceedings are available for download on-site through the DATE wireless network for every fully registered conference delegate at the following link: www.date-conference.com/proceedings

WHova Conference App
The Whova app can be downloaded via the following link or in the Apple/Google stores for free: https://whova.com/download
Please install the app and search for the conference
“DATE 2020” > Password: “DATE”
A browser version can be accessed at https://whova.com/webapp/e/date_202003/

Online Conference Evaluation via the WHova App (“survey” button): every fully registered delegate, who completes the online conference evaluation via the app or the DATE webpage, will receive one of the exclusive DATE collector mugs at the registration desk (when showing the confirmation page).

Breaks
Coffee Break in the Exhibition Area
On all conference days (Tuesday to Thursday), coffee and tea will be served during the coffee breaks in the Exhibition Area in “Salon des Médailleurs” of Espace 1968 at the below-mentioned times.
Seated Lunch in the Lunch Area
On all conference days (Tuesday to Thursday), a seated lunch (lunch buffet) will be offered in the Lunch Area in the Alpes Congrès building to fully registered conference delegates only. There will be an access control at the entrance to the Alpes Congrès building.

Tuesday, 10 March 2020
Coffee Break 1030 – 1130 supported by Hisilicon
Lunch Break 1300 – 1430
Keynote in “Jean Prouvé” 1350 – 1420
Coffee Break 1600 – 1700

Wednesday, 11 March 2020
Coffee Break 1000 – 1100
Lunch Break 1230 – 1430
Keynote in “Jean Prouvé” 1345 – 1420 supported by CEDA
Coffee Break 1600 – 1700

Thursday, 12 March 2020
Coffee Break 1000 – 1100
Lunch Break 1230 – 1400
Keynote in “Jean Prouvé” 1320 – 1350
Coffee Break 1530 – 1600

Welcome Reception & PhD Forum
Monday, 9 March 2020
hosted by EDAA, ACM SIGDA and IEEE CEDA
All registered conference delegates and exhibition visitors are kindly invited to join the DATE 2020 Welcome Reception & PhD Forum, which will take place in the Lunch Area in the Alpes Congrès building on Monday, 9 March 2020, 1800 – 2100.

The PhD Forum of the DATE Conference is a poster session and a buffet style dinner hosted by the European Design Automation Association (EDAA), the ACM Special Interest Group on Design Automation (SIGDA), and the IEEE Council on Electronic Design Automation (CEDA). The purpose of the PhD Forum is to offer a forum for PhD students to discuss their thesis and research work with people of the design automation and system design community. It represents a good opportunity for students to get exposure on the job market and to receive valuable feedback on their work.

Interactive Presentations
sponsored by Cadence Academic Network
Interactive presentations allow presenters to interactively discuss novel ideas and work in progress, which may require additional research work and discussion, with other researchers working in the same area. Interested attendees can walk around freely and talk to any author they want in a vivid face-to-face format. IP presentations will also be accompanied by a poster. Each IP will additionally be introduced in a relevant regular session prior to the IP Session in a one-minute presentation.

To give an overview, there will be one central projection displaying a list of all the presentations going on at the same time in the IP area. Interactive Presentation (IP) Sessions will be held in the Poster Area in “Salon des Médaillés” of Espace 1968 in 30-minute time slots on the following days:

Tuesday, 10 March 2020
IP Session 1 1600 – 1630
IP Session 2 1000 – 1030
IP Session 3 1600 – 1630

Wednesday, 11 March 2020
IP Session 4 1000 – 1030
IP Session 5 1530 – 1600

Presentation of the Best IP Award during the DATE Party (Summum)
Thursday, 12 March 2020
**TUESDAY OPENING SESSION**

Luca Benini

**AMPHITÉÂTRE DAUPHINE**  
10 MARCH 2020, 0955–1030

1.1.2 | Open Parallel Ultra-Low Power Platforms for Extreme Edge AI

Luca Benini, ETH Zurich, CH

Edge Artificial Intelligence is the new megatrend, as privacy concerns and networks bandwidth/latency bottlenecks prevent cloud offloading of sensor analytics functions in many application domains, from autonomous driving to advanced prosthetic. The next wave of „Extreme Edge AI“ pushes aggressively towards sensors and actuators, opening major research and business development opportunities. In this talk, I will give an overview of recent efforts in developing an Extreme Edge AI platform based on open source parallel ultra-low power (PULP) Risc-V processors and accelerators. I will then look at what comes next in this brave new world of hardware renaissance.

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**TUESDAY LUNCHTIME KEYNOTE**

Catherine Schuman

**AMPHITÉÂTRE JEAN PROUVÉ**  
10 MARCH 2020, 1350 – 1420

3.0 | Neuromorphic Computing: Past, Present, and Future

Catherine Schuman, Oak Ridge National Laboratory, US

Though neuromorphic systems were introduced decades ago, there has been a resurgence of interest in recent years due to the looming end of Moore’s law, the end of Dennard scaling, and the tremendous success of AI and deep learning for a wide variety of applications. With this renewed interest, there is a diverse set of research ongoing in neuromorphic computing, ranging from novel hardware implementations, device and materials to the development of new training and learning algorithms. There are many potential advantages to neuromorphic systems that make them attractive in today’s computing landscape, including the potential for very low power, efficient hardware that can perform neural network computation. Though some compelling results have been demonstrated thus far that demonstrate these advantages, there is still significant opportunity for innovations in hardware, algorithms, and applications in neuromorphic computing. In this talk, a brief overview of the history of neuromorphic computing will be discussed, and a summary of the current state of research in the field will be presented. Finally, a list of key challenges, open questions, and opportunities for future research in neuromorphic computing will be enumerated.
Jim Tung, MathWorks, US

The buzz about AI is deafening. Compelling applications are starting to emerge, dramatically changing the customer service that we experience, the marketing messages that we receive, and some systems we use. But, as organizations decide whether and how to incorporate AI in their systems and services, they must bring together new combinations of specialized knowledge, domain expertise, and business objectives. They must navigate through numerous choices – algorithms, processors, compute placement, data availability, architectural allocation, communications, and more. At the same time, they must keep their focus on the applications that will create compelling value for them. In this keynote, Jim Tung looks at the promising opportunities and practical challenges of building AI into our systems and services.

supported by IEEE CEDA

Joachim Schultze, German Center for Neurodegenerative Diseases (DZNE e.V.), DE

As any other area of our lives, medicine is experiencing the digital revolution. We produce more and more quantitative data in medicine, and therefore, we need significantly more compute power and data storage capabilities in the near future. Yet, since medicine is inherently decentralized, current compute infrastructures are not built for that. Central cloud storage and centralized supercomputing infrastructures are not helpful in a discipline such as medicine that will produce data always at the edge. Here we completely need to rethink computing. What we require are distributed federated cloud solutions with sufficient memory at the edge to cope with the large sensor data that record many medical data of individual patients. Here memory-driven computing comes in as a perfect solution. Its potential to provide sufficiently large memory at the edge, where data is generated, yet its potential to connect these new devices to build distributed federated cloud solutions will be key to drive the digital revolution in medicine. I will provide our own efforts using memory-driven computing towards this direction.

Philippe Quinio, STMicroelectronics, FR

The Cloud is promising orders of magnitude savings in time to market for integrated circuits, owing to CPU elasticity. However, practical limitations still mandate a selective approach to the product design flow and the business models have yet to be fully defined by vendors. The economic equation of designing in the cloud is challenging. In addition, design houses, IDMs and OEM customers have to decide to what extent they want to rely on Cloud service providers to maintain the confidentiality of their IP or SOC databases and honour export control requirements, in a context where such concerns are increasingly relevant in EDA vendor and IC supplier selection. This keynote will explore those topics based on ST’s own experience and trials.
EXECUTIVE SESSIONS

Co-Chairs:
Giovanni De Micheli, EPFL, CH
Marco Casale-Rossi, Synopsys, IT

DATE 2020 will again feature an Executive Track of presentations by leading industry and academia representatives. This one-day programme will be held on Tuesday, 10 March, the first day of the DATE conference immediately after the Opening Session and will run in parallel to the technical conference tracks. It will be comprised of a lunch keynote and a hot topic session.

The lunch keynote by Dr. Catherine Schuman, Research Scientist at Oak Ridge National Laboratory, TN, USA, will provide an overview of “Neuromorphic Computing: Past, Present, and Future”. The hot topic session will offer new perspectives about the emerging memory architectures, with a special focus on neuromorphic computing, and AIoT applications.

This year’s Executive Track should offer prospective attendees valuable information about the vision and roadmaps of leading companies and research institutions from a business and technology point-of-view.

2.1  MEMORIES FOR EMERGING APPLICATIONS
Chair: Pierre-Emmanuel Gaillardon, University of Utah, US
Co-Chair: Kvatinsky Shahar, Technion, IL
> see page 042

3.0  LUNCHTIME KEYNOTE: NEUROMORPHIC COMPUTING: PAST, PRESENT, AND FUTURE
Catherine Schuman, Oak Ridge National Laboratory, US
> see page 011

EMBEDDED ARTIFICIAL INTELLIGENCE

Co-Chairs:
Bernabé Linares, IMSE-CNM, ES
Li-C Wang, University of California, Santa Barbara, US

Nowadays there are many cognitive applications working on portable mobile devices, which however perform most of their intensive computations on the cloud. This implies power hungry servers spread all over the world, plus an important continuous communication overhead between the edge devices, the internet and the servers, drastically increasing the power consumption of world-wide internet. If internet power consumption keeps increasing with the present trend, it is estimated that by 2030 one fifth of the world-wide electricity consumption would be just to keep internet and their servers running.

By moving cognitive computation intense tasks locally on embedded edge devices, not only world-wide internet power consumption growth trend will be reduced, but also users will recover their right to keep their personal data privacy.

In this Special Day on Embedded AI, sessions will be organised to discuss new trends in cognitive algorithms, hardware architectures, software designs, emerging device technologies as well as the application space for deploying AI into edge devices. The topics will include technical areas to enable the realization of embedded artificial intelligence on specialized chips, such as bio-inspired chips, with and without self-learning capabilities, special low power accelerator chips for aiding in vector/matrix-based computations, convolution and deep-net chips, etc for possible machine learning, cognitive, and perception applications in health, automotive, robotics, or smart cities applications.

5.1  TUTORIAL OVERVIEWS
> see page 063

6.1  EMERGING DEVICES, CIRCUITS AND SYSTEMS
> see page 071

7.0  LUNCHTIME KEYNOTE: LEVERAGING EMBEDDED INTELLIGENCE IN INDUSTRY: CHALLENGES AND OPPORTUNITIES
> see page 012

7.1  INDUSTRY AI CHIPS
> see page 077

8.1  NEUROMORPHIC CHIPS AND SYSTEMS
> see page 083
Silicon photonics has emerged as a promising solution in the area of high-performance computing. This emerging technology opens new multi-disciplinary research questions including low-loss CMOS compatible components, as well as software CAD and design tools to explore the design space of the resulting complex devices and systems. The DATE Special Day on Silicon Photonics will focus on data communication via photonics for both data centre/high-performance computing and optical networks-on-chip applications. Industrial and academic experts will highlight recent advances on devices and integrated circuits. The sessions will also feature talks on design automation and link-level simulations. Other applications of silicon photonics such as sensing and optical compute will also be discussed.

**Thursday**

9.1 **Advancements on Silicon Photonics**  
> see page 089

10.1 **High-Speed Silicon Photonics Interconnects for Data Center and HPC**  
> see page 097

11.0 **Lunchtime Keynote: Memory Driven Computing to Revolutionize the Medical Sciences**  
> see page 013

11.1 **Advanced Applications**  
> see page 103

12.1 **Design Automation for Photonics**  
> see page 109

**Tuesday**

3.1 **Special Session: Architectures for Emerging Technologies**  
Chair: Pierre-Emmanuel Gaillardon, University of Utah, US  
Co-Chair: Michael Niemier, University of Notre Dame, US  
> see page 046

3.3 **EU/ESA Projects: Heterogeneous Computing**  
Chair: Carles Hernandez, UPV, ES  
Co-Chair: Francisco J. Cazorla, BSC, ES  
> see page 048

4.3 **EU Projects: Nanoelectronics with CMOS and Alternative Technologies**  
Chair: Dimitris Gizopoulos, University of Athens, GR  
Co-Chair: George Karakonstantis, Queen’s University Belfast, GB  
> see page 057
**WEDNESDAY**

5.3 SPECIAL SESSION: SECURE COMPOSITION OF HARDWARE SYSTEMS  
Chair: Ilia Polian, University of Stuttgart, DE  
Co-Chair: Francesco Regazzoni, ALaRI, CH  
> see page 064

5.8 SPECIAL SESSION: HIGH-LEVEL SYNTHESIS FOR AI HARDWARE  
Chair: Massimo Cecchetti, Mentor, A Siemens Business, US  
Co-Chair: Astrid Ernst, Mentor, A Siemens Business, US  
> see page 068

6.3 SPECIAL SESSION: MODERN LOGIC REASONING METHODS FOR FUNCTIONAL ECO  
Chair: Patrick Vuillod, Synopsys, US  
Co-Chair: Christoph Scholl, Albert-Ludwigs-University Freiburg, DE  
> see page 072

7.3 SPECIAL SESSION: REALIZING QUANTUM ALGORITHMS ON REAL QUANTUM COMPUTING DEVICES  
Chair: Eduard Alarcon, Universitat Politècnica de Catalunya, ES  
Co-Chair: Swaroop Ghosh, Pennsylvania State University, US  
> see page 078

**THURSDAY**

9.3 SPECIAL SESSION: IN-MEMORY COMPUTING FOR EDGE AI  
Chair: Maha Kooli, CEA-Leti, FR  
Co-Chair: Alexandre Levisse, EPFL, CH  
> see page 090

9.8 SPECIAL SESSION – PANEL: VARIATION-AWARE ANALYSES OF MEGA-MOSFET MEMORIES, CHALLENGES AND SOLUTIONS  
Moderators:  
Firas Mohamed, Silvaco, FR  
Jean-Baptiste Duluc, Silvaco, FR  
> see page 094

10.3 SPECIAL SESSION: NEXT GENERATION ARITHMETIC FOR EDGE COMPUTING  
Chair: Farhad Merchant, RWTH Aachen University, DE  
Co-Chair: Akash Kumar, TU Dresden, DE  
> see page 098

11.3 SPECIAL SESSION: EMERGING NEURAL ALGORITHMS AND THEIR IMPACT ON HARDWARE  
Chair: Ian O’Connor, École Centrale de Lyon, FR  
Co-Chair: Michael Niemier, University of Notre Dame, US  
> see page 104

11.8 SPECIAL SESSION: SELF-AWARE, BIOLOGICALLY-INSPIRED ADAPTIVE HARDWARE SYSTEMS FOR ULTIMATE DEPENDABILITY AND LONGEVITY  
Chair: Martin A. Trefzer, University of York, GB  
Co-Chair: Andy M. Tyrrell, University of York, GB  
> see page 106

12.8 SPECIAL SESSION: EDA CHALLENGES IN MONOLITHIC 3D INTEGRATION: FROM CIRCUITS TO SYSTEMS  
Chair: Pascal Vivet, CEA-Leti, FR  
Co-Chair: Mehdi Tahoori, Karlsruhe Institute of Technology, DE  
> see page 113
SPECIAL INITIATIVE

TWO-DAY INITIATIVE ON AUTONOMOUS SYSTEMS DESIGN – AUTOMATED VEHICLES AND BEYOND

Initiative Organisers:
Rolf Ernst, TU Braunschweig, DE
Selma Saidi, TU Dortmund, DE
Dirk Ziegenbein, Robert Bosch GmbH, DE

The DATE initiative on Autonomous Systems Design (ASD) is a two-day special event at DATE. It focuses on recent trends and emerging design challenges in the field of autonomous systems. Such systems are becoming more and more integral parts of many internet-of-things and cyber-physical systems applications. Automated driving constitutes today one of the best examples of this trend, in addition to other application domains such as avionics and robotics. The ASD initiative is organised as a Thursday Special Day and Friday Workshop to constitute a two-day continuous program covering architectures and frameworks for autonomous systems, adaptive techniques for managing software and environmental uncertainty, and formal verification methods for safety assurance in machine learning algorithms. The initiative gathers distinguished speakers from both academia and industry, including participation from Airbus, AUDI AG, DENSO Automotive, NXP Semiconductor, Robert Bosch GmbH, Toyota Research Institute, Volkswagen AG and Volokopter.

THURSDAY SPECIAL DAY

9.2 ARCHITECTURES AND FRAMEWORKS FOR AUTONOMOUS SYSTEMS
> see page 089

10.2 UNCERTAINTY HANDLING IN SAFE AUTONOMOUS SYSTEMS (UHSAS)
> see page 098

11.2 AUTONOMOUS CYBER-PHYSICAL SYSTEMS: MODELLING AND VERIFICATION
> see page 103

12.2 EMERGING APPROACHES TO AUTONOMOUS SYSTEMS DESIGN
> see page 109

ASD INITIATIVE RECEPTION
supported by AID
Autonomous Intelligent Driving GmbH
> see page 110

FRIDAY WORKSHOP

W03 SECOND DATE WORKSHOP ON AUTONOMOUS SYSTEMS DESIGN (ASD 2020)
> see page 148

AUTONOMOUS RENAULT ZOE:
Autonomous Driving Demo: Focus on the Embedded Bayesian Perception Component
INRIA Rhone-Alpes, FR
MONDAY, 9 MARCH 2020
- Monday Tutorials
- Half-day Forum “Advancing Diversity in EDA”, supported by IEEE CEDA and ACM SIGDA
- Fringe Meetings
- Welcome Reception & PhD Forum, hosted by EDAA, ACM SIGDA and IEEE CEDA

TUESDAY, 10 MARCH 2020
- Opening Session: Plenary, Awards Ceremony & Keynote Addresses
- Technical Conference
- Executive Sessions and Keynote
- Vendor Exhibition & Exhibition Theatre
- University Booth
- Fringe Meetings
- DATE Party | Networking Event supported by HiSilicon

WEDNESDAY, 11 MARCH 2020
- Technical Conference
- Special Day on “Embedded Artificial Intelligence” and Keynote
- Interactive Presentations IP2 and IP3
- Vendor Exhibition & Exhibition Theatre
- University Booth
- Fringe Meetings
- DATE Party | Networking Event supported by HiSilicon

THURSDAY, 12 MARCH 2020
- Technical Conference
- Special Day on “Silicon Photonics” and Keynote
- Special Initiative on “Autonomous Systems Design”
- Interactive Presentations IP4 and IP5
- Vendor Exhibition, Exhibition Theatre and Exhibition Keynote
- University Booth
- Fringe Meetings

FRIDAY, 13 MARCH 2020
- Special Interest Workshops
- Special Initiative on “Autonomous Systems Design”

CONTACTS
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EVENT OVERVIEW

MONDAY EVENTS

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<tr>
<th>Time</th>
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<tr>
<td>1300</td>
<td>Tutorial and Conference Registration</td>
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<tr>
<td>1400</td>
<td>Start of Tutorials</td>
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<tr>
<td>1530 - 1600</td>
<td>Coffee Break</td>
</tr>
<tr>
<td>1800 - 2100</td>
<td>Welcome Reception &amp; PhD Forum, hosted by EDAA, ACM SIGDA, incl. Awards Presentation, Lunch Area</td>
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Registered tutorial participants can attend any tutorial and may move between tutorials during the session.

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<thead>
<tr>
<th>Time</th>
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<tr>
<td>1400 - 1800</td>
<td>Villard de Lans 2</td>
<td>M04 Security in the Post-Quantum Era: Threats and Countermeasures</td>
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<td>M06</td>
<td>Autrans 1</td>
<td>M06 HW/SW Co-Design of Heterogeneous Parallel Dedicated Systems (HEPSYCODE)</td>
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<tr>
<td>M07</td>
<td>Autrans 2</td>
<td>M07 Evolutionary computing for EDA</td>
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<tr>
<td>M08</td>
<td>Chamrousse</td>
<td>M08 An industry approach to deploying deep learning network on FPGA</td>
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<tr>
<td>1400 - 1800</td>
<td>Lesdiguières</td>
<td>M01 Early System Reliability Analysis for Cross-layer Soft Errors Resilience in Microprocessor Systems</td>
</tr>
<tr>
<td>M02</td>
<td>Bayard</td>
<td>M02 AI Chip Technologies and DFT Methodologies</td>
</tr>
<tr>
<td>M03</td>
<td>Berlioz</td>
<td>M03 Data Analytics for Scalable Computing Systems Design: Challenges, Opportunities, and Solutions</td>
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MONDAY EVENTS

FM09 | FDSOI IP SOC DAY

SAINT-NIZIER
9 MARCH 2020, 1300 – 1800
Organiser: Gabrièle Saucier, Design And Reuse, FR
> see page 163

FM04 | FORUM ON “ADVANCING DIVERSITY IN EDA”
supported by IEEE CEDA and ACM SIGDA

ALPE D’HUEZ
9 MARCH 2020, 1400 – 1800
Organisers:
Chengmo Yang, University of Delaware, US
Nele Mentens, KU Leuven, BE
Ayse Coskun, Boston University, US
> see page 163

FM01 | WELCOME RECEPTION & PHD FORUM

hosted by EDAA, ACM SIGDA and IEEE CEDA

LUNCH AREA
9 MARCH 2020, 1800 – 2100
Organiser: Robert Wille, Johannes Kepler University Linz, AT
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### WEDNESDAY, 11 MARCH 2020

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<td>Registration</td>
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| 0830 | Track 1: Jean Prouvé  
Track 2: Chamrousse  
Track 3: Autrans  
Track 4: Stendhal |  
- 5.1 Tutorial Overviews  
- 5.2 Machine Learning Approaches to Analog Design  
- 5.3 Secure Composition of Hardware Systems  
- 5.4 New Frontiers in Formal Verification for Hardware  
- 5.5 Model-Based Analysis and Security  
- 5.6 Logic synthesis towards fast, compact, and secure designs  
- 5.7 Stochastic Computing  
- 5.8 High-Level Synthesis for AI Hardware  
- 5.9 Efficient Data Representations in Neural Networks  
- 5.10 From DFT to Yield Optimization  
- 5.11 Safety and efficiency for smart automotive and energy systems  
- 5.12 Solutions for EDA Design Environments |
| 0900 | Exhibition and Coffee Break |
| 1000 | Exhibition Theatre  
1000 – 1030 | IP2 Interactive Presentations, Poster Area |
| 1030 | Track 5: Bayard  
Track 6: Lesdiguières  
Track 7: Berlioz  
Exhibition Theatre: Alpe d’Huez |  
- 6.1 Emerging Devices, Circuits and Systems  
- 6.2 Secure and fast memory and storage  
- 6.3 Modern Logic Reasoning Methods for Functional ECO  
- 6.4 Micro-architecture to the rescue of memory  
- 6.5 Efficient Data Representations in Neural Networks  
- 6.6 From DFT to Yield Optimization  
- 6.7 Safety and efficiency for smart automotive and energy systems  
- 6.8 Solutions for EDA Design Environments |
| 1100 | Exhibition and Lunch Break |
| 1130 | Keynote supported by IEEE CEDA, Jean Prouvé |
| 1300 | Track 5: Bayard  
Track 6: Lesdiguières  
Track 7: Berlioz  
Exhibition Theatre: Alpe d’Huez |  
- 7.1 Industry AI chips  
- 7.2 Reconfigurable Systems and Architectures  
- 7.3 Realizing Quantum Algorithms on Real Quantum Computing Devices  
- 7.4 Simulation and verification: where real issues meet scientific innovation  
- 7.5 Runtime support for multi/many cores  
- 7.6 Attacks on Hardware Architectures  
- 7.7 Self-Adaptive and Learning Systems  
- 7.8 SystemC-based Virtual Prototyping: From SoC Modelling to the Digital Twin Revolution |
| 1330 | Exhibition and Lunch Break |
| 1400 | Keynote supported by IEEE CEDA, Jean Prouvé |
| 1500 | Track 5: Bayard  
Track 6: Lesdiguières  
Track 7: Berlioz  
Exhibition Theatre: Alpe d’Huez |  
- 8.1 Neuromorphic chips and systems  
- 8.2 We are all hackers: design and detection of security attacks  
- 8.3 Optimizing System-Level Design for Machine Learning  
- 8.4 Architectural and Circuit Techniques toward Energy-efficient Computing  
- 8.5 CNN Dataflow Optimizations  
- 8.6 Micro-architecture-level reliability analysis and protection  
- 8.7 Physical Design and Analysis  
- 8.8 MathWorks Tutorial |
| 1530 | Exhibition and Coffee Break |
| 1600 | Exhibition Theatre  
1600 – 1630 | IP3 Interactive Presentations, Poster Area |
| 1630 | Keynote supported by IEEE CEDA, Jean Prouvé |
| 1700 | Track 5: Bayard  
Track 6: Lesdiguières  
Track 7: Berlioz  
Exhibition Theatre: Alpe d’Huez |
| 1730 | Keynote supported by IEEE CEDA, Jean Prouvé |
| 1800 | Track 5: Bayard  
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**Opening & Executive Sessions**  
**Keynotes**  
**Special & EU Sessions**  
**IP Sessions**  
**Exhibition Theatre**
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<td>Registration</td>
<td>Speaker’s Breakfast, Lunch Area</td>
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<tr>
<td>0830 – 1000</td>
<td>9.1 Advancements on Silicon Photonics</td>
<td>9.2 Architectures and Frameworks for Autonomous Systems</td>
<td>9.3 In-Memory Computing for Edge AI</td>
<td>9.4 Efficient DNN design with Approximate Computing</td>
</tr>
<tr>
<td>1000 – 1100</td>
<td>Exhibition and Coffee Break</td>
<td>Exhibition and Coffee Break</td>
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</tr>
<tr>
<td>1100 – 1230</td>
<td>10.1 High-Speed Silicon Photonics Interconnects for Data Center and HPC</td>
<td>10.2 Uncertainty Handling in Safe Autonomous Systems</td>
<td>10.3 Next Generation Arithmetic for Edge Computing</td>
<td>10.4 Design Methodologies for Hardware Approximation</td>
</tr>
<tr>
<td>1230 – 1400</td>
<td>Exhibition and Lunch Break</td>
<td>Exhibition and Lunch Break</td>
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<tr>
<td>1530 – 1600</td>
<td>Exhibition and Coffee Break</td>
<td>Exhibition and Coffee Break</td>
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**Special Day Sessions | Keynotes**

**Special & EU Sessions**

**ASD Initiative**

**IP Sessions**

**Exhibition Theatre**

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**Track 5**

**Bayard**

9.5 Emerging memory devices

9.6 Intelligent Dependable Systems

9.7 Diverse Applications of Emerging Technologies

9.8 Panel: Variation-aware analyzes of Mega-MOSFET Memories, Challenges and Solutions

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**Track 6**

**Lesdiguières**

10.5 Emerging Machine Learning Applications and Models

10.6 Secure Processor Architecture

10.7 Accelerators for Neuromorphic Computing

10.8 Exhibition Theatre Keynote and Publisher’s Session

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**Track 7**

**Berlioz**

11.5 Compile time and virtualization support for embedded system design

11.6 Aging: estimation and mitigation

11.7 System Level Security

11.8 Self-aware, biologically-inspired adaptive hardware systems for ultimate dependability and longevity

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**Exhibition Theatre Alpe d’Huez**

12.5 Cyber-Physical Systems for Manufacturing and Transportation

12.6 Industrial Experience: From Wafer-Level Up to IoT Security

12.7 Power-efficient multi-core embedded architectures

12.8 EDA Challenges in Monolithic 3D Integration: From Circuits to Systems
**MONDAY TUTORIALS**

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<td>Workshop Registration and Welcome Refreshments</td>
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<td>Coffee Break</td>
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<td>1200</td>
<td>Lunch Break</td>
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<tr>
<td>1430</td>
<td>Coffee Break</td>
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**ESPACE 1968 | LEVEL 1**

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<tr>
<th>Location</th>
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<tr>
<td>Chamrousse</td>
<td>W03 Second DATE Workshop on Autonomous Systems Design (ASD 2020)</td>
</tr>
<tr>
<td>Autrans 1</td>
<td>W07 Workshop on Trustworthy Manufacturing and Utilization of Secure Devices (TRUDEVICE 2020)</td>
</tr>
<tr>
<td>Villard de Lans 2</td>
<td>W06 Stochastic Computing for Neuromorphic Architectures (SCONA)</td>
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<tr>
<td>Saint-Nizier</td>
<td>W08 Workshop on Quantum Computing</td>
</tr>
<tr>
<td>Alpe d’Huez</td>
<td>W09 IRT NANOELEC: bridging the gap between Semiconductor technologies and architecture Design</td>
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**ALPES CONGRÈS | LEVEL 0**

<table>
<thead>
<tr>
<th>Location</th>
<th>Workshop</th>
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<tbody>
<tr>
<td>Lesdiguières</td>
<td>W01 Optical/ Photonic Interconnects for Computing Systems (OPTICS)</td>
</tr>
<tr>
<td>Berlioz</td>
<td>W02 Computation -In-Memory (CIM): from Device to Applications</td>
</tr>
<tr>
<td>Bayard</td>
<td>W05 2nd Workshop Open-Soure Design Automation (OSDA 2020)</td>
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**M01 EARLY SYSTEM RELIABILITY ANALYSIS FOR CROSS-LAYER SOFT ERRORS RESILIENCE IN MICROPROCESSOR SYSTEMS**

**LESDIGUIÈRES 1400 – 1800**

**Organisers**

- Alberto Bosio, Lyon Institute of Nanotechnology, FR
- Stefano Di Carlo, Politecnico di Torino, IT
- Dimitris Gizopoulos, University of Athens, GR
- Alessandro Savino, Politecnico di Torino, IT
- Ramon Canal, Universitat Politècnica de Catalunya and Barcelona Supercomputing Center, ES

In a world with computation at the epicenter of every activity, computing systems must be highly reliable even if miniaturization makes the underlying hardware unreliable. Techniques able to guarantee high reliability are associated to high costs (reliability tax). Early reliability analysis has the potential to take informed design decisions during to maximize reliability while minimizing the reliability tax. This tutorial focuses on early cross-layer reliability analysis considering the full computing continuum (from IoT/CPS to HPC applications) with emphasis on soft errors. The tutorial will guide attendees from the definition of the problem down to the proper modeling and design exploration strategies considering the full system stack.

**Introduction to Reliability**

Reliability is a very broad domain in which several (sometimes competing) communities have provided significant contributions. However, as often happens, definitions and metrics have different meaning in different communities creating a serious obstacle in sharing of knowledge and in the efficient implementation of cross-layer reliability techniques that require synergy between all layers of the system stack.

To overcome this problem in this introduction prof. Gizopoulos will provide an overview of the basic concepts, definitions and metrics required to work in the reliability domains trying to build a common language that could be understood by researchers with different background (e.g., hardware vs software developers).

**Cross-Layer Reliability Techniques Overview**

Cross-layer reliability (or cross-layer resilience) is gaining increasing relevance both in the academic and industrial sectors. In a cross-layer resilient system, physical and circuit level techniques can mitigate low-level faults. Hardware redundancy can be used to manage errors at the hardware architecture layer. Eventually, software implemented error detection and correction mechanisms can manage those errors that escaped the lower layers of the stack. In order to understand the potential but also the complexity of this design paradigm prof. Di Carlo will give a brief overview of the most used protection techniques available at the different layers including:

- Logic Layer
- Architectural Layer
- Software Layer
- System-Layer
The goal is not to provide an exhaustive review of the state-of-the-art but to give an idea of the building blocks that can be exploited in a cross-layer resilient design and most importantly to let the audience understand the size and complexity of the related design space that makes the reliability analysis a crucial task in the early phases of the design.

**Reliability analysis in a Cross-Layer Domain**

The decision of how to distribute the error management across the different layers has the goal to meet the system reliability requirements of a specific application, considering its sensitivity to hardware faults while minimizing the related reliability tax. Overall, by considering multiple layers, one can exploit a wider range of information when handling errors. This leads to globally optimized error management strategies dedicated not only to reliability, but also to other design constraints. However, despite a cross-layer holistic design approach has several advantages compared to traditional single layer techniques, it increases the complexity of the design process since a larger design space must be explored. This translates into an increasing demand for system-level reliability analysis frameworks able to evaluate different combinations of cross-layer error protection techniques early in the design cycle. Unfortunately, such tools still lack maturity, especially compared to those available to optimize other design parameters such as power and performance.

This represents the core of the tutorial in which all presenters will exploit their experience in several years of research and collaboration in this domain to guide the audience in an overview of the main reliability analysis on a cross-layer domain. In particular the tutorial will cover the following topics:

- **Fault Injection approaches**
  - Device Level
  - Microarchitectural Level
  - ISA/Software Level
- **Stochastic Cross-Layer Modelling and Analysis**

This tutorial presents methodologies and results obtained in the framework of several EC projects including in which the presenters have been actively involved: CLERECO - FP7 (https://www.clereco.eu), UniServer - H2020 (http://www.uniserver2020.eu/) and RECIPE - FETHPC project (http://www.recipe-project.eu/). Evolutionary approaches to the design of variability-aware cells, SRAM and analogue circuits.
M03  DATA ANALYTICS FOR SCALABLE COMPUTING
SYSTEMS DESIGN: CHALLENGES, OPPORTUNITIES,
AND SOLUTIONS
BERLIOZ  1400 – 1800

Organisers
Partha Pratim Pande, Washington State University, US
Krishnendu Chakrabarty, Duke University, US

Speakers
Jana Doppa, Washington State University, US
Hai (Helen) Li, Duke University/TUM-IAS, US
Rob Aitken, ARM, US

Abstract
The rate of growth of Big Data, slowing down of Moore’s law,
and the rise of emerging applications pose significant challenges
in the design of large-scale computing systems with high-perfor-
manence, energy-efficiency, and reliability. This tutorial will con-
sider solutions based on machine learning and data analytics to
address various challenges and answer the following questions:
1. How to use machine learning and statistical modeling for ef-
effective design space exploration of computing systems to op-
timize for power, performance, and thermal metrics?
2. How to use machine learning techniques to efficiently manage
resources of computing systems (e.g., power, memory, inter-
connects) to improve performance and energy-efficiency?
3. What are the challenges in Processing-in-Memory (PIM) to ef-
solutely solve machine learning algorithms?
4. How can data analytics facilitate fault diagnosis, detect anom-
alies, and increase robustness in the network backbone of
emerging large-scale networking systems?
5. How can machine learning be used during the design process
to produce higher quality, more robust manufactured devices?

To address these outstanding challenges, out-of-the-box ap-
proaches need to be explored. By integrating machine learning
algorithms, data analytics, statistical modeling, and design of ad-
vanced computing systems, this tutorial will engage a broad sec-
ton of DATE conference attendees. This tutorial will attract new-
comers who want to learn how to apply machine learning and
data analytics to solve problems in computing systems, as well
as experienced researchers looking for exciting new directions in
computing systems design, EDA methodologies, and multi-scale
computing. This tutorial covers design, optimization and resil-
ience: three main pillars of designing computing systems. It also
highlights how machine learning and EDA researchers can join
hands to design energy-efficient and reliable chips and systems.

Objectives
The main objective of the tutorial is to help attendees understand
the emerging inter-dependence of data analytics and computer
system design. We will elaborate the most important hard-
ware-software co-design challenges that both data analytics and
EDA community need to fully comprehend. We will provide an
overview of some interesting emerging solutions to these prob-
lems. Specific aims are as follows:

- Design principles for advanced manycore systems as an en-
abler for machine learning and big data applications
- Data-driven methods for design space exploration and dynamic
resource management
- Accelerator designs on conventional and emerging platforms
- Ensure proactive fault tolerance through failure prediction
based on time-series data analysis
- Machine learning inspired test, manufacturing and validation
methodologies

1400–1530  SESSION 1
1400–1445  Machine Learning for Scalable Design Optimization: Theory-
Guided Practical Algorithms
1445–1530  Machine Learning for Design Space Exploration
and Optimization of Manycore Systems

1530–1600  Coffee Break

1600–1800  SESSION 2
1600–1640  Deep Learning and Neuromorphic Computing - Technology,
Hardware and Implementation
1640–1720  Predictive Analytics for Anomaly Detection and Failure
Prediction in Complex Core Routers
1700–1800  Machine learning for testable, robust and manufacturable
designs

1800–2100  Welcome Reception & PhD Forum
hosted by EDAA, ACM SIGDA, and IEEE CEDA
The advancements in the area of high fidelity qubit technologies, resilient quantum circuits and algorithms have fuelled the development of scalable quantum computers. This brings forth serious consequences for security, especially, the public-key cryptography. The dominant protocols in the public-key cryptography are shown to be vulnerable in face of a quantumenabled adversary. Therefore, it is of prime importance to understand these trends, and how the security research is gearing up to address these challenges.

This tutorial will discuss the growth of scalable quantum computers, their challenges and the latest research to solve practical problems using NISQ computers. Glue talks will cover the corresponding threats caused by these machines. Based on that, the tutorial will discuss various post-quantum primitives. Finally, new vulnerabilities in post-quantum cryptography are presented, opening up a new research direction.

**CHALLENGES OF SCALABLE QUANTUM COMPUTING**

*Quantum Technology Overview*

**Speaker:** Swaroop Ghosh, Pennsylvania State University, US

*EDA for Quantum Computing*

**Speaker:** Robert Wille, Johannes Kepler University Linz, AT

*Scalable Quantum Computer*

**Speaker:** Koen Bertels, TU Delft, NL

*Security Threats from Quantum Computers*

**Speaker:** Anupam Chattopadhyay, Nanyang Technological University, SG

**POST-QUANTUM SECURITY PRIMITIVES**

*Quantum Key Distribution*

**Speaker:** Francesco Regazzoni, Alarri, CH

*Quantum Random Number Generators*

**Speaker:** Swaroop Ghosh, Pennsylvania State University, US

*Post-Quantum Cryptography*

**Speaker:** Sujay Sinha Roy, University of Birmingham, GB

*Beyond Post-Quantum Security*

**Speaker:** Shivam Bhasin, Nanyang Technological University, SG

1800–2100 Welcome Reception & PhD Forum

hosted by EDAA, ACM SIGDA, and IEEE CEDA

In the last years, the spread and importance of embedded systems are even more increasing, but it is still not yet possible to completely standardize and engineer their system-level design flow. The main design problems are to model functional (F) and non-functional (NF) requirements and to validate the system before implementation. Designers commonly use one or more system-level models (e.g. block diagrams, UML, SystemC, etc.) to have a complete problem view and to perform a check on HW/SW resource allocation by simulating the system behavior. In this scenario, SW tools to support designers to reduce cost and overall complexity of systems development are even more of fundamental importance. Co-existence of functional and non-functional requirements is the most relevant challenge. Unfortunately, there are no general methodologies defined for this purpose and often the only option is to refer to experienced designer indications, for taking advantage of empirical criteria and qualitative assessments. In such a context, this tutorial faces the problem of the HW/SW co-design of dedicated/embedded systems based on heterogeneous parallel architectures and presents a methodology (with related prototypal tools), called HepsyCode, able to support the development of such systems in different application domains.

**Main objectives:**

- to present the state of the art about the most used commercial and academic design tools in the field of hw/sw co-design (with particular attention to design space exploration considering F and NF requirements)
- to present a methodology, called HepsyCode, able to support the development of heterogeneous parallel embedded/dedicated systems in different application domains
- to show live demos related to the use of HepsyCode with one or more case studies

1400–1700 A System-Level Methodology for HW/SW Co-Design of Heterogeneous Parallel Dedicated Systems

**Speaker:** Luigi Pomante, Università degli Studi dell’Aquila, IT

1700–1730 Real-Time and Mixed Criticality Extensions for the HepsyCode Methodology

**Speaker:** Vittoriano Muttillo, Università degli Studi dell’Aquila - DEWS, IT

1730–1800 Design for Monitorability: a HW/SW unified approach for embedded system monitoring

**Speaker:** Giacomo Valente, Università degli Studi dell’Aquila - DEWS, IT

1800–2100 Welcome Reception & PhD Forum

hosted by EDAA, ACM SIGDA, and IEEE CEDA
Electronic Design Automation (EDA) methods that use an evolutionary algorithm (EA) as the core optimizer have become more and more popular, especially in the context of new optimization challenges connected with energy-efficient machine learning implemented in embedded systems. The goal of this tutorial is to acquaint the DATE community with the state-of-the-art genetic and evolutionary algorithms, evolutionary circuit design and approximation methods, and demonstrate on several case studies how conventional designs can be improved by means of the evolutionary approach. The tutorial should also lead to better understanding of advantages and disadvantages of the EA-based techniques, principles of the multi-objective optimization (in comparison to the single-objective optimization) and a fair evaluation practice of search-based algorithms. In the first part of the tutorial, we will briefly introduce the principles of evolutionary computing, terminology, the multi-objective optimization driven by the Pareto optimality concept, and fundamental branches of EAs – genetic algorithms (GA) and genetic programming (GP). We will emphasize that a correct statistical evaluation of results is mandatory when stochastic algorithms such as EAs are employed. In the second part, Cartesian Genetic Programming (CGP) will be introduced as a method providing high quality designs of common and approximate digital circuits at different levels of abstraction. Case studies will be focused on evolutionary design of variability-aware cells, approximate arithmetic circuits, image operators, hash functions and neural networks.

This tutorial is primarily devoted to researchers, CAD engineers and students who would like to learn the principles of evolutionary algorithms and how they can be used to design, optimize or approximate circuit designs. Also those who are interested in particular applications such as variability-tolerant design, low-power circuit design, circuit approximation or neural network accelerator optimization will find this tutorial as a useful source of information. After taking the tutorial, the participants should be able to formulate a particular EDA problem as a problem for an EA, i.e. to encode a candidate solution, devise suitable search operators and develop a fitness function.
### SPEAKERS PRESENTING AUTHORS ARE HIGHLIGHTED

#### M08 AN INDUSTRY APPROACH TO DEPLOYING DEEP LEARNING NETWORK ON FPGA

**CHAMROUSSE 1400 – 1800**

**Organiser**

John Zhao, MathWorks, US

FPGAs provide a flexible and attractive edge platform for competitive deep learning accelerators that also support differentiating customization because of their increasing floating-point operation (FLOP) performance and their support for both sparse data and compact data types.

MATLAB and Simulink provide a rich environment for AI system design and deployment, with libraries of proven, specialized algorithms ready to use for specific applications. The environment enables a model-based design workflow for fast prototyping and implementation of the algorithms on heterogeneous embedded targets, such as FPGA or MPSoC.

This tutorial introduces a new workflow enabled by new capabilities in MATLAB that bridges the gap between a pre-trained neural network and general-purpose FPGAs, providing a new approach for graduate students, researchers and engineers in AI technology development or system design to rapidly prototype and prove the concept of their designs or algorithms. You will learn in this seminar, through presentation and examples, how to easily deploy a pre-trained deep learning network on a general purpose FPGAs without writing VHDL code. Specifically, you will learn:

- How to design, train and customize neural network in MATLAB
- How to select the data types in MATLAB for efficient deployment on FPGA
- How to do speed and resource tradeoff for a specific FPGA platform
- How to automatically generate the portable VHDL and Verilog code for the customized inference processor
- How to use the provided interface functions to transfer data between the host MATLAB and the processor on FPGA
- How to integrate the pre-trained neural network processor into a larger system with data pre-processing and post-processing components

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<td>Designing, training and customizing neural network with MATLAB</td>
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<tr>
<td>1445–1600</td>
<td>Generating optimized VHDL/Verilog code for the customized neural network processor and deploying on FPGA</td>
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<tr>
<td>Speaker: John Zhao, MathWorks, US</td>
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<td>1600–1630</td>
<td>Coffee Break in Salon des Médailleurs</td>
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<tr>
<td>1630–1800</td>
<td>Profiling and debugging the neural network processor on FPGA</td>
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<td>using the interface between MATLAB and FPGA</td>
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<tr>
<td>Speaker: John Zhao, MathWorks, US</td>
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<tr>
<td>1800–2100</td>
<td>Welcome Reception &amp; PhD Forum</td>
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2.1 EXECUTIVE SESSION: MEMORIES FOR EMERGING APPLICATIONS

**AMPHITHEÂTRE JEAN PROUVE** 1130 - 1300

- Chair: Pierre-Emmanuel Gaillardon, University of Utah, US
- Co-Chair: Kvatinisky Shahar, Technion, IL

Memories play a prime role in virtually every modern computing systems. While memory technology has been able to follow the aggressive trend of scaling and keep up with the most stringent demands, there exists new applications for which traditional memories struggle to deliver viable solutions. In this context, and more than ever, novel memory technologies are required. Identifying a close match between a killer application and a supporting emerging memory technology will ensure unprecedented capabilities and open durable new horizons for computing systems. In this executive session, we will explore specific cases where novel memories (OxRAM and SOT MRAM in particular) are opening such novel applications unachievable with standard memories.

1130 Resistive RAM and its Dense 3D Integration for the N3XT 1,000X

**Subhasish Mitra**
Stanford University, US

1200 Emerging Memories for Von Neumann and for Neuromorphic Computing

**Jamil Kawa**
Synopsys, US

1230 ReRAM Technology for next generation AI and cost-effective embedded memory

**Amir Regev**
Weebit Nano, AU

1300 Exhibition and Lunch Break

2.2 HARDWARE-ASSISTED SECURE SYSTEMS

**CHAMROUSSE** 1130 - 1300

- Chair: Prabhat Mishra, University of Florida, US
- Co-Chair: Kavan Elif Bilge, University of Sheffield, GB

This session covers state-of-the-art hardware-assisted techniques for secure systems such as random number generators, PUFs, and logic locking & obfuscation. In addition, novel detection methods for hardware Trojans are presented.

1130 Backtracking Search for Optimal Parameters of a PLL-based True Random Number Generator

**Brice Colombier**¹, Nathalie Bochard¹, Florent Bernard² and Lilian Bossuet¹
¹Université de Lyon, FR; ²Laboratory Hubert Curien, Université de Lyon, UJM Saint-Etienne, FR

1200 Long-term Continuous Assessment of SRAM PUF and Source of Random Numbers

**Rui Wang**, Georgios Selimis, Roel Maes and Sven Goossens
Intrinsic-ID, NL

1215 Rescuing Logic Encryption in Post-SAT Era by Locking & Obfuscation

**Amin Rezaei**, Yuanqi Shen and **Hai Zhou**
Northwestern University, US

1230 Selective Concolic Testing for Hardware Trojan Detection in Behavioral SystemC Designs

**Bin Lin**¹, Jinchao Chen² and Fei Xie¹
¹Portland State University, US; ²Northwestern Polytechnical University, CN

1245 Test Pattern Superposition to Detect Hardware Trojans

**Chris Nigh** and **Alex Orailoglu**
University of California, San Diego, US

2.3 FUELING THE FUTURE OF COMPUTING: 3D, TFT, OR DISRUPTIVE MEMORIES?

**AUTRANS** 1130 - 1300

- Chair: Yvain Thonnart, CEA-Leti, FR
- Co-Chair: Marco Vacca, Politecnico di Torino, IT

In the post-CMOS era, the future of computing relies more and more on emerging technologies, like resistive memories, TFT and 3D integration or their combination, to continue performance improvements: from a novel accelerating solution for deep neural networks with ferroelectric transistor technology, to a physical design methodology for face-to-face 3D ICs to enable commercial-quality IC layouts. Furthermore, the monolithic 3D advantage obtained combining TFT and RRAM technology is quantified using a novel open-source CAD flow.

1130 Ternary Compute-Enabled Memory using Ferroelectric Transistors for Accelerating Deep Neural Networks

**Sandeep Krishna Thirumula**, Shubham Jain, Sumeet Gupta and Anand Raghunathan
Purdue University, US

1200 Macro-3D: A Physical Design Methodology for Face-to-Face-Stacked Heterogeneous 3D ICs

**Lennart Bamberg**¹,³, Lingjun Zhu², Sai Pentapati², Da Eun Shim², Alberto Garcia-Ortiz³ and Sung Kyu Lim²
¹GrAi Matter Labs, NL; ²Georgia Tech, US; ³University of Bremen, DE

1230 Quantifying the Benefits of Monolithic 3D Computing Systems Enabled by TFT and RRAM

**Abdallah M. Felfel**¹,³, Kamalika Datta¹, Arko Dutt¹, Hasita Veluri², Ahmed Zaky¹, Aaron Thean² and Mohamed M Sabry Aly¹
¹Nanyang Technological University, SG; ²National University of Singapore, SG; ³Zewail City of Science and Technology, EG


**Ting-Jung Chang**, Zhuozhi Yao, Barry P. Rand and David Wentzlafl
Princeton University, US

1300 Exhibition and Lunch Break
### 2.4 CHALLENGES IN ANALOG DESIGN AUTOMATION & SECURITY

**STENDHAL**

<table>
<thead>
<tr>
<th>Time</th>
<th>Session Title</th>
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<tbody>
<tr>
<td>1130</td>
<td><strong>GANA: Graph Convolutional Network Based Automated Netlist Annotation for Analog Circuits</strong>&lt;br&gt;Kishor Kunal, Tonmoy Dhar, Meghna Madhusudan, Jitesh Poojary, Arvind Sharma, Wenbin Xu, Steven Burns, Jiang Hu, Ramesh Harjani and Sachin S. Sapatnekar&lt;br&gt;&lt;sup&gt;1&lt;/sup&gt;University of Minnesota Twin Cities, US; &lt;sup&gt;2&lt;/sup&gt;Texas A&amp;M University, US; &lt;sup&gt;3&lt;/sup&gt;Intel Corporation, US</td>
</tr>
</tbody>
</table>

**Chair:**  Manuel Barragan, TIMA, FR  
**Co-Chair:**  Haralampos-G. Stratigopoulos, Sorbonne Université, CNRS, LIP6, FR

Producing reliable and secure analog circuits is a challenging task. This session addresses novel and systematic approaches to analog security, based on key sequencing, and analog design, from automatic netlist annotation to Bayesian modeling optimization.

### 2.5 PRUNING TECHNIQUES FOR EMBEDDED NEURAL NETWORKS

**BAYARD**

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<th>Time</th>
<th>Session Title</th>
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<tr>
<td>1130</td>
<td><strong>Deeper Weight Pruning without Accuracy Loss in Deep Neural Networks</strong>&lt;br&gt;Byungmin Ahn and Taewhan Kim&lt;br&gt;Seoul National University, KR</td>
</tr>
</tbody>
</table>

**Chair:**  Marian Verhelst, KU Leuven, BE  
**Co-Chair:**  Dirk Ziegenbein, Robert Bosch GmbH, DE

Network pruning has been applied successfully to reduce the computational and memory footprint of neural network processing. This session presents three innovations to better exploit pruning in embedded processing architectures. The solutions presented extend the sparsity concept to the bit level with an enhanced bit-level pruning technique based on CSD representations, introduce a novel group-level pruning technique, demonstrating an improved trade-off between hardware-execution cost and accuracy loss, and explore a sparsity-aware cache architecture to reduce cache miss rate and execution time.

1200 Flexible Group-Level Pruning of Deep Neural Networks for On-Device Machine Learning  
Kwangbae Lee, Hoseung Kim, Hayun Lee and Dongkun Shin<br>Sungkyunkwan University, KR  

1230 Sparsity-Aware Caches to Accelerate Deep Neural Networks  
**Vinod Ganesan**<sup>1</sup>, Sanchari Sen<sup>2</sup>, Pratyush Kumar<sup>1</sup>, Neel Gala<sup>1</sup>, Kamakoti Veezhinatha<sup>1</sup> and Anand Raghunathan<sup>2</sup><br><sup>1</sup>IIIT Madras, IN; <sup>2</sup>Purdue University, US

1300 Exhibition and Lunch Break

### 2.6 IMPROVING RELIABILITY AND FAULT TOLERANCE OF ADVANCED MEMORIES

**LESDIGUIÈRES**

<table>
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<th>Time</th>
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<tr>
<td>1130</td>
<td><strong>On Improving Fault Tolerance of Memristor Crossbar Based Neural Network Designs by Target Sparsifying</strong>&lt;br&gt;Song Jin, Songwei Pei and Yu Wang&lt;br&gt;&lt;sup&gt;1&lt;/sup&gt;North China Electric Power University, CN; &lt;sup&gt;2&lt;/sup&gt;School of Computer Science, Beijing University of Posts and Telecommunications, CN</td>
</tr>
</tbody>
</table>

**Chair:**  Mounir Benabdenbi, TIMA Laboratory, FR  
**Co-Chair:**  Said Hamdioui, TU Delft, NL

This session discusses reliability issues for different memory technologies; addressing fault tolerance of memristors, how to reduce simulations with importance sampling and advance metrics as measure for the reliability of NAND flash memories.

<table>
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<tr>
<td>1130</td>
<td><strong>An Efficient Yield Analysis of SRAM Using Scaled-Sigma Adaptive Importance Sampling</strong>&lt;br&gt;Liang Pang, Mengyun Yao and Yifan Chai&lt;br&gt;&lt;sup&gt;1&lt;/sup&gt;School of Electronic Science &amp; Engineering, Southeast University, CN; &lt;sup&gt;2&lt;/sup&gt;School of Microelectronics, Southeast University, CN</td>
</tr>
</tbody>
</table>

1200 **Fast and Accurate High-Sigma Failure Rate Estimation through Extended Bayesian Optimized Importance Sampling**  
Michael Hefenbrock, Dennis Weller, Michael Beigl and Mehdi Tahoori<br>Karlsruhe Institute of Technology, DE

1245 **Valid Window: A New Metric to Measure the Reliability of NAND Flash Memory**  
Min Ye, Qiao Li, Jianqiang Nie, Tei-Wei Kuo and Chun Jason Xue<br><sup>1</sup>City University of Hong Kong, HK; <sup>2</sup>YEESTOR Microelectronics Co., Ltd, CN

1300 Exhibition and Lunch Break
2.7  OPTIMIZING EMERGING APPLICATIONS FOR POWER-EFFICIENT COMPUTING

BERLIOZ  1130 - 1300

Chair:  Jungwook Choi, Hanyang University, KR
Co-Chair:  Shafique Muhammad, TU Wien, AT

This session focuses on emerging applications for power-efficient computing, such as bioinformatics and few-shot learning. Methods such as Hyperdimensional computing or computing in memory are applied to process DNA pattern matching or to perform few-shot learning in a more power-efficient way.

1130  GenieHD: Efficient DNA Pattern Matching Accelerator Using Hyperdimensional Computing
Yeseong Kim, Mohsen Imani, Niema Moshiri and Tajana Rosing
University of California, San Diego, US

1200  REPUTE: An OpenCL based Read Mapping Tool for Embedded Genomics
Sidharth Maheshwari, Rishad Shafik, Alex Yakovlev, Ian Wilson and Amit Acharyya
Newcastle University, GB; IT Hyderabad, IN

1230  A Fast and Energy Efficient Computing-in-Memory Architecture for Few-Shot Learning Applications
Dayane Reis, Ann Franchesca Laguna, Michael Niemier and X. Sharon Hu
University of Notre Dame, US

1300  Exhibition and Lunch Break

3.0  LUNCHTIME KEYNOTE SESSION

AMPHITHÉÂTRE JEAN PROUVE  1350 - 1420

Chair:  Marco Casale-Rossi, Synopsys, IT
Co-Chair:  Giovanni De Micheli, EPFL, CH

1350  Neuromorphic Computing: Past, Present, and Future
Catherine Schuman
Oak Ridge National Laboratory, US

> see page 011

3.1  SPECIAL SESSION: ARCHITECTURES FOR EMERGING TECHNOLOGIES

AMPHITHÉÂTRE JEAN PROUVE  1430 - 1600

Chair:  Pierre-Emmanuel Gaillardon, University of Utah, US
Co-Chair:  Michael Niemier, University of Notre Dame, US

The past five decades have witnessed transformations happening at an ever-growing pace thanks to the sustained increase of capabilities of electronics systems. We are now at the dawn of a new revolution where emerging technologies, understand beyond silicon complementary metal oxide semiconductors, are going to further revolutionize the way we design electronics. In this hot topic session, we intend to elaborate on the architectural opportunities and challenges brought by non-standard semiconductor technologies. In addition to provide new perspectives to the DATE community beyond the currently hot novel architectures, such as neuromorphic or in-memory computing, this proposal also serve the purpose of tightening the link between DATE and the EDA community at large with the mission and roles of the IEEE Rebooting Computing Initiative - https://rebootingcomputing.ieee.org.

1430  Cryo-CMOS interfaces for a scalable quantum computer
Edoardo Charbon, Andrei Vladimirescu, Fabio Sebastian and Masoud Babaie
1EPFL, CH; 2University of California, Berkeley, US; 3TU Delft, NL

1445  The N3XT 1,000X for the Coming Superstorm of Abundant Data: Carbon Nanotube FETs, Resistive RAM, Monolithic 3D Gage Hills and Mohamed M. Sabry
1Massachusetts Institute of Technology, US; 2Nanyang Technological University, SG

1500  Multiplier Architectures: Challenges and Opportunities with Plasmonic-based Logic
Eleonora Testa, Samantha Lubaba Noor, Odysseas Zografos, Mathias Soeken, Francky Catthoor, Azad Naemi and Giovanni Demicheli
1EPFL, CH; 2Georgia Tech, US; 3IMEC, BE

1515  Quantum Computer Architecture: Towards Full-Stack Quantum Accelerators
TU Delft, NL

1530  Utilizing buried power rails and backside PDN to further CMOS scaling below 5nm nodes
Odysseas Zografos, Sudhir Patli, Satadru Sarkar, Bilal Chehab, Doyoung Jang, Rogier Baert, Peter Debacker, Myung-Hee Na and Julien Ryckaert
IMEC, BE

1545  A RRAM-based FPGA for Energy-efficient Edge Computing
Xifan Tang, Ganesh Gore, Patsy Cadareanu, Edouard Giacomin and Pierre-Emmanuel Gaillardon
University of Utah, US

1600  Exhibition and Coffee Break

3.2  ACCELERATING DESIGN SPACE EXPLORATION

LESDIGUIÈRES  1430 - 1600

Chair:  Christian Pilato, Politecnico di Milano, IT
Co-Chair:  Luca Carloni, Columbia University, US

Accelerating Design Space Exploration efficiently is needed to optimize hardware accelerators. At high level, learning techniques can provide ways to either recognize previously synthesized kernels or to model the hidden dependencies between synthesis directive costs and performances. At a lower level, speeding up RTL simulations based on data dependencies analysis can speed up one of the most time consuming steps.
EU/ESA PROJECTS ON HETEROGENEOUS COMPUTING

3.3

CHAMROUSSE

1430 - 1600

Chair: Carles Hernandez, Universitat Politècnica de València, ES

Co-Chair: Francisco J. Cazorla, BSC, ES

In the scope of this session the presented EU/ESA projects cover topics related to the control electronics and data processing architecture and functionality of the Wide Field Imager, one of two scientific instruments of the next European X-ray observatory ATHENA; task-based programming models to provide a software ecosystem for heterogeneous hardware composed of CPUs, GPUs, FPGAs and dataflow engines; and a framework to allow Big Data solutions to dynamically and transparently exploit heterogeneous hardware accelerators.

1430

ESA Athena WFI Onboard Electronics - Distributed Control and Data Processing (work in progress in the project)

Markus Plattner1, Sabine Ott1, Jintin Tran1, Christopher Mandla1, Manfred Steller2, Harald Jeszensky2, Roland Ottensamer2, Jan-Christoph Tenzer4, Thomas Schanz4, Samuel Pliego4, Konrad Skup5, Denis Tcherniak5, Chris Thomas7, Julian Thornhill7 and Sebastian Albrecht1

1Max Planck Institute for extraterrestrial Physics, DE; 2IWF - Space Research Institute, AT; 3TU Wien, AT; 4University of Tübingen, DE; 5CBK Warsaw, PL; 6Technical University of Denmark, DK; 7University of Leicester, GB

TECHNICAL SESSIONS – TUESDAY

1430

Efficient and Robust High-Level Synthesis Design Space Exploration through offline Micro-kernels Pre-characterization

Zi Wang, Jianqi Chen and Benjamin Carrión Schaefer

University of Texas at Dallas, US

1500

Prospector: Synthesizing Efficient Accelerators via Statistical Learning

Atefeh Mehrabi1, Aninda Manocha1,2, Benjamin Lee1 and Daniel Sorin1

1Duke University, US; 2Princeton University, US

1530

Tango: An Optimizing Compiler for Just-In-Time RTL Simulation

Blaise-Pascal Tine, Sudhakar Yalamanchili and Hyesoon Kim

Georgia Tech, US

IPs

IP1-10, IP1-11, IP1-12

1600

Exhibition and Coffee Break

TECHNICAL SESSIONS – TUESDAY

1500

LEGaTO: Low-Energy, Secure, and Resilient Toolset for Heterogeneous Computing

Behzad Salami1, Konstantinos Parasysi1, Adrian Cristal1, Osman Unsal1, Xavier Martorell1, Paul Carpenter1, Raul De La Cruz1, Leonardo Bautista1, Daniel Jimenez1, Carlos Alvarez1, Saber Nabavi1, Sergi Madonar1, Miquel Pericás2, Pedro Trancoso2, Mustafa Abduljabbar2, Jing Chen2, Pirah Noor Soomro2, Madhavan Manivannan2, Michal von dem Berge3, Stefan Krupop3, Frank Klawonn4, Amani Mihkalfi4, Sigrun May4, Tobias Becker5, Georgi Gaydadjiev5, Hans Salomonsson5, Devdatt Dubhashi6, Oron Port2, Yoav Etsion2, Le Quoc Do8, Christof Fetzer8, Martin Kaiser9, Nils Kuczka1, Jens Hagemeyer1, René Griessl9, Lennart Tigges9, Kevin Mika9, Arne Hüffmeier9, Marcelo Pasin10, Valerio Schiavoni10, Isabella Rocha10, Christian Göttel10 and Pascal Felber10

1BSC, ES; 2Chalmers, SE; 3Christmann Informationstechnik + Medien GmbH & Co. KG, DE; 4Helmholtz-Zentrum für Infektionsforschung GmbH, DE; 5MAXELER, GB; 6MIS, SE; 7TECHNION, IL; 8TU Dresden, DE; 9UNIBI, DE; 10University of Neuchâtel, CH

Efficient Compilation and Execution of JVM-Based Data Processing Frameworks on Heterogeneous Co-Processors

Christos Kotselidis1, Ioannis Komniosis2, Orestis Akrivopoulos3, Sebastian Bress4, Katerina Doka5, Hazeef Mohammed6, Georgios Mylonas7, Vassilis Spitakakis8, Daniel Strimpe9, Juan Fumero1, Foivos S. Zakka1, Michail Papadimitriou1, Maria Xekalaki1, Nikos Foutris1, Athanasios Stratikopoulos1, Nectarios Koziris1, Ioannis Konstantinou5, Ioannis Mytilinis6, Constantin Bitsakos5, Christos Tsalidis5, Christos Tselios5, Nikolaos Kanakis5, Clemens Lutz4, Viktor Rosenfeld4 and Volker Markl4

1University of Manchester, GB; 2Exus Ltd., US; 3Spark Works ITC Ltd., GB; 4German Research Center for Artificial Intelligence, DE; 5National TU Athens, GR; 6Kaleao Ltd., GB; 7Computer Technology Institute & Press Diophantus, GR; 8Neurocom Luxembourg, LU; 9iProov Ltd., GB

1600

Exhibition and Coffee Break

ACCELERATING NEURAL NETWORKS AND VISION WORKLOADS

STENDHAL

1430 - 1600

Chair: Leonidas Kosmidis, BSC, ES

Co-Chair: Georgios Keramidas, Aristotle University of Thessaloniki/Think Silicon S.A., GR

This session presents different solutions to accelerate emerging applications. The papers include various microarchitecture techniques as well as complete SoC and RISC-V based solutions. More fine-grained techniques are also presented like fast computations on sparse matrices. Vision applications are represented by the popular VSLAM, while various types and forms of emerging Neural Networks (such as Recurrent, Quantized, and Siamese NNs) are considered.
<table>
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<tr>
<th>Time</th>
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<tbody>
<tr>
<td>1430</td>
<td>PSB-RNN: A Processing-in-Memory Systolic Array Architecture using Block Circulant Matrices for Recurrent Neural Networks</td>
<td>Nagadastagiri Challapalle¹, Sahithi Rampalli¹, Makesh Tarun Chandran¹, Gurpreet Singh Kalsi², John (Jack) Sampson¹, Sreenivas Subramoney² and Vijaykrishnan Narayanan¹ ¹Pennsylvania State University, US; ²Intel Labs, IN</td>
</tr>
<tr>
<td>1500</td>
<td>XpulpNN: Accelerating Quantized Neural Networks on RISC-V Processors Through ISA Extensions</td>
<td>Angelo Garofalo¹, Giuseppe Tagliavini¹, Francesco Conti¹, Davide Rossi¹ and Luca Benini¹ ¹Università di Bologna, IT; ²ETH Zurich, CH</td>
</tr>
<tr>
<td>1530</td>
<td>SNA: A Siamese Network Accelerator to Exploit the Model-Level Parallelism of Hybrid Network Structure</td>
<td>Xingbin Wang, Boyan Zhao, Rui Hou and Dan Meng Chinese Academy of Sciences, CN</td>
</tr>
<tr>
<td>1545</td>
<td>HcveAcc: A High-Performance and Energy-Efficient Accelerator for Tracking Task in VSLAM System</td>
<td>Li Renwei, Wu Junning, Liu Meng, Chen Zuding, Zhou Shengang and Feng Shanggong Chinese Academy of Sciences, CN</td>
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<td>1600</td>
<td>Exhibition and Coffee Break</td>
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### 3.5 PARALLEL REAL-TIME SYSTEMS

**Chair:** Liliana Cucu-Grosjean, Inria, FR  
**Co-Chair:** Antoine Bertout, ENSMA, FR  
This session presents novel techniques to enable parallel execution in real-time systems. More precisely, the papers are solving limitations of previous DAG models, devising tool chains to ensure WCET bounds, correcting results on heterogeneous processors, and considering wireless networks with application-oriented scheduling.

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<tr>
<td>1430</td>
<td>On the Volume Calculation for Conditional DAG Tasks: Hardness and Algorithms</td>
<td>Jinghao Sun¹, Yaoyao Chi², Tianfei Xu¹, Lei Cao¹, Nan Guan², Zhishan Guo³ and Wang Yi⁴ ¹Northeastern University, CN; ²Hong Kong Polytechnic University, CN; ³University of Central Florida, US; ⁴Uppsala Universitet, SE</td>
</tr>
<tr>
<td>1500</td>
<td>WCET-aware Code Generation and Communication Optimization for Parallelizing Compilers</td>
<td>Simon Reder and Juergen Becker Karlsruhe Institute of Technology, DE</td>
</tr>
<tr>
<td>1530</td>
<td>Template schedule construction for global real-time scheduling on unrelated multiprocessor platforms</td>
<td>Antoine Bertout¹, Joel Goossens², Emmanuel Grolleau¹ and Xavier Poczekajo² ¹LIAA, Université de Poitiers, ISAE-ENSSA, FR; ²Université Libre de Bruxelles, BE</td>
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### 3.6 NOC IN THE AGE OF NEURAL NETWORK AND APPROXIMATE COMPUTING

**Chair:** Romain Lemaire, CEA, FR  
**Co-Chair:** Jean-Philippe Diguet, CNRS/ Lab-STICC, FR  
To support innovative applications, new paradigms have been introduced, such as neural network and approximate computing. This session presents different NoC-based architectures that support these computing approaches. In these advanced architectures, NoC designs are no longer only a communication infrastructure but also part of the computing system. Different mechanisms are introduced at network-level to support the application and thus enhance the performance and power efficiency. As such, new NoC-based architectures must respond to highly demanding applications such as image segmentation and classification by taking advantage of new topologies (multiple layers, 3D…) and new technologies, such as ReRAM.

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<tr>
<td>1430</td>
<td>GRAMARCH: A GPU-ReRAM based Heterogeneous Architecture for Neural Image Segmentation</td>
<td>Biresh Kumar Joardar¹, Nitthilan Kannappan Jayakodi¹, Jana Doppa¹, Partha Pratim Pande¹, Hai (Helen) Li²,³ and Krishnendu Chakrabarty² ¹Washington State University, US; ²TU Munich, DE; ³Duke University, US</td>
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<tr>
<td>1500</td>
<td>An approximate multiplane network-on-chip</td>
<td>Ling Wang¹, Xiaohang Wang² and Yadong Wang¹ ¹Harbin Institute of Technology, CN; ²South China University of Technology, CN</td>
</tr>
<tr>
<td>1530</td>
<td>Shenjing: A low power reconfigurable neuromorphic accelerator with partial-sum and spike networks-on-chip</td>
<td>Bo Wang, Jun Zhou, Weng-Fai Wong and Li-Shiuan Peh National University of Singapore, SG</td>
</tr>
<tr>
<td>1600</td>
<td>Exhibition and Coffee Break</td>
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3.7 AUGMENTED AND ASSISTED LIVING: A REALITY

BERLIOZ  1430 - 1600

Chair: Graziano Pravadelli, Università di Verona, IT
Co-Chair: Vassilis Pavlidis, Aristotle University of Thessaloniki, GR

Novel solutions for healthcare and ambient assistant living: innovative brain-computer interfaces, novel cancer prediction systems and energy-efficient ECG and wearable systems.

1430 Compressing Subject-Specific Brain-Computer Interface Models into One Model by Superposition in Hyperdimensional Space

Michael Hersche, Philipp Rupp, Luca Benini and Abbas Rahimi
ETH Zurich, CH

1500 A novel FPGA-based system for Tumor Growth Prediction

Konstantinos Malavazos¹, Maria Papadogiorgaki¹, Pavlos Malakonakis¹ and Yannis Papaefstathiou²
¹TU Crete, GR; ²Aristotle University of Thessaloniki, GR

1530 An Event-Based System for Low-Power ECG QRS Complex Detection

Silvio Zanoli¹, Tomas Teijeiro¹, Fabio Montagna² and David Atienza¹
¹EPFL, CH; ²Università di Bologna, IT

1545 Semi-Autonomous Personal Care Robots Interface driven by EEG Signals Digitization

Giovanni Mezzina and Daniela De Venuto
Politecnico di Bari, IT

IPs
IP1-18, IP1-19

1600 Exhibition and Coffee Break

3.8 SOLUTIONS FOR AI ON CHIP USING NEUROMORPHIC HARDWARE, FOR AI FROM EDGE TO CLOUD AND FOR POWER-EFFICIENCY

EXHIBITION THEATRE  1430 – 1615

Organiser: Jürgen Haase, edacentrum, DE

At DATE 2020 Exhibition Theatre leading experts provide attendees with their advice on the latest technologies in the field, covering applications as well as solutions for the design process. In this session Intel and Andes Technology will cover the implementation of AI highlighting neuromorphic hardware, RISC-V and AI from edge to cloud. Dolphin Design will show how to speed up the design of the required power-efficient SoC.

1430 AI on Chip: Perception, Learning, and Control in Neuromorphic Hardware

Yulia Sandamirskaya
Neuromorphic Computing Lab, Intel Labs, DE

Today, Artificial Intelligent systems are dominated by deep neural networks that learn to solve tasks from data. The DNNs have replaced computer vision architectures with hand-crafted features and have revolutionised data and signal processing. In order to train and run DNN architectures efficiently, specialised hardware accelerators are developed. One type of these accelerators is neuromorphic hardware, originally developed to emulate behaviour of biological neurons using electrical circuits. Modern neuromorphic devices such as Intel’s Loihi research chip directly execute spiking neuronal networks and often include plasticity— the ability of network connections to change on the fly based on local activity in the network. This hardware promises a new computing framework that goes beyond deep learning. These new computing framework features ultrafast event-based inference and one-shot learning — key capabilities to deploy DNNs in low-latency applications in dynamic environments. This talk will show how neuromorphic hardware can be used to solve robotic tasks.

AI from Edge to Cloud: Leveraging RISC-V with DSP, Vector and Custom Instructions

Charlie Su
Andes Technology Corporation, TW

In this talk, Andes Technology will present RISC-V processors for applications ranging from very compact, low power cores used in Sensors to mid-ranged cores in running protocol stacks and doing high-speed control, and number-crunching cores to process high-volume data in parallel. Those highly-configurable AndesCores™ with extensibility and modularity inherited from RISC-V allow designers to use one ISA for all of the workloads. They are also adopted by AI SoC’s with applications from edge to cloud. We will provide an overview of the RISC-V DSP extension for low-data volume workloads like Keyword Spotting and Face detection with low power. For higher data throughput applications, we will introduce the industry-first commercial RISC-V Vector Processor solution and how it can be used to speed up compute-intensive applications. Last but not least, one of RISC-V’s strength is to allow well-defined custom instruction extensions to fulfill Domain Specific Acceleration (DSA) without breaking ISA compatibility. In the end, we will also cover Andes Custom Extensions™, an automation framework to bring DSA capability to the hands of every designer instead of limiting it to just CPU experts.

PMU design in weeks, not months: the need for SPEED

Pierre Gazull
Dolphin Design, FR

Energy-efficiency has now replaced low-power as one of the biggest challenges that the semiconductor industry is facing. All vertical market segments are calling for more power-efficient applications, driven by a global need to reduce our environmental footprint and make the best use of energy sources. The emergence of smart cities, smart homes and smart buildings, enabled by billions of battery-operated IoT devices connected to data centers, will force the semiconductor industry to adopt disruptive approaches to improve the energy-efficiency of both edge and cloud devices.

When it comes to IC design, the traditional approaches for power reduction were mainly driven by Moore’s law and are now suffering from its slowdown, pushing SoC design teams to use more and more advanced SoC architecture and complex design techniques to overcome the fact that technology scaling is not
sufficient anymore. As a consequence, the SoC complexity required to demonstrate the best energy-efficiency figures results in longer design cycles, higher development costs and additional risks.

Leveraging its SPEED Platform that reduces the PMU design time from months to weeks, Dolphin Design provides a turn-key solution to speed-up and secure the design of advanced power management solutions from SoC architecture to implementation. Energy-efficiency and low power designs are part of Dolphin’s DNA since its inception. In this presentation we will present how we work hand-in-hand with our customers to simplify the design of power-efficient SoC, allowing them to focus on their core competencies and added value.

1600 Exhibition and Coffee Break

IP1 INTERACTIVE PRESENTATIONS

POSTER AREA 1600 - 1630
Interactive Presentations run simultaneously during a 30-minute slot. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session

IP1-1 DynUnlock: Unlocking Scan Chains Obfuscated using Dynamic Keys
Nimisha Limaye1 and Ozgur Sinanoglu2
1New York University, US; 2New York University Abu Dhabi, AE

IP1-2 CMOS Implementation of Switching Lattices
Ismail Cevik, Levent Aksoy and Mustafa Altun
Istanbul TU, TR

IP1-3 A Timing Uncertainty-Aware Clock Tree Topology Generation Algorithm for Single Flux Quantum Circuits
Soheil Nazar Shahasavani, Bo Zhang and Massoud Pedram
University of Southern California, US

IP1-4 Symmetry-based A/M-S BIST (SymBIST): Demonstration on a SAR ADC IP
Antonios Pavlidis1, Marie-Minerve Louerat1, Eric Faehn2, Anand Kumar3 and Haralampos-G. Stratigopoulos1
1Sorbonne Université, CNRS, LIP6, FR; 2STMicroelectronics, FR; 3STMicroelectronics, IN

IP1-5 Range Controlled Floating-Gate Transistors: A Unified Solution for Unlocking and Calibrating Analog ICs
Sai Govinda Rao Nimmalapudi, Georgios Volanis, Yichuan Lu, Angelos Antonopoulos, Andrew Marshall and Yiorgos Makris
University of Texas at Dallas, US

IP1-6 Testing Through Silicon Vias in Power Distribution Network of 3D-IC with Manufacturing Variability Cancellation
Koutaro Hachiya1 and Atsushi Kurokawa2
1Teikyo Heisei University, JP; 2Hiroasaki University, JP

IP1-7 TFAFreq: Towards a Fast Emulation of DNN Approximate Hardware Accelerators on GPU
Filip Vaverka, Vojtech Mrzak, Zdenek Vasicek and Lukas Sekanina
Brno University of Technology, CZ

IP1-8 Binary Linear ECCs Optimized for Bit Inversion in Memories with Asymmetric Error Probabilities
Valentin Gherman, Samuel Evain and Bastien Giraud
CEA, FR

IP1-9 BeLDPC: Bit Errors Aware Adaptive Rate LDPC Codes for 3D TLC NAND Flash Memory
Meng Zhang, Fei Wu, Qin Yu, Weihua Liu, Lanan Cui, Yahui Zhao and Changsheng Xie
Huazhong University of Science & Technology, CN

IP1-10 Poisoning the (Data) Well in ML-based CAD: A Case Study of Hiding Lithographic Hotspots
Kang Liu, Benjamin Tan, Ramesh Karri and Siddharth Garg
New York University, US

IP1-11 SOLOMON: An Automated Framework for Detecting Fault Attack Vulnerabilities in Hardware
Milind Srivastava1, Pavanlji Silps1, Indrani Roy1, Chester Rebeiro1, Aritra Hazra2 and Swarup Bhunia2
1IIT Madras, IN; 2IIT Kharagpur, IN; 3University of Florida, US

IP1-12 Formal Synthesis of Monitoring and Detection Systems for Secure CPS Implementations
Ipsita Koley1, Saurav Kumar Ghosh1, Dey Soumyajit1, Debdeep Mukhopadhyay1, Amogh Kashyap K N2, Sachin Kumar Singh2, Lavanay Lokesh2, Jithin Nalupurakkal2 and Nishant Sinha2
1IIT Kharagpur, IN; 2Robert Bosch Engineering and Business Solutions Private Limited, IN

IP1-13 ASCELLA: Accelerating Sparse Computation by Enabling Stream Accesses to Memory
Bahar Asgari, Ramyed Hadidi and Hyesoon Kim
Georgia Tech, US

IP1-14 Acceleration of probabilistic reasoning through custom processor architecture
Nimish Shah, Laura I. Galindez Olascoaga, Wannes Meert and Marian Verhelst
KU Leuven, BE

IP1-15 A Performance Analysis Framework for Real-Time Systems Sharing Multiple Resources
Shayan Tabatabaie Nikkah, Marc Geilen, Dip Goswami and Kees Goossens
Eindhoven University of Technology, NL

IP1-16 Scaling Up the Memory Interference Analysis for Hard Real-Time Many-Core Systems
Matthieu Schuh1, Maximilien Dupont de Dinechin2, Matthieu Moy2 and Claire Maiza2
1Verimag/ Kalray, FR; 2ENS Paris/ ENS Lyon/LIP, FR; 3ENS Lyon/ LIP, FR; 4Grenoble INP/ Verimag, FR

IP1-17 Lightweight Anonymous Routing in NoC based SoCs
Subodha Charles, Megan Logan and Prabhat Mishra
University of Florida, US

IP1-18 A Non-invasive Wearable Bioimpedance System to Wirelessly Monitor Bladder Filling
Markus Reichmuth, Simone Schuerle and Michele Magno
ETH Zurich, CH
4.1 HARDWARE-ENABLED SECURITY

**AMPHITHÉÂTRE JEAN PROUVE**  
**Chair:** Cedric Marchand, Ecole Centrale de Lyon, FR

This session covers solutions in hardware-based design to improve security. The papers in the session propose a NTT (Number Theoretic Transform) technique enabling faster polynomial multiplication, a reliable key-PUF for key generation, and a runtime circuit de-obfuscating solution. Post-Quantum cryptography and new attacks will be discussed along this session.

**1700** A Flexible and Scalable NTT Hardware: Applications from Homomorphically Encrypted Deep Learning to Post-Quantum Cryptography  
Ahmet Can Mert¹, Emre Karabulut², Erdinc Ozturk¹, Erkay Savas³, Michela Becchi² and Aydin Aysu²  
¹Sabanci University, TR; ²North Carolina State University, US

**1730** Reliable and Lightweight PUF-based Key Generation using Various Index Voting Architecture  
Jeong-Hyeon Kim¹, Ho-Jun Jo¹, Kyung-kuk Jo¹, Sunghee Cho¹, Jaejong Chung² and Joon-Sung Yang¹  
¹Sungkyunkwan University, KR; ²Incheon National University, KR

**1800** Estimating the Circuit De-obfuscation Runtime based on Graph Deep Learning  
Zhiqian Chen¹, Gaurav Kolhe², Setareh Rafatirad², Chang-Tien Lu¹, Sai Manoj Pudukotai Dinakarrao², Houman Homayouni² and Liang Zhao²  
¹Virginia Tech, US; ²George Mason University, US

**IPs**  
IP2-1, IP2-2

**1830** Exhibition Reception in Exhibition Area

4.3 EU PROJECTS ON NANOELECTRONICS WITH CMOS AND ALTERNATIVE TECHNOLOGIES

**AUTRANS**  
**Chair:** Dimitris Gizopoulos, University of Athens, GR  
**Co-Chair:** George Karakonstantis, Queen’s University Belfast, GB

This session presents the results of three European Projects in different stages of execution covering the development of a complete synthesis and optimization methodology for nano-crossbar arrays; the reliability, security, and associated EDA tools for nanoelectronic systems, and the exploitation of STT-MTJ technologies for heterogeneous function implementation.

**1700** Nano-Crossbar based Computing: Lessons Learned and Future Directions  
Mustafa Altun¹, Ismail Cevik¹, Ahmet Erten¹, Osman Eksik¹, Mircea Stan² and Csaba Moritz³  
¹Istanbul TU, TR; ²University of Virginia, US; ³University of Massachusetts Amherst, US

**1730** RESCUE: Interdependent Challenges of Reliability, Security and Quality in Nanoelectronic Systems  
Maksim Jenihhin¹, Said Hamdiou², Matteo Sonza Reorda³, Milos Krstic¹, Peter Langendoerfer⁴, Christian Sauër⁵, Anton Klotz⁵, Michael Huebner⁵, Joerg Nolte⁵, H.T. Vierhaus⁵, Georgios Selimis⁵, Dan Alexandrescu⁶, Mottaqiallah Taouil⁶, Geert-Jan Schrijen⁷, Luca Sterpone⁷, Giovanni Squillero⁷, Zoya Dyka⁷ and Jaan Raik⁴  
¹Tallinn University of Technology, EE; ²TU Delft, NL; ³Politecnico di Torino, IT; ⁴Leibniz-Institut für innovative Mikroelektronik, DE; ⁵Cadence Design Systems, DE; ⁶BTU Cottbus-Senftenberg, DE; ⁷Intrinsic-ID, NL; ⁸IROC Technologies, FR
1800  
A Universal Spintronic Technology based on Multifunctional Standardized Stack  
*Mehdi Tahoori*, Sarath Mohanachandran Nair¹, Rajendra Bishnoi², Lionel Torres³, Guillaume Partigeon⁴, Gregory DiPendina⁵ and Guillaume Prenat⁵  
¹Karlsruhe Institute of Technology, DE; ²TU Delft, NL; ³Université de Montpellier, FR; ⁴LIRMM, FR; ⁵Spintec, FR

1830  
Exhibition Reception in Exhibition Area

### 4.4 SOME RUN IT HOT, OTHERS DO NOT

**STENDHAL**  
Chair:  *Pascal Vivet*, CEA-Leti, FR  
Co-Chair:  *Daniele J. Pagliari*, Politecnico di Torino, IT

Temperature management is a must-have in modern computing systems. The session presents a set of techniques for smart cooling systems, both active and pro-active, and thermal control policies. The techniques presented are vertically applied to different components, such as computing and communication sub-systems, and use orthogonal modeling and optimization strategies, such as machine-learning.

**1700**  
A Learning-Based Thermal Simulation Framework for Emerging Two-Phase Cooling Technologies  
*Zihao Yuan*¹, *Geoffrey Vaartstra*², *Prachi Shukla*¹, *Zhengmao Lu*², *Evelyn Wang*², *Sherief Reda*³ and *Ayse Coskun*¹  
¹Boston University, US; ²Massachusetts Institute of Technology, US; ³Brown University, US

**1730**  
Lightweight Thermal Monitoring in Optical Networks-on-Chip via Router Reuse  
*Mengquan Li*¹, *Jun Zhou*² and *Weichen Liu*²  
¹Nanyang Technological University, CN; ²Nanyang Technological University, SG

**1800**  
A Spectral Approach to Scalable Vectorless Thermal Integrity Verification  
*Zhiqiang Zhao*¹ and *Zhuo Feng*²  
¹Michigan Technological University, US; ²Stevens Institute of Technology, US

**1815**  
Dynamic Thermal Management with Proactive Fan Speed Control Through Reinforcement Learning  
*Arman Iranfar*¹, *Federico Terranove*², *Gabor Csortas*¹, *Marina Zapater*¹, *William Fornaciari*² and *David Atienza*¹  
¹EFFL, CH; ²Politecnico di Milano, IT

**1830**  
Exhibition Reception in Exhibition Area

### 4.6 ARTIFICIAL INTELLIGENCE AND SECURE SYSTEMS

**AUTRANS**  
Chair:  *Annelie Heuser*, Université de Rennes, Inria, CNRS, FR  
Co-Chair:  *Ilia Polian*, University of Stuttgart, DE

In this session we will cover artificial intelligence algorithms in the context of secure systems. The presented papers cover an extension of a trusted execution environment to securely run machine learning algorithms, novel attacking strategies against logic-locking countermeasures, and an investigation of aging effects on the success rate of machine learning modelling attacks.

**1700**  
A Particle Swarm Optimization Guided Approximate Key Search Attack on Logic Locking In The Absence of Scan Access  
*Rajit Karmakar* and *Santanu Chattopadhyay*  
IIT Kharagpur, IN
4.7 FUTURE COMPUTING FABRICS: SECURITY AND DESIGN INTEGRATION

BERLIOZ 1700 – 1830

Chair: Elena Gnani, Università di Bologna, IT
Co-Chair: Gage Hills, Massachusetts Institute of Technology, US

Emerging technologies always promise to achieve computational and resource-efficiency. This session addresses various aspects of efficiency in the context of security and future computing fabrics: a unique challenge at the intersection of hardware security and machine learning, fully front-end compatible CAD frameworks to enable access to floating-gate memristive devices, and current recycling in superconducting circuits.

1700 Security Enhancement for RRAM Computing System through Obfuscating Crossbar Row Connections

Minhui Zou1, Zhenhua Zhu2, Yi Cai2, Junlong Zhou1, Chengliang Wang3 and Yu Wang2

1Nanjing University of Science and Technology, CN; 2Tsinghua University, CN; 3Chongqing University, CN

1700 Modeling a Floating-Gate Memristive Device for Computer Aided Design of Neuromorphic Computing

Loai Danial1, Vasu Gupta2, Evgeny Pikhay3, Yakov Roizin3 and Shahar Kvatinsky1

1Technion, IL; 2Technion, IN; 3TowerJazz, IL

1800 Ground plane partitioning for current recycling of superconducting circuits

Naveen Kumar Katam, Bo Zhang and Massoud Pedram

University of Southern California, US

1815 Silicon Photonic Microring Resonators: Design Optimization Under Fabrication Non-Uniformity

Asif Mirza, Febin Sunny, Sudeep Pasricha and Mahdi Nikdast

Colorado State University, US

IPs

IP2-8, IP2-9

1730 Effect of Aging on PUF Modeling Attacks based on Power Side-Channel Observations

Trevor Kroeger1, Wei Cheng2, Jean Luc Danger2, Sylvain Guilley3 and Naghmeh Karimi1

1University of Maryland Baltimore County, US; 2Télécom ParisTech, FR; 3Secure-IC, FR

1800 Offline Model Guard: Secure and Private ML on Mobile Devices

Sebastian P. Bayerl1, Tommaso Frassetto2, Patrick Jauernig2, Korbinian Riedhammer1, Ahmad-Reza Sadeghi2, Thomas Schneider3, Emmanuel Staff2 and Christian Weinert2

1TH Nürnberg, DE; 2TU Darmstadt, DE

1700 Exhibition Reception in Exhibition Area

1800 Exhibition Reception in Exhibition Area

1830 Exhibition Reception in Exhibition Area
The main benefits to choose Defacto STAR is

- NoC configuration change and RTL generation in 15 s
- No need to develop our own tools

NoC module will then be integrated at SoC level and connected to IPs delivered by Third-parties. We also use Defacto STAR tool to generate the SoC RTL and associated Testbench.

Quick decision of System In Package implementation for IoT/5G era

Iyad Rayane
Zuken, FR

The increasing complexity of system on chips (SoCs) combined with a new generation of designs that combine multiple chips in a single package (SiP) is creating new challenges in the design of IC packages, printed circuit boards (PCBs) and integrated circuits (ICs). The process typically involves three independent design processes – chip, package and PCB – carried out with point tools whose interface requires time-consuming manual processes that are error-prone and limit the potential for reuse. This challenge is being addressed by a new integrated 3D chip/package/board co-design environment that makes it possible to take quick decision of the best SiP implementation by considering the system-level impact of each design decision, especially for optimizing. The new co-design approach enables netlist management to follow up design modification including die partitioning and seamless electrical characteristic verification during the design. The end result is higher performance and improved quality for smart systems, MEMS and IoT applications.

Exhibition Reception in Exhibition Area
TECHNICAL SESSIONS – WEDNESDAY

5.3 SPECIAL SESSION: SECURE COMPOSITION OF HARDWARE SYSTEMS

AUTTRANS 0830 - 1000

Chair: Ilia Polian, University of Stuttgart, DE
Co-Chair: Francesco Regazzoni, ALaRi, CH

Today’s electronic systems consist of mixtures of programmable, reconfigurable, and application-specific hardware components, tied together by tremendously complex software. At the same time, systems are increasingly integrated such that a sub-system that was traditionally regarded “harm-less” (car’s entertainment system) finds itself tightly coupled with safety-critical sub-systems (driving assistance) and security-sensitive sub-systems such as online payment and others. Moreover, a system’s hardware components are now often directly accessible to the end users and thus vulnerable to physical attacks. The goal of this hot-topic session is to establish a common understanding of principles and techniques that can facilitate composition and integration of hardware systems and achieve security guarantees. Theoretical foundations of secure composition are currently limited to software systems, and unique security challenges arise when a real system, composed of a range of hardware components with different owners and trust assumptions, is put together. Physical and side-channel attacks add another level of complexity to the problem of secure composition. Moreover, practical hardware systems include software stacks of tremendous size and complexity, and hardware-software interaction can create new security challenges. This hot-topic session will consider secure composition both from a purely hardware-centric and from a hardware-software perspective in a more complex system. It will also target composition of countermeasures against hardware-centric attacks and against software-driven attacks on hardware. It brings together researchers and industry practitioners who deal with secure composition: security-oriented electronic design automation; secure architectures of automotive hardware-software systems; and advanced attack scenarios against complexed hardware systems.

0830 Towards Secure Composition of Integrated Circuits and Electronic Systems: On the Role of EDA
Johann Knechtel1, Elif Bilge Kavun2, Francesco Regazzoni3, Annelie Heuser4, Anupam Chattopadhyay4, Debdeep Mukhopadhyay5, Dey Soumyajit6, Yunsu Fei7, Yaacov Belenky8, Itamar Levi8, Tim Güneysu9, Patrick Schaumont10 and Ilia Polian11
1New York University Abu Dhabi, AE; 2University of Sheffield, GB; 3ALaRi, CH; 4Université de Rennes/Inria/ CNRS/ IRISA, FR; 5Nanyang Technological University, SG; 6IIT Kharagpur, IN; 7Northeastern University, US; 8Intel, IL; 9Bar-Ilan University, IL; 10Ruhr-University Bochum, DE; 11Virginia Tech, US; 12University of Stuttgart, DE

0855 Attacker Modeling on Composed Systems
Tobias Basic, Jan Müller, Pierre Schnarz and Marc Stoettinger
Continental AG, DE

0915 Pitfalls in Machine Learning-based Adversary Modeling for Hardware Systems
Fatemeh Ganji1, Sarah Amir1, Shahin Tajik1, Jean-Pierre Seifert2 and Domenic Forte1
1University of Florida, US; 2TU Berlin, DE

0935 Using Universal Composition to Design and Analyze Secure Complex Hardware Systems
Ran Canetti1, Marten van Dijk2, Hoda Maleki3, Ulrich Rührmair4 and Patrick Schaumont5
1Boston University, US; 2University of Connecticut, US; 3University of Augusta, US; 4TU Munich, DE; 5Worcester Polytechnic Institute, US

5.4 NEW FRONTIERS IN FORMAL VERIFICATION FOR HARDWARE

STENDHAL 0830 - 1000

Chair: Alessandro Cimatti, Fondazione Bruno Kessler, IT
Co-Chair: Heinz Riener, EPFL, CH

The session presents several new techniques in hardware verification. The technical papers propose methods for the formal verification of industrial arithmetic circuits and processors, and show how reinforcement learning can be used for verification of shared memory protocols. Two interactive presentations describe how to use high-level synthesis to supply security guarantees and to generate certificates when verifying multipliers.

0830 Gap-free Processor Verification by S²QED and Property Generation
Keerthikumara Devarajegowda1, Mohammad Rahmani Fadiheh2, Eshan Singh3, Clark Barrett4, Subhasish Mitra5, Wolfgang Ecker1, Dominik Stoffel6 and Wolfgang Kunz2
1Infineon Technologies, DE; 2TU Kaiserslautern, DE; 3Stanford University, US

0900 SPEAR: Hardware-based Implicit Rewriting for Square-root Verification
Atif Yasin1, Tiankai Su1, Sebastien Pillement2 and Maciej Ciesielski1
1University of Massachusetts Amherst, US; 2University of Nantes, FR

0930 A Reinforcement Learning Approach to Directed Test Generation for Shared Memory Verification
Nicolas Pfeifer, Bruno V. Zimpel, Gabriel A. G. Andrade and Luiz C. V. dos Santos
Federal University of Santa Catarina, BR

0945 Towards Formal Verification of Optimized and Industrial Multipliers
Alireza Mahzoon1, Daniel Grosse1, Christoph Scholl2 and Rolf Drechsler1,2
1University of Bremen, DE; 2DFKI, DE; 3University of Freiburg, DE

1000 Exhibition and Coffee Break

IPs
IP2-12, IP2-13
5.5 MODEL-BASED ANALYSIS AND SECURITY

BAYARD 0830 - 1000
Chair: Ylies Falcone, Université Grenoble Alpes and Inria, FR
Co-Chair: Todd Austin, University of Michigan, US
The session explores the use of state-of-the-art model-based analysis and verification techniques to secure and improve the performance of embedded systems. More specifically, it presents the use of satisfiability modulo theory, runtime monitoring, fuzzing, and model-checking to evaluate how secure is a system, prevent, and detect attacks.

0830 Is Register Transfer Level Locking Secure?
Chandan Karfa1, Ramanuj Chouksey1, Christian Pilato2, Siddharth Garg3 and Ramesh Karri2
1IIT Guwahati, IN; 2Politecnico di Milano, IT; 3New York University, US

0900 Design Space Exploration for Model-based Communication Systems
Valentina Richthammer, Marcel Rieß, Julian Bestler, Frank Slomka and Michael Gläß
University of Ulm, DE

0930 Statistical Time-based Intrusion Detection in Embedded Systems
Nadir Carreon Rascon, Allison Gilbreath and Roman Lysecky
University of Arizona, US

IPs IP2-14, IP2-15

1000 Exhibition and Coffee Break

5.6 LOGIC SYNTHESIS TOWARDS FAST, COMPACT, AND SECURE DESIGNS

LESDIGUIÈRES 0830 - 1000
Chair: Valeria Bertacco, University of Michigan, US
Co-Chair: Lukas Sekanina, Brno University of Technology, CZ
The logic synthesis family is growing. While traditional optimization goals such as area and delay are still very important in today’s design automation, new applications require improvement of aspects such as security or power consumption. This session showcases various algorithms addressing both emerging and traditional optimization goals. An algorithm is proposed for cryptographic applications which reduces the multiplicative complexity thereby making designs less vulnerable to attacks. A synthesis method converts flip-flops to latches in a clever way and saves power in this way. Approximation and bi-decomposition techniques are used in an area optimization strategy. Finally, a methodology for design minimization in advanced technology nodes is presented that takes both wire congestion and coupling effects into account.

0830 A Logic Synthesis Toolbox for Reducing the Multiplicative Complexity in Logic Networks
Eleonora Testa1, Mathias Soeken1, Heinz Riener1, Luca Amaru2 and Giovanni De Micheli1
1EPFL, CH; 2Synopsys, US

0900 Saving Power by Converting Flip-Flop to 3-Phase Latch-Based Designs
Huimei Cheng, Xi Li, Yichen Gu and Peter Beerel
University of Southern California, US

0930 Computing the full quotient in bi-decomposition by approximation
Anna Bernasconi1, Valentina Ciriani2, Jordi Cortadella3 and Tiziano Villa4
1Università di Pisa, IT; 2Università degli Studi di Milano, IT; 3Università Politecnica de Catalunya, ES; 4Università di Verona, IT

0945 MiniDelay: Multi-Strategy Timing-Aware Layer Assignment for Advanced Technology Nodes
Xinghai Zhang1, Zhen Zhuang1, Genggeng Liu1, Xing Huang2, Wen-Hao Liu3, Wenzhong Guo1 and Ting-Chi Wang2
1Fuzhou University, CN; 2National Tsing Hua University, TW; 3Cadence Design Systems, US

IPs IP2-16, IP2-17

1000 Exhibition and Coffee Break

5.7 STOCHASTIC COMPUTING

BERLIOZ 0830 - 1000
Chair: Robert Wille, Johannes Kepler University Linz, AT
Co-Chair: Shigeru Yamashita, Ritsumeikan, JP
Stochastic computing uses random bitstreams to reduce computational and area costs of a general class of Boolean operations, including arithmetic addition and multiplication. This session considers stochastic computing from a model-, accuracy-, and applications-perspective, by presenting papers that span from models of pseudo-random number generators, to accuracy analysis of stochastic circuits, to novel applications for signal processing tasks.

0830 The Hypergeometric Distribution as a More Accurate Model for Stochastic Computing
Timothy Baker and John Hayes
University of Michigan, US

0900 Accuracy Analysis for Stochastic Circuits with D-Flip Flop Insertion
Kuncai Zhong and Weikang Qian
University of Michigan-Shanghai Jiao Tong University, CN

0930 Dynamic Stochastic Computing for Digital Signal Processing Applications
Siting Liu and Jie Han
University of Alberta, CA

IPs IP2-18, IP2-19, IP2-20

1000 Exhibition and Coffee Break
One of the fastest growing areas of hardware and software design is artificial intelligence (AI)/machine learning (ML), fueled by the demand for more autonomous systems like self-driving vehicles and voice recognition for personal assistants. Many of these algorithms rely on convolutional neural networks (CNNs) to implement deep learning systems. While the concept of convolution is relatively straightforward, the application of CNNs to the ML domain has yielded dozens of different neural network approaches. These networks can be executed in software on CPUs/GPUs, the power requirements for these solutions make them impractical for most inferencing applications, the majority of which involve portable, low-power devices. To improve the power/performance, hardware teams are forming to create ML hardware acceleration blocks. However, the process of taking any one of these compute-intensive networks into hardware, especially energy-efficient hardware, is a time consuming process if the team employs a traditional RTL design flow. Consider all of these interdependent activities using a traditional flow:

- Expressing the algorithm correctly in RTL.
- Choosing the optimal bit-widths for kernel weights and local storage to meet the memory budget.
- Designing the microarchitecture to have a low enough latency to be practical for the target application, while determining how the accelerator communicates across the system bus without killing the latency the team just fought for.
- Verifying the algorithm early on and throughout the implementation process, especially in the context of the entire system.
- Optimizing for power for mobile devices.
- Getting the product to market on time. This domain is in desperate need of a productivity-boosting methodology shift away from an RTL flow.

**IP2**

**INTERACTIVE PRESENTATIONS**

**POSTER AREA**

Interactive Presentations run simultaneously during a 30-minute slot. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session.

**IP2-1**

**Sampling from Discrete Distributions in Combinational Hardware with Application to Post-Quantum Cryptography**

Michael Lyons and Kris Gaj

George Mason University, US

**IP2-2**

**On the performance of Non-Profiled Differential Deep Learning Attacks against an AES encryption algorithm protected using a Correlated Noise hiding countermeasure**

Amir Alipour¹, Athanasios Papadimitriou², Vincent Berouille¹, Ehsan Aerabi¹ and David Hely¹

¹Université Grenoble Alpes, Grenoble INP ESISAR, LCIS Laboratory, FR; 
²Université Grenoble Alpes, Grenoble INP ESISAR, ESYNOV, FR

**IP2-3**

**Fast and Accurate Performance Evaluation for RISC-V using Virtual Prototypes**

Vladimir Herdt¹, Daniel Grosse¹,² and Rolf Drechsler¹,²

¹University of Bremen, DE; ²DFKI, DE

**IP2-4**

**Automated Generation of LTL Specifications For Smart Home IoT Using Natural Language**

Shiyou Zhang¹, Juan Zhai², Lei Bu³, Mingsong Chen², Linzhang Wang¹ and Xuandong Li¹

¹Nanjing University, CN; ²East China Normal University, CN

**IP2-5**

**A Heat-Recirculation-Aware VM Placement Strategy for Data Centers**

Hao Feng¹, Yuhui Deng² and Yi Zhou³

¹Jinan University, CN; ²Chinese Academy of Sciences; Jinan University, CN; ³Columbus State University, US

**IP2-6**

**Energy Optimization in NCFET-based Processors**

Sami Salamin¹, Martin Rapp¹, Hussam Amrouch¹, Andreas Gerstlauer¹ and Joerg Henkel¹

¹Karlsruhe Institute of Technology, DE; ²University of Texas at Austin, US

**IP2-7**

**Towards a Model-based Multi-Objective Optimization Approach For Safety-Critical Real-Time Systems**

Soulimane Kamni, Yassine Ouhammou, Antoine Bertout and Emmanuel Grolleau

LIAS, Université de Poitiers, ISAE-ENSMA, FR

**IP2-8**

**Current-Mode Carry-Free Multiplier Design using a Memristor-Transistor Crossbar Architecture**

Shengqi Yu¹, Ahmed Soltan², Rishad Shafik¹, Thanasin Bunnam¹, Domenico Balsamo¹, Fei Xia¹ and Alex Yakovlev¹

¹Newcastle University, GB; ²Nile University, EG

**IP2-9**

**n-bit Data Parallel Spin Wave Logic Gate**

Abdulqader Mahmoud¹, Frederic Vanderveken², Florin Ciubotaru², Christoph Adelmann², Sorin Cotofana¹ and Said Hamdiou¹

¹TU Delft, NL; ²IMEC, BE

**IP2-10**

**High-speed analog simulation of CMOS vision chips using explicit integration techniques on many-core processors**

Gines Domenech-Asensi¹ and Tom J Kazmierski²

¹Universidad Politecnica de Cartagena, ES; ²University of Southampton, GB
IP2-11  A 100KHz-1GHz Termination-dependent Human Body Communication Channel Measurement using Miniaturized Wearable Devices
Shitij Avlani, Mayukh Nath, Shovan Maity and Shreyas Sen
Purdue University, US

IP2-12  From DRUP to PAC and Back
Daniela Kaufmann, Armin Biere and Manuel Kauers
Johannes Kepler University Linz, AT

IP2-13  Verifiable Security Templates for Hardware
William Harrison and Gerard Allwein
1Oak Ridge National Laboratory, US; 2Naval Research Laboratory, US

IP2-14  IFFSET: In-Field Fuzzing of Industrial Control Systems using System Emulation
Dimitrios Tychalas and Michail Maniatakos
1New York University, US; 2New York University Abu Dhabi, AE

IP2-15  FANNet: Formal Analysis of Noise Tolerance, Training Bias and Input Sensitivity in Neural Networks
Mahum Naseer, Mishal Fatima Minhas, Faq Khalid, Muhammad Abdullah Hanif, Osman Hasan and Muhammad Shafique
1TU Wien, AT; 2National University of Sciences and Technology, PK

IP2-16  A Scalable Mixed Synthesis Framework for Heterogeneous Networks
Max Austin, Scott Temple, Walter Lau Neto, Luca Amaru, Xifan Tang and Pierre-Emmanuel Gaillardon
1University of Utah, US; 2Synopsys, US

IP2-17  DiSCERN: Distilling Standard Cells for Emerging Reconfigurable Nanotechnologies
Shubham Rai, Michael Raitza, Siva Satyendra Sahoo and Akash Kumar
1TU Dresden, DE; 2CfAED, DE

IP2-18  A 16 × 128 Stochastic-Binary Processing Element Array for Accelerating Stochastic Dot-Product Computation Using 1-16 Bit-Stream Length
Qian Chen, Yuqi Su, Hyunjoon Kim, Taegun Yoo, Tony Tae-Hyoung Kim and Bongjin Kim
Nanyang Technological University, SG

IP2-19  Towards Exploring the Potential of Alternative Quantum Computing Architectures
Arighna Deb, Gerhard W. Dueck and Robert Wille
1Kalinga Institute of Industrial Technology, IN; 2University of New Brunswick, CA; 3Johannes Kepler University Linz, AT

IP2-20  Accelerating Quantum Approximate Optimization Algorithm using Machine Learning
Mahabubul Alam, Abdullah Ash-Saki and Swaroop Ghosh
Pennsylvania State University, US

6.1  SPECIAL DAY ON "EMBEDDED AI": EMERGING DEVICES, CIRCUITS AND SYSTEMS
AMPHITHEÂTRE JEAN PROUVE  1100 - 1230
Chair: Carlo Reita, CEA, FR
Co-Chair: Bernabe Linares-Barranco, CSIC, ES
This session focuses on the advantages and use of novel emerging nanotechnology devices and their use in designing circuits and systems for embedded AI hardware solutions.

In-Memory Resistive RAM Implementation of Binarized Neural Networks for Medical Applications
Bogdan Penkovsky, Marc Bocquet, Tifenn Hirtzlin, Jacques-Olivier Klein, Etienne Nowak, Elisa Vianello, Jean-Michel Portal and Damien Querlioz
1Université Paris-Saclay, FR; 2Aix-Marseille University, FR; 3CEA-Leti, FR; 4Université Paris-Sud, FR

Mixed-signal vector-by-matrix multiplier circuits based on 3D-NAND memories for neuromorphic computing
Mohammad Bavandpour, Shubham Sahay, Mohammad Mahmoodi and Dmitri Strukov
University of California, Santa Barbara, US

Modular RRAM based in-memory computing design for embedded AI
Xinxin Wang, Qiwen Wang, Mohammed A. Zidan, Fan-Hsuan Meng, John Moon and Wei Lu
University of Michigan, US

Neuromorphic computing: toward dynamical data processing
Fabian Alibart
CNRS, Lille, FR

1100
Exhibition and Lunch Break

6.2  SECURE AND FAST MEMORY AND STORAGE
CHAMROUSSE  1100 - 1230
Chair: Hao Yu, SUSTech, CN
Co-Chair: Chengmo Yang, University of Delaware, US
As memories become persistent, the design of traditional data structures such as trees and hash tables as well as filesystems should be revisited to cope with the challenges brought by new memory devices. In this context, the main focus of this session is on how to improve performance, security, and energy-efficiency of memory and storage. The specific techniques range from the designs of integrity trees and hash tables, the management of superpages in filesystems, data prefetch in solid state drives (SSDs), as well as energy-efficient carbon-nanotube cache design.

An Efficient Persistency and Recovery Mechanism for SGX-style Integrity Tree in Secure NVM
Mengya Lei, Fang Wang, Dan Feng, Fan Li and Jie Xu
Huazhong University of Science & Technology, CN

1100
6.3 SPECIAL SESSION: MODERN LOGIC REASONING METHODS FOR FUNCTIONAL ECO
AUTRANS 1100 - 1230

Chair: Patrick Vuillod, Synopsys, US
Co-Chair: Christoph Scholl, Albert-Ludwigs-University Freiburg, DE

Functional Engineering Change Order (ECO) is the problem of incrementally updating an existing logic network after a (possibly late) change in the design specification. The problem requires (i) to identify a small portion of the network’s logic to be changed and (ii) to automatically synthesize a patch to replace this portion and rectify the network’s functional behavior. ECOs can be solved using the logical framework of quantified Boolean formulæ (QBF), where a logic query asks for the existence of a set of nodes and values at those nodes to rectify the logic network’s output functions. The global nature of the problem, however, challenges scalability. Any internal node in the logic network is a potential location for rectification and any node in the logic network may be used to simplify the synthesized patch. Furthermore, off-the-self QBF algorithms do not allow a formulation of resource costs for reusing existing logic.

1100 Engineering Change Order for Combinational and Sequential Design Rectification
Jie-Hong Roland Jiang1, Victor Kravets2 and Nian-Ze Lee1
1National Taiwan University, TW; 2IBM, US

1120 Exact DAG-Aware Rewriting
Heinz Rie1, Alan Mishchenko2 and Mathias Soeken1
1EPFL, CH; 2University of California, Berkeley, US

1140 Learning to Automate the Design Updates from Observed Engineering Changes in the Chip Development Cycle
Victor Kravets1, Jie-Hong Roland Jiang2 and Heinz Rie1
1IBM, US; 2National Taiwan University, TW; 3EPFL, CH

6.4 MICROARCHITECTURE TO THE RESCUE OF MEMORY STENDHAL 1100 - 1230

Chair: Olivier Sentieys, INRIA, FR
Co-Chair: Jeronimo Castrillon, TU Dresden, DE

This session discusses micro-architectural innovations across three different memory technologies, namely, caches, 3D-stacked DRAM and non-volatile. This includes exploiting several aspects of redundancy to maximize cache utilization through compression, as well as multicast in 3D-stacked high-speed memories for graph analytics, and a microarchitecture solution to unify persistency and encryption in non-volatile memories.

1100 Efficient Hardware-Assisted Crash Consistency in Encrypted Persistent Memory
Zhan Zhang1, Jianhui Yue2, Xiaofei Liao1 and Hai Jin1
1Huazhong University of Science & Technology, CN; 2Michigan Technological University, US

1130 2DCC: Cache Compression in Two Dimensions
Amin Ghasemazar1, Mohammad Ewais2, Prashant Nair1 and Mieszko Lis1
1University of British Columbia, CA; 2UofT, CA

1200 GraphVine: Exploiting Multicast for Scalable Graph Analytics
Leul Belayneh and Valeria Bertacco
University of Michigan, US

IPs
IP3-2

1230 Exhibition and Lunch Break
6.5  EFFICIENT DATA REPRESENTATIONS IN NEURAL NETWORKS

BAYWARD 1100 - 1230

Chair:  Brandon Reagen, Facebook and New York University, US
Co-Chair:  Sebastian Steinhorst, TU Munich, DE

The large processing requirements of ML models strain the capabilities of low-power embedded systems. Addressing this challenge, the first presentation proposes a robust co-design to leverage stochastic computing for highly accurate and efficient inference. Next, a structural optimization is proposed to counter faults at low voltage levels. Then, authors present a method for sharing results in binarized CNNs to reduce computation. The session will conclude with a talk implementing binary networks on mobile GPUs.

1100  ACOUSTIC: Accelerating Convolutional Neural Networks through Or-Unipolar Skipped Stochastic Computing

Wojciech Romaszkan, Tianmu Li, Tristan Melton, Sudhakar Pamarti and Puneet Gupta
University of California, Los Angeles, US

1130  Accuracy Tolerant Neural Networks Under Aggressive Power Optimization

Xiang-Xiu Wu1, Yi-Wen Hung1, Yung-Chih Chen2 and Shih-Chieh Chang1
1National Tsing Hua University, TW; 2Yuan Ze University, TW

1200  A Convolutional Result Sharing Approach for Binarized Neural Network Inference

Ya-Chun Chang1, Chia-Chun Lin1, Yi-Ting Lin1, Yung-Chih Chen2 and Chun-Yao Wang1
1National Tsing Hua University, TW; 2Yuan Ze University, TW

1215  PhoneBit: Efficient GPU-Accelerated Binary Neural Network Inference Engine for Mobile Phones

Gang Chen1, Shengyu He2, Haitao Meng2 and Kai Huang1
1Sun Yat-sen University, CN; 2Northeastern University, CN

1230  Exhibition and Lunch Break

6.6  FROM DFT TO YIELD OPTIMIZATION

LESDIGUIÈRES 1100 - 1230

Chair:  Maria Michael, University of Cyprus, CY
Co-Chair:  Ernesto Sanchez, Politecnico di Torino, IT

The session presents a variety of semiconductor test techniques, including a new design-for-testability scheme for FinFET SRAMs, a method to increase yield based on error-metric-independent signature analysis, and a synthesis method for fault-tolerant reconfigurable scan networks.

1100  A DFT Scheme to Improve Coverage of Hard-to-Detect Faults in FinFET SRAMs

Guilherme Cardoso Medeiros1, Cemil Cem Gürsoy2, Moritz Fieback1, Lizhou Wu1, Maksim Jenihhin2, Mottaqiallah Taouil3 and Said Hamdioui1
1TU Delft, NL; 2Tallinn University of Technology, EE

1130  Synthesis of Fault-Tolerant Reconfigurable Scan Networks

Sebastian Brandhofer, Michael Kochte and Hans-Joachim Wunderlich
University of Stuttgart, DE

1200  Using Programmable Delay Monitors for Wear-Out and Early Life Failure Prediction

Chang Liu1,2, Eric Schneider1 and Hans-Joachim Wunderlich1
1University of Stuttgart, DE; 2Altran Deutschland, DE

1215  Maximizing Yield for Approximate Integrated Circuits

Marcello Traiola1,5, Arnaud Virazel1, Patrick Girard2, Mario Barbareschi3 and Alberto Bosio4
1LIRMM, FR; 2LIRMM/ CNRS, FR; 3Università di Napoli Federico II, IT; 4Lyon Institute of Nanotechnology, FR; 5Université de Montpellier, FR

1230  Exhibition and Lunch Break

6.7  SAFETY AND EFFICIENCY FOR SMART AUTOMOTIVE AND ENERGY SYSTEMS

BERLIOZ 1100 - 1230

Chair:  Selma Saidi, TU Dortmund, DE
Co-Chair:  Donghwa Shin, Soongsil University, KR

This session presents four papers dealing with various aspects of smart automotive and energy systems, including safety and efficiency of photovoltaic panels, deterministic execution behavior of adaptive automotive applications, efficient implementation of fail-operative automated vehicles, and efficient resource usage in networked automotive systems.

1100  A Diode-Aware Model of PV Modules from Datasheet Specifications

Sara Vinco, Yukai Chen, Enrico Macii and Massimo Poncino
Politecnico di Torino, IT

1130  Achieving Determinism in Adaptive AUTOSAR

Christian Menard1, Andres Goens1, Marten Lohstroh2 and Jeronimo Castrillon1
1TU Dresden, DE; 2University of California, Berkeley, US

1200  A Fail-safe Architecture for Automated Driving

Sebastian vom Dorff1, Bert Böddeker2, Maximilian Kneissl1 and Martin Fränzle3
1DENSO Automotive Deutschland GmbH, DE; 2Autonomous Intelligent Driving GmbH, DE; 3Carl von Ossietzky University Oldenburg, DE

1215  Priority-Preserving Optimization of Status Quo ID-Assignments in Controller Area Network

Sebastian Schwitalla, Lea Schönberger and Jian-Jia Chen
TU Dortmund, DE

1230  Exhibition and Lunch Break
6.8 SOLUTIONS FOR EDA DESIGN ENVIRONMENTS
EXHIBITION THEATRE 1100 – 1230

Organiser: Jürgen Haase, edacentrum, DE
At DATE 2020 Exhibition Theatre leading experts provide attendees with their advice on the latest technologies in the field, covering applications as well as solutions for the design process. In this session Altair and SEMI/ESDA will cover design environments and IP enabling for different levels of abstraction and multi-physics simulations, as well as the Heterogeneous Integration Roadmap (HIR) for connecting design, manufacturing and assembly.

1100 Future Vision of Altair for EDA Applications
Philippe le Marrec
Altair, FR
Today the design of EDA applications are not only focused on hardware/software parts. In many cases as in mechatronic, powertrain and control systems, the environment has to be used with the design itself at different level of abstraction. Altair is providing environments which now help users to interact with dedicated solvers and to handle multi-physics simulations.

1120 Saving Serious Money with License First Scheduling
Stuart Taylor
Altair, US
Often seen as a minor detail in job scheduling, we present an alternative view where we treat software licenses as the primary consideration in job dispatch. Through some innovative techniques we will show how license utilization can be doubled with real world examples.

1145 Connecting Design, Manufacturing and Assembly in the Moore’s Law 2.0 Era
Paul Cohen
SEMI/ESDA, US
As device scaling predicted by Moore’s Law becomes more difficult and costly, designers are looking towards new solutions to deliver increasing system level functionality and performance along with lower power and cost. The International Technology Roadmap for Semiconductors (ITRS) served as a designer’s guide to upcoming technologies for many years until it’s retirement in 2016. The Heterogeneous Integration Roadmap (HIR) provides a new guideline for system level integration for the coming decades. This includes new technologies which will have an impact on the tradeoffs facing designers. In addition, the increasing use of silicon in products and applications with long lifetimes and critical safety requirements suggests that long term process effects can no longer be safely ignored. All of this requires increased communication amongst all aspects of system design, manufacture, and assembly as we move towards Moore 2.0.

1230 Exhibition and Lunch Break
7.2 RECONFIGURABLE SYSTEMS AND ARCHITECTURES
CHAMROUSSE

1430 - 1600

Chair: Christian Pilato, Politecnico di Milano, IT
Co-Chair: Philippe Coussy, Université Bretagne Sud/ Lab-STICC, FR

Reconfigurable technologies are evolving at the device, architecture, and system levels, from embedded computation to server-based accelerator integration. In this session we explore ideas at these levels, discussing architectural features for power optimisation of CGRAs, a framework for integrating FPGA accelerators in serverless environments, and placement strategies on alternative FPGA device technologies.

1430

A Framework for Adding Low-Overhead, Fine-Grained Power Domains to CGRAs
Ankita Nayak, Keyi Zhang, Raj Setaluri, Alex Carsello, Makai Mann, Stephen Richardson, Rick Bahr, Pat Hanrahan, Mark Horowitz and Priyanka Raina
Stanford University, US

1500

BlastFunction: an FPGA-as-a-Service system for Accelerated Serverless Computing
Marco Bacis, Rolando Brondolin and Marco D. Santambrogio
Politecnico di Milano, IT

1530

Energy-aware Placement for SRAM-NVM Hybrid FPGAs
Seongsik Park, Jongwan Kim and Sungroh Yoon
Seoul National University, KR

1600

Exhibition and Coffee Break

7.3 SPECIAL SESSION: REALIZING QUANTUM ALGORITHMS ON REAL QUANTUM COMPUTING DEVICES
AUTRANS

1430 - 1600

Chair: Eduard Alarcon, Universitat Politècnica de Catalunya, ES
Co-Chair: Swaroop Ghosh, Pennsylvania State University, US

Quantum computing is currently moving from an academic idea to a practical reality. Quantum computing in the cloud is already available and allows users from all over the world to develop and execute real quantum algorithms. However, companies which are heavily investing in this new technology such as Google, IBM, Rigetti, and Intel follow different technological approaches. This led to a situation where we have substantially different quantum computing devices available thus far. Because of that, various methods for realizing the intended quantum functionality to a respectively given quantum computing device are available. This special session provides an introduction and overview into this domain and comprehensively describes corresponding methods (also referred to as compilers, mappers, synthesizers, or routers). By this, attendees will be provided with a detailed understanding on how to use quantum computers in general and dedicated quantum computing devices in particular.

1430

Running Quantum Algorithms on Resource-Constrained Quantum Devices
Carmen G. Almudever
TU Delft, NL

1500

Realizing Quantum Circuits on IBM Q Devices
Robert Wille
Johannes Kepler University Linz, AT

1530

Every Device is (almost) Equal Before the Compiler
Gian Giacomo Guerreschi
Intel Corporation, US

1600

Exhibition and Coffee Break

7.4 SIMULATION AND VERIFICATION: WHERE REAL ISSUES MEET SCIENTIFIC INNOVATION
STENDHAL

1430 - 1600

Chair: Avi Ziv, IBM, IL
Co-Chair: Graziano Pravadelli, Università di Verona, IT

This session presents recent concerns and innovative solutions in verification and simulation, covering topics ranging from partial verification to lazy event prediction, till signal name disambiguation. They tackle these challenges by reducing complexity, exploiting GPUs, and using similarity-learning techniques.

1430

Verification Runtime Analysis: Get the Most Out of Partial Verification
Martin Ring1, Fritjof Bornbebusch1, Christoph Lüth1,2, Robert Wille2 and Rolf Drechsler1,2
1DFKI, DE; 2University of Bremen, DE; 3Johannes Kepler University Linz, AT

1500

GPU-accelerated Time Simulation of Systems with Adaptive Voltage and Frequency Scaling
Eric Schneider and Hans-Joachim Wunderlich
University of Stuttgart, DE

1530

Lazy Event Prediction using Defining Trees and Schedule Bypass for Out-of-Order PDES
Daniel Mendoza, Zhongqi Cheng, Emad Arasteh and Rainer Doemer
University of California, Irvine, US

1545

Embedding Hierarchical Signal to Siamese Network for Fast Name Rectification
Yi-An Chen1, Gung-Yu Pan2, Che-Hua Shih2, Yen-Chin Liao1, Chia-Chih Yen2 and Hsie-Chia Chang1
1National Chiao Tung University, TW; 2Synopsys, TW

1600

Exhibition and Coffee Break
7.5 TECHNICAL SESSIONS – WEDNESDAY

**RUNTIME SUPPORT FOR MULTI/MANY CORES**

**BAYARD** 1430 - 1600

**Chair:** Sara Vinco, Politecnico di Torino, IT  
**Co-Chair:** Jeronimo Castrillon, TU Dresden, DE

In the era of heterogenous embedded systems, the diverse nature of computing elements pushes more than ever the need for smart runtime systems to be able to deal with resource management, multi-application mapping, task parallelism, and non-functional constraints. This session tackles these issues with solutions that span from resource-aware software architectures to novel runtime systems optimizing memory and energy consumption.

1430 **Resource-Aware MapReduce Runtime for Multi/Many-core Architectures**

Konstantinos Iliakis, Sotirios Xydis and Dimitrios Soudris  
National TU Athens, GR

1500 **Towards a Qualifiable OpenMP Framework for Embedded Systems**

Adrián Munera Sánchez, Sara Royuela and Eduardo Quiñones  
BSC, ES

**IPs**  
**IP3-11**

1600 Exhibition and Coffee Break

7.6 TECHNICAL SESSIONS – WEDNESDAY

**ATTACKS ON HARDWARE ARCHITECTURES**

**LESDIGUIÈRES** 1430 - 1600

**Chair:** Johanna Sepúlveda, Airbus Defence and Space, DE  
**Co-Chair:** Jean-Luc Danger, Telecom ParisTech, FR

Hardware architectures are under the continuous threat of all types of attacks. This session covers attacks based on side-channel leakage and the exploitation of vulnerabilities at the micro-architectural and circuit level.

1430 **Sweeping for Leakage in Masked Circuit Layouts**

Danilo Šijačić1,2, Josep Balasch1 and Ingrid Verbauwhede1  
1KU Leuven, BE; 2IMEC, BE

1500 **Increased reproducibility and comparability of data leak evaluations using ExOT**

Philipp Miedl, Bruno Klopott and Lothar Thiele  
ETH Zurich, CH

1515 **GhostBusters: Mitigating Spectre Attacks on a DBT-Based Processor**

Simon Rokicki  
IRISA, FR

1530 **Dynamic Faults based Hardware Trojan Design in STT-MRAM**

Sarah Mohanachandran Nair1, Rajendra Bishnoi2, Arunkumar Vijayan1 and Mehdi Tahoori1  
1Karlsruhe Institute of Technology, DE; 2TU Delft, NL

**IPs**  
**IP3-12**  
**IP3-13**, **IP3-14**

1600 Exhibition and Coffee Break

7.7 TECHNICAL SESSIONS – WEDNESDAY

**SELF-ADAPTIVE AND LEARNING SYSTEMS**

**BERLIOZ** 1430 - 1600

**Chair:** Gilles Sassatelli, Université de Montpellier, FR  
**Co-Chair:** Rishad Shafik, University of Newcastle, GB

Recent advances in machine learning have pushed the boundaries of what is possible in self-adaptive and learning systems. This session pushes the state of art in runtime power and performance trade-offs for deep neural networks and self-optimizing embedded systems.

1430 **AnytimeNet: Controlling Time-Quality Tradeoffs in Deep Neural Network Architectures**

Jung-Eun Kim1, Richard Bradford2 and Zhong Shao1  
1Yale University, US; 2Collins Aerospace, US

1500 **AntiDote: Attention-based Dynamic Optimization for Neural Network Runtime Efficiency**

Fuxun Yu1, Chenchen Liu2, Di Wang3, Yanzhi Wang4 and Xiang Chen1  
1George Mason University, US; 2University of Maryland, Baltimore County, US; 3Microsoft, US; 4Northeastern University, US

1530 **Using Learning Classifier Systems for the DSE of Adaptive Embedded Systems**

Fedor Smirnov, Behnaz Pourmohseni and Jürgen Teich  
Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

**IPs**  
**IP3-13**, **IP3-14**

1600 Exhibition and Coffee Break

7.8 TECHNICAL SESSIONS – WEDNESDAY

**SYSTEMC-BASED VIRTUAL PROTOTYPING: FROM SOC MODELING TO THE DIGITAL TWIN REVOLUTION**

**EXHIBITION THEATRE** 1430 – 1600

**Organiser:** Laurent Maillet-Contoz, STMicroelectronics, FR

SystemC-based virtual prototyping has been adopted and deployed for several years in the semiconductor industry, to implement the shift-left paradigm. While interest has been long focused on SoC modeling, the trends are now to extend the modeling activities to the next level, as part of the digital twin revolution. In this session, the multiple benefits of this approach are discussed, as well as the upcoming challenges, both from an industrial and an academic perspective.

1545 **Oracle-based Logic Locking Attacks: Protect the Oracle Not Only the Netlist**

Emmanouil Kalligeros, Nikolaos Karousos and Irene Karybali  
University of the Aegean, GR

**IPs**  
**IP3-12**

1600 Exhibition and Coffee Break
**TECHNICAL SESSIONS – WEDNESDAY**

**1430** Virtual Twins: Modeling trends and challenges ahead  
Laurent Maillet-Contoz  
STMicroelectronics, FR

**1500** The TLM methodology: a swiss knife for studying HW/SW interactions and a gold mine for research topics  
Florenc Maraninchi  
Verimag, Université Grenoble Alpes, CNRS, Grenoble INP Institute of Engineering, FR

**1530** SystemC-based simulation of industrial manufacturing control systems  
Frank Oppenheimer  
OFFIS - Institute for Information Technology, DE

**1600** Exhibition and Coffee Break

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**IP 3** INTERACTIVE PRESENTATIONS

**POSTER AREA 1600 - 1630**  
Interactive Presentations run simultaneously during a 30-minute slot. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session

**IP3-1 CNT-Cache: an Energy-efficient Carbon Nanotube Cache with Adaptive Encoding**  
Dawen Xu¹, Kexin Chu¹, Cheng Liu², Ying Wang², Lei Zhang² and Huawei Li²  
¹School of Electronic Science & Applied Physics Hefei University of Technology Anhui, CN; ²Chinese Academy of Sciences, CN

**IP3-2 Enhancing Multithreaded Performance of Asymmetric Multicores with SIMD Offloading**  
Jeckson Dellagostin Souza¹, Madhavan Manivannan², Miquel Pericas² and Antonio Carlos Schneider Beck¹  
¹Universidade Federal do Rio Grande do Sul, BR; ²Chalmers, SE

**IP3-3 Hardware Acceleration of CNN with One-Hot Quantization of Weights and Activations**  
Gang Li, Peisong Wang, Zejian Liu, Cong Leng and Jian Cheng  
Chinese Academy of Sciences, CN

**IP3-4 BNNsplit: Binarized Neural Networks for embedded distributed FPGA-based computing systems**  
Giorgia Fiscaletti, Marco Speziali, Luca Stornaiuolo, Marco D. Santambrogio and Donatella Sciuto  
Politecnico di Milano, IT

**IP3-5 L2L: A Highly Accurate Log₂ Lead Quantization of Pre-trained Neural Networks**  
Salim Ullah¹, Siddharth Gupta², Kapil Ahuja², Aruna Tiwari² and Akash Kumar¹  
¹TU Dresden, DE; ²IIT Indore, IN

**IP3-6 Fault Diagnosis of Via-Switch Crossbar in Non-volatile FPGA**  
Ryutarô Doi¹, Xu Bai², Toshitsugu Sakamoto² and Masanori Hashimoto¹  
¹Osaka University, JP; ²NEC Corporation, JP

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**8.1 SPECIAL DAY ON “EMBEDDED AI”: NEUROMORPHIC CHIPS AND SYSTEMS**

**AMPHITHÉÂTRE JEAN PROUVE 1700 - 1830**

Chair: Wei Lu, University of Michigan, US  
Co-Chair: Bernabe Linares-Barranco, CSIC, ES

Within the global field of AI, there is a subfield that focuses on exploiting neuroscience knowledge for artificial intelligent hardware systems. This is the neuromorphic engineering field. This session presents some examples of AI research focusing on this AI subfield.

**1700** SpiNNaker2: A Platform for Bio-Inspired Artificial Intelligence and Brain Simulation  
Bernhard Vogginner, Christian Mayr, Sebastian Höppner, Johannes Partzsch and Steve Furber  
TU Dresden, DE
An On-Chip Learning Accelerator for Spiking Neural Networks using STT-RAM Crossbar Arrays
Shruti R. Kulkarni, Shihui Yin, Jae-sun Seo and Bipin Rajendran
New Jersey Institute of Technology, US

Overcoming Challenges for Achieving High in-situ Training Accuracy with Emerging Memories
Shanshi Huang, Xiaoyu Sun, Xiaochen Peng, Hongwu Jiang and Shimeng Yu
Georgia Tech, US

DATE Party – Networking Event
supported by HiSilicon

WE ARE ALL HACKERS: DESIGN AND DETECTION OF SECURITY ATTACKS
CHAMROUSSE 1700 - 1830
Chair: Francesco Regazzoni, ALaRI, CH
Co-Chair: Daniel Grosse, University of Bremen, DE
This session deals with hardware trojans and vulnerabilities, proposing detection techniques and design paradigms to model attacks. It describes attacks by leveraging the exclusive characteristics of microfluidic devices and malicious usage of energy management. As for defenses, an automated test generation approach for hardware trojan detection using delay-based side-channel analysis is also presented.

Automated Test Generation for Trojan Detection using Delay-based Side Channel Analysis
Yangdi Lyu and Prabhat Mishra
University of Florida, US

Microfluidic Trojan Design in Flow-based Biochips
Shayan Mohammed1, Sukanta Bhattacharjee2, Yong-Ak Song3, Krishnendu Chakrabarty4 and Ramesh Karri1
1New York University, US; 2IIT Guwahati, IN; 3New York University Abu Dhabi, AE; 4Duke University, US

Towards Malicious Exploitation of Energy Management Mechanisms
Safouane Noubir, Maria Mendez Real and Sebastien Pillement
École Polytechnique de l’Université de Nantes, FR
IPs IP4-1, IP4-2

DATE Party – Networking Event
supported by HiSilicon

OPTIMIZING SYSTEM-LEVEL DESIGN FOR MACHINE LEARNING
AUTRANS 1700 - 1830
Chair: Luciano Lavagno, Politecnico di Torino, IT
Co-Chair: Yuko Hara-Azumi, Tokyo Institute of Technology, JP
In the last years, the use of ML techniques, as deep neural networks, have become a trend in system-level design, either to help the flow finding promising solutions or to deploy ML-based applications. This session presents various approaches to optimize several aspects of system-level design, like the mapping of applications on heterogeneous platforms, the inference of CNNs or the file-system usage.

ESP4ML: Platform-Based Design of Systems-on-Chip for Embedded Machine Learning
Davide Giri, Kuan-Lin Chiu, Giuseppe Di Guglielmo, Paolo Mantovani and Luca Carloni
Columbia University, US

Probabilistic Sequential Multi-Objective Optimization of Convolutional Neural Networks
Zixuan Yin, Warren Gross and Brett Meyer
McGill University, CA

ARS: Reducing F2FS Fragmentation for Smartphones using Decision Trees
Lihua Yang, Fang Wang, Zhipeng Tan, Dan Feng, Jiaxing Qian and Shiyun Tu
Huazhong University of Science & Technology, CN
IPs IP4-3, IP4-4

DATE Party – Networking Event
supported by HiSilicon

ARCHITECTURAL AND CIRCUIT TECHNIQUES TOWARD ENERGY-EFFICIENT COMPUTING
STENDHAL 1700 - 1830
Chair: Sara Vinco, Politecnico di Torino, IT
Co-Chair: Davide Rossi, Università di Bologna, IT
The session discusses low-power design techniques at the architectural as well as the circuit level. The presented works span from new solutions for conventional computing, such as ultra-low power tunable precision architectures and speculative SRAM arrays, to emerging paradigms, like spiking neural networks and stochastic computing.

TRANSPIRE: An energy-efficient TRANSprecision floating-point Programmable architecture
Rohit Prasad1,3,4, Satyajit Das2, Kevin Martin1, Giuseppe Tagliavini1, Philippe Coussy1, Luca Benini2 and Davide Rossi3
1Università Bretagne Sud, FR; 2IIT Palakkad, IN; 3Università di Bologna, IT; 4Università Bretagne Sud/ Lab-STICC, FR

Modeling and Designing of a PVT Auto-tracking Timingspeculative SRAM
Shan Shen, Tianxiang Shao, Ming Ling, Jun Yang and Longxing Shi
Southeast University, CN
TECHNICAL SESSIONS – WEDNESDAY

1800 Solving Constraint Satisfaction Problems Using the Loihi Spiking Neuromorphic Processor
Chris Yakopcic¹, Nayim Rahman¹, Tanvir Atahary¹, Tarek M. Taha¹ and Scott Douglass²
¹University of Dayton, US; ²Air Force Research Laboratory, US

1815 Accurate Power Density Map Estimation for Commercial Multi-Core Microprocessors
Jinwei Zhang, Sheriff Sadiqbatcha, Wentian Jin and Sheldon Tan
University of California, Riverside, US

8.6 MICROARCHITECTURE-LEVEL RELIABILITY ANALYSIS AND PROTECTION

1700 - 1830

Chair: Michail Maniatakos, New York University Abu Dhabi, AE

Co-Chair: Alessandro Savino, Politecnico di Torino, IT

Reliability analysis and protection at the microarchitecture level is of paramount importance to speed-up the design face of any computing system. On the analysis side, this session starts presenting a reverse-order ACE (Architecturally Correct Execution) analysis that is more accurate than original ACE proposals, then moving to an instruction level analysis based on a genetic-algorithm able to improve program resiliency to errors. Finally, on the protection side, the session presents a low-cost ECC plus approximation mechanism for GPU register files.

rACE: Reverse-Order Processor Reliability Analysis
Athanassios Chatzidimitriou and Dimitris Gizopoulos
University of Athens, GR

1730 DEFCON: Generating and Detecting Failure-prone Instruction Sequences via Stochastic Search
Ioannis Tsiokanos¹, Lev Mukhanov¹, Giorgis Georgakoudis², Dimitrios S. Nikolopoulos³ and Georgios Karakonstantis¹
¹Queen’s University Belfast, GB; ²Lawrence Livermore National Laboratory, US; ³Virginia Tech, US

1800 LAD-ECC: Energy-Efficient ECC Mechanism for GPGPUs Register File
Xiaohui Wei, Hengshnan Yue and Jingweijia Tan
Jilin University, CN

8.5 CNN DATAFLOW OPTIMIZATIONS

8.7 PHYSICAL DESIGN AND ANALYSIS

BAYARD 1700 - 1830

Chair: Mario Casu, Politecnico di Torino, IT

Co-Chair: Wanni Chang, University of York, GB

This session focuses on efficient dataflow approaches for reducing CNN runtime on embedded hardware platforms. The papers to be presented demonstrate techniques for enhancing parallelism to improve performance of CNNs, leverage output prediction to reduce the runtime for time-critical embedded applications during inference, and presents a Keras-based DNN framework for real-time cyber physical systems.

1700 Analysis and Solution of CNN Accuracy Reduction over Channel Loop Tiling
Yesung Kang¹, Yoonho Park¹, Sunghoon Kim¹, Eunjoo Kwon¹, Taeho Lim², Mingyu Woo³, Sangyun Oh⁴ and Seokhyeong Kang¹
¹Pohang University of Science and Technology, KR; ²SK Hynix, KR; ³University of California, San Diego, US; ⁴Ulsan National Institute of Science and Technology, KR

1730 DCCNN: Computational Flow Redefinition for Efficient CNN Inference through Model Structural Decoupling
Fuxun Yu¹, Zhiwei Qin¹, Di Wang², Ping Xu¹, Chenchen Liu³, Zhi Tian¹ and Xiang Chen¹
¹George Mason University, US; ²Microsoft, US; ³University of Maryland, Baltimore County, US

1800 ABC: Abstract prediction Before Concreteness
Jung-Eun Kim¹, Richard Bradford², Man-Ki Yoon¹ and Zhong Shao¹
¹Yale University, US; ²Collins Aerospace, US

1815 A compositional approach using Keras for neural networks in real-time systems
Xin Yang, Partha Roop, Hammond Pearce and Jin Woo Ro
University of Auckland, NZ

1900 DATE Party – Networking Event
supported by HiSilicon

> SEE PAGE 009

IPs
IP4-5, IP4-6

IPs
IP4-9

IPs
IP4-7, IP4-8

86 87
DATE 2020
SPEAKERS | PRESENTING AUTHORS ARE HIGHLIGHTED
**TECHNICAL SESSIONS – WEDNESDAY**

**1730**  
Towards Serial-Equivalent Multi-Core Parallel Routing for FPGAs  
**Minghua Shen** and Nong Xiao  
Sun Yat-sen University, CN

**1800**  
Self-Aligned Double-Patterning Aware Legalization  
**Hua Xiang**¹, Gi-Joon Nam¹, Gustavo Tellez², Shyam Ramji² and Xiaoqing Xu³  
¹IBM Research, US; ²IBM Thomas J. Watson Research Center, US; ³University of Texas at Austin, US

**1815**  
Explainable DRC Hotspot Prediction with Random Forest and SHAP Tree Explainer  
**Wei Zeng**¹, Azadeh Davoodi¹ and Rasit Onur Topaloglu²  
¹University of Wisconsin-Madison, US; ²IBM, US

**IPs**  
IP4-10, IP4-11

**1900**  
DATE Party – Networking Event  
supported by HiSilicon  
> SEE PAGE 009

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**TECHNICAL SESSIONS – THURSDAY**

**9.1**  
SPECIAL DAY ON "SILICON PHOTONICS": ADVANCEMENTS ON SILICON PHOTONICS  
**AMPHITHÉÂTRE JEAN PROUVE** 0830 - 1000

Chair: Gabriela Nicolescu, École Polytechnique de Montréal, CA

Co-Chair: Luca Ramini, Hewlett Packard Labs, US

**0830**  
System Study of Silicon Photophotonics Modulator in Short Reach Gridless Coherent Networks  
**Naim Ben-Hamida**¹, Ahmad Abdo¹, Xueyang Li², Md Samiul Alam², Mahdi Parvizi¹, Claude D’Amours³ and David V. Plant³  
¹Ciena Corporation, CA; ²McGill University, CA; ³University of Ottawa, CA

**0900**  
Fully Integrated Photonic Circuits on Silicon by means of III-V/ Silicon Bonding  
**Florian Denis-le Coarer**  
SCINTIL Photonics, US

**0930**  
III-V/Silicon hybrid lasers integration on CMOS-compatible 200mm and 300mm platforms  
**Karim Hassan**¹, Szilag Bertrand¹, Laetitia Adelmini¹, Cecilia Dupre¹, Elodie Ghegin², Philippe Rodriguez¹, Fabrice Nemouchi¹, Pierre Brianseau¹, Antoine Schembri¹, David Carrara³, Pierrick Cavalie³, Florent Franchin³, Marie-Christine Roure¹, Loic Sanchez¹, Christophe Jany¹ and Ségolène Olivier¹  
¹CEA-Leti, FR; ²STMicroelectronics, FR; ³Almae Technologies, FR

**1000**  
Exhibition and Coffee Break

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**9.2**  
AUTONOMOUS SYSTEMS DESIGN INITIATIVE: ARCHITECTURES AND FRAMEWORKS FOR AUTONOMOUS SYSTEMS  
**CHAMROUSSE** 0830 - 1000

Chair: Selma Saidi, TU Dortmund, DE  
Co-Chair: Rolf Ernst, TU Braunschweig, DE

**0830**  
DeepRacing: A framework for Agile Autonomy  
**Trent Weiss** and Madhur Behl  
University of Virginia, US

**0900**  
Fail-Operational Automotive Software Design Using Agent-Based Graceful Degradation  
**Philipp Weiss**¹, Andreas Weichslgartner², Felix Reimann² and Sebastian Steinhorst¹  
¹TU Munich, DE; ²Audi Electronics Venture GmbH, DE

**0930**  
A Distributed Safety Mechanism using Middleware and Hypervisors for Autonomous Vehicles  
**Tjerk Bijlsma**¹, Andrii Buriachevskyi², Alessandro Frigerio³, Yuting Fu³, Kees Goossens³, Ali Osman Örs³, Pieter J. van der Perk³, Andrei Terechko² and Bart Vermeulen²  
¹TNO, NL; ²NXP Semiconductors, NL; ³Eindhoven University of Technology, NL

**1000**  
Exhibition and Coffee Break
9.3 SPECIAL SESSION: IN MEMORY COMPUTING FOR EDGE AI

AUTRANS  
Chair: Maha Kooli, CEA-Leti, FR  
Co-Chair: Alexandre Levisse, EPFL, CH  
In-Memory Computing (IMC) represents new computing paradigm where computation happens at data location. Within the landscape of IMC approaches, non-von Neumann architectures seek to minimize data movement associated with computing. Artificial intelligence applications are one of the most promising use case of IMC since they are both compute- and memory-intensive. Running such applications on edge devices offers significant save of energy consumption and high-speed acceleration. This special session proposes to take the attendees along a journey through IMC solutions for Edge AI. This session will cover four different viewpoints of IMC for Edge AI with four talks:  
(i) Enabling flexible electronics very-Edge AI with IMC,  
(ii) design automation methodology for computational SRAM for energy efficient SIMD operations,  
(iii) circuit/architecture/application multiscale design and optimization methodologies for IMC architectures, and  
(iv) device circuit and architecture optimizations to enable PCM-based deep learning accelerators.  
The speakers come from three different continents (Asia, Europe, America) and four different countries (Singapore, France, USA, Switzerland). Two speakers are affiliated to academic institutes; one to industry; and one to an institute of technological research center. We strongly believe that the topic and especially selected talks are extremely hot topics in the community and will attract various people from different countries and affiliations, from both academia and industry. Furthermore, thanks to its cross layer nature, we believe that this session is tailored to touch a wide range of experts from device and circuit community up to system and application design community. We also believe that highlighting and discussing such design methodologies is a key point for high quality and high impact research. Following up previous occurrences and success of IMC-oriented sessions and panels in DAC2019 as well as in ISLPED2019, we believe that this topic is extremely hot in the community and will trigger fruitful interactions and, we hope, collaboration among the community. We thereby expect more than 60 attendees for this session. This session will be the object of two scientific papers that will be integrated with DATE proceedings in case of acceptance.

0830 Fledge: Flexible edge platforms enabled by in-memory computing  
Kamalika Datta¹, Umesh Chand², Arko Dutt¹, Devendra Singh², Aaron Thean² and Mohamed M. Sabry¹  
¹Nanyang Technological University, SG; ²National University of Singapore, SG

0850 Bitcells for Energy-Efficient Vector Processing  
Jean-Philippe Noel¹, Valentin Egloff¹, Maha Kooli¹, Roman Gauchi¹, Jean-Michel Portal², Henri-Pierre Charles¹, Pascal Vivet¹ and Bastien Giraud¹  
¹CEA-Leti, FR; ²Aix-Marseille University, FR

9.4 EFFICIENT DNN DESIGN WITH APPROXIMATE COMPUTING

STENDHAL  
Chair: Daniel Menard, INSA Rennes, FR  
Co-Chair: Seokhyeong Kang, Pohang University of Science and Technology, KR  
Deep Neural Networks (DNN) are widely used in numerous domains. Cross-layer DNN approximation requires efficient simulation framework. The GPU-accelerated simulation framework, ProxSim, supports DNN inference and retraining for approximate hardware. A significant amount of energy is consumed during the training process due to excessive memory accesses. The precision-controlled memory systems, dedicated for GPUs, allow flexible management of approximation. New generation of networks, like Capsule Networks, provide better learning capabilities but at the expense of high complexity. ReD-CaNe methodology analyzes resilience through an error injection and approximates them.

0900 PCM: Precision-Controlled Memory System for Energy Efficient Deep Neural Network Training  
Boyéal Kim¹, SangHyun Lee¹, Hyun Kim², Duy-Thanh Nguyen³, Minh-Son Le³, Ik Joon Chang³, Dohun Kwon³, Jin Hyeok Yoo⁴, Jun Won Choi⁵ and Hyuk-Jae Lee¹  
¹Seoul National University, KR; ²Seoul National University of Science and Technology, KR; ³Kyung Hee University, KR; ⁴Hanyang University, KR

0930 ReD-CaNe: A Systematic Methodology for Resilience Analysis and Design of Capsule Networks under Approximations  
Alberto Marchisio¹, Vojtech Mrazek², Muhammad Abdullah Hanif¹ and Muhammad Shafique¹  
¹TU Wien, AT; ²Brno University of Technology, CZ

SPEAKERS | PRESENTING AUTHORS ARE HIGHLIGHTED
9.5 EMERGING MEMORY DEVICES

**Chair:** Alexandre Levisse, EPFL, CH
**Co-Chair:** Marco Vacca, Politecnico di Torino, IT

The development of future memories is driven by new devices, studied to overcome the limitations of traditional memories. Among these devices STT magnetic RAMs play a fundamental role, due to their excellent performance coupled with long endurance and non-volatility. What are the issues that these memories face? How can we solve them and make them ready for a successful commercial development? And if, by changing perspective, emerging devices are used to improve existing memories like SRAM? These are some of the questions that this section aim to answer.

**0830**
**Impact of Magnetic Coupling and Density on STT-MRAM Performance**
Lizhou Wu¹, Siddharth Rao², Mottaqiallah Taouil¹, Erik Jan Marinissen², Gouri Sankar Kar² and Said Hamdioui¹
¹TU Delft, NL; ²IMEC, BE

**0900**
**High-Density, Low-Power Voltage-Control Spin Orbit Torque Memory with Synchronous Two-Step Write and Symmetric Read Techniques**
Haotian Wang¹, Wang Kang¹, Liuyang Zhang¹, He Zhang¹, Brajesh Kumar Kaushik² and Weisheng Zhao¹
¹Beihang University, CN; ²IIT Roorkee, IN

**0930**
**Design of Almost-Nonvolatile Embedded DRAM Using Nanoelectromechanical Relay Devices**
Hongtao Zhong, Mingyang Gu, Juejian Wu, Huazhong Yang and Xueqing Li
Tsinghua University, CN

**IPs**
IP4-14, IP4-15

1000 Exhibition and Coffee Break

9.7 DIVERSE APPLICATIONS OF EMERGING TECHNOLOGIES

**Chair:** Vasilis Pavlidis, The University of Manchester, GB
**Co-Chair:** Bing Li, TU Munich, DE

This session examines a diverse set of applications for emerging technologies. Papers consider the use of Q-learning to perform more efficient backups in non-volatile processors, the use of emerging technologies to mitigate hardware side-channels, time-sequence-based classification that rise from ultrasonic patterns due to hand movements for gesture recognition, and processing-in-memory-based solutions to accelerate DNA alignment searches.

**0830**
**Q-learning Based Backup for Energy Harvesting Powered Embedded Systems**
Wei Fan, Yujie Zhang, Weining Song, Mengying Zhao, Zhaoyan Shen and Zhiping Jia
Shandong University, CN

**0900**
**A Novel TIGFET-based DFF Design for Improved Resilience to Power Side-Channel Attacks**
Mohammad Mehdi Sharifi¹, Ramin Rajaei¹, Patsy Cadareanu², Pierre-Emmanuel Gaillard², Yier Jin³, Michael Niemier¹ and X. Sharon Hu¹
¹University of Notre Dame, US; ²University of Utah, US; ³University of Florida, US

**0930**
**Low Complexity Multi-directional In-Air Ultrasonic Gesture Recognition Using a TCN**
Emad A. Ibrahim¹, Marc Geilen¹, Jos Huisken¹, Min Li² and Jose Pineda de Gyvez²
¹Eindhoven University of Technology, NL; ²NXP Semiconductors, NL

**IPs**
IP4-17

1000 Exhibition and Coffee Break
Designing large memories under manufacturing variability requires statistical approaches that rely on SPICE simulations at different Process, Voltage, Temperature operating points to verify that yield requirements will be met. Variation-aware simulations of full memories that consist of millions of transistors is a challenging task for both SPICE simulators and statistical methodology to achieve accurate results.

The ideal solution for variation-aware verifications of full memories would be to run Monte Carlo simulations through SPICE simulators to assess that all the addressable elements enable successful write and read operations. However, this classical approach suffers from practical issues and prevent it to be used. Indeed, for large memory arrays (e.g. MB and more) the number of SPICE simulations to perform would be intractable to achieve a descent statistical precision. Moreover, the SPICE simulation of a single sample of the full-memory netlist that involve millions or billions of MOSFETs and parasitic elements might be very long or impossible because of the netlist size. Unfortunately, Fast-SPICE simulations are not a palatable solution for final verification because the loss of accuracy compared to pure SPICE simulations is difficult to evaluate for such netlists.

So far, most of the variation-aware methodologies to analyze and validate Mega-MOSFET memories rely on the assumption that the sub-blocks of the system (e.g. control unit, IOs, row decoders, column circuitries, memory cells) might be assessed independently. Doing so memory designers apply dedicated statistical approaches for each individual sub-block to reduce the overall simulation time to achieve variation-aware closure. When considering that each element of the memory is independent of its neighborhood, the simulation of the memory is drastically reduced to few MOSFETs on the critical paths (longest paths for read or write memory operation), the other sub-blocks being idealized and estimations being derived under Gaussian assumption. Using such an approach, memory designers avoid the usual statistical simulations of the full memory that is, most of the time, unpractical in terms of duration and load. Although the aforementioned approach has been widely used by memory designers, these methods reach their limits when designing memory for low-power and advanced-node technologies where non idealities arise.

The consequence of less reliable results is that the memory designers compensate by increasing security margins at the expense of performances to achieve satisfactory yield. In this context sub-blocks can no longer be considered individually and Gaussianity no longer prevails, other practical simulation flows are required to verify full memories with satisfying performances. New statistical approaches and simulation flows must handle memory slices or critical paths with all relevant sub-blocks in order to consider element interactions to be more realistic. Additionally, these approaches must handle the hierarchy of the memory to respect variation ranges of each sub-block, from low sigma for control units and IOs to high sigma for highly replicated blocks. Using a virtual reconstruction of the full memory the yield can be asserted without relying on the assumptions of individual sub-block analyzes. With accurate estimation over the full memory, no more security margins are required, and better performances will be reached.\footnote{Panelists:}

Panelists:

Yves Laplanche, ARM, FR
Lorenzo Ciampolini, CEA, FR
Pierre Faubet, Silvaco, FR

1000 Exhibition and Coffee Break

**SPEAKERS | PRESENTING AUTHORS ARE HIGHLIGHTED**

**DATE 2020**

**POSTER AREA 1000 - 1030**
Interactive Presentations run simultaneously during a 30-minute slot. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session.

**IP4-1**
Jiaqi Zhang\textsuperscript{1}, Ying Zhang\textsuperscript{1}, Huawei Li\textsuperscript{2} and Jianhui Jiang\textsuperscript{3} \\
\textsuperscript{1}Tongji University, CN; \textsuperscript{2}Chinese Academy of Sciences, CN; \textsuperscript{3}School of Software Engineering, Tongji University, CN

**IP4-2**
Bitstream Modification Attack on SNOW 3G \\
Michail Moraitis and Elena Dubrova \\
Royal Institute of Technology - KTH, SE

**IP4-3**
A Machine Learning Based Write Policy for SSD Cache in Cloud Block Storage \\
Yu Zhang\textsuperscript{1}, Ke Zhou\textsuperscript{1}, Ping Huang\textsuperscript{2}, Hua Wang\textsuperscript{1}, Jianying Hu\textsuperscript{3}, Yangtao Wang\textsuperscript{1}, Yongguang Ji\textsuperscript{3} and Bin Cheng\textsuperscript{3} \\
\textsuperscript{1}Huazhong University of Science & Technology, CN; \textsuperscript{2}Temple University, US; \textsuperscript{3}Tencent Technology (Shenzhen) Co., Ltd., CN

**IP4-4**
You Only Search Once: A Fast Automation Framework for Single-Stage DNN/Accelerator Co-design \\
Weiwei Chen, Ying Wang, Shuang Yang, Cheng Liu and Lei Zhang \\
Chinese Academy of Sciences, CN
When Sorting Network Meets Parallel Bitstreams: A Fault-Tolerant Parallel Ternary Neural Network Accelerator based on Stochastic Computing

Yawen Zhang¹, Sheng Lin², Runsheng Wang¹, Yanzhi Wang², Yuan Wang¹, Weikang Qian³ and Ru Huang¹
¹Peking University, CN; ²Northeastern University, US; ³Shanghai Jiao Tong University, CN

WavePro: Clock-less Wave-Propagated Pipeline Compiler for Low-Power and High-Throughput Computation

Yehuda Kra, Adam Teman and Tzachi Noy
Bar-Ilan University, IL

DeepNVM: A Framework for Modeling and Analysis of Non-Volatile Memory Technologies for Deep Learning Applications

Ahmet Inci, Mehmet M. Isgenc and Diana Marculescu
Carnegie Mellon University, US

Efficient Embedded Machine Learning applications using Echo State Networks

Rolando Brondolin¹, Luca Cerina¹, Giuseppe Franco²,³, Claudio Gallicchio³, Alessio Micheli³ and Marco D. Santambrogio¹
¹Politecnico di Milano, IT; ²Scuola Superiore Sant’Anna, IT; ³Università di Pisa, IT

ExpliFrame: Exploiting Page Frame Cache for Fault Analysis of Block Ciphers

Anirban Chakraborty¹, Sarani Bhattacharya², Sayandeep Saha¹ and Debdeep Mukhopadhyay¹
¹IIT Kharagpur, IN; ²KU Leuven, BE

XGBIR: An XGBoost-based IR Drop Predictor for Power Delivery Network

Chi-Hsien Pao, Yu-Min Lee and An-Yu Su
National Chiao Tung University, TW

On Pre-Assignment Route Prototyping for Irregular Bumps on BGA Packages

Jyun-Ru Jiang¹, Yun-Chih Kuo², Simon Chen³ and Hung-Ming Chen¹
¹National Chiao Tung University, TW; ²National Taiwan University, TW; ³MediaTek, inc, TW

Towards best-effort approximation: Applying NAS to Approximate Computing

Weiwei Chen, Ying Wang, Shuang Yang, Cheng Liu and Lei Zhang
Chinese Academy of Sciences, CN

On the Automatic Exploration of Weight Sharing for Deep Neural Network Compression

Etienne Dupuis¹,², David Novo², Ian O’Connor¹ and Alberto Bosio¹
¹Lyon Institute of Nanotechnology, FR; ²Université de Montpellier, FR; ³École Centrale de Lyon, FR

Robust and High-Performance 12-T Interlocked SRAM for In-Memory Computing

Neelam Surana, Mili Lavana, Abhishek Barma and Joycee Mekie
IIT Gandhinagar, IN

High Density STT-MRAM compiler design, validation and characterization methodology in 28nm FDSOI technology

Piyush Jain¹, Akshay Kumar¹, Nicolaas Van Winkelhoff², Didier Gayraud², Surya Gupta¹, Abdelali El Amraoui², Giorgio Palma², Alexandra Gourio², Laurentz Vachez², Luc Palau², Jean-Christophe Buy² and Cyrille Dray²
¹ARM Embedded Technologies Pvt Ltd., IN; ²ARM France, FR

An Approximation-based Fault Detection Scheme for Image Processing Applications

Matteo Biasielli, Luca Cassano and Antonio Miele
Politecnico di Milano, IT

Transport-Free Module Binding for Sample Preparation using Microfluidic Fully Programmable Valve Arrays

Gautam Choudhary¹, Sandeep Pal¹, Debraj Kundu¹, Sukanta Bhattacharjee², Shigeru Yamashita³, Bing Li⁴, Ulf Schlichtmann⁴ and Sudip Roy¹
¹IIT Roorkee, IN; ²IIT Guwahati, IN; ³Ritsumeikan University, JP; ⁴TU Munich, DE; ⁵Adobe Research, IN

Special Day on "Silicon Photonics": High-Speed Silicon Photonics Interconnects for Data Center and HPC

Amphithéâtre Jean Prouve 1100 - 1230
Chair: Ian O’Connor, École Centrale de Lyon, FR
Co-Chair: Luca Ramini, Hewlett Packard Labs, US

The need and challenges of Co-packing and Optical Integration in Data Centers

Liron Gantz
Mellanox, US

Power and Cost Estimate of Scalable All-to-All Topologies with Silicon Photonics Links

Luca Ramini
Hewlett Packard Labs, US

The next frontier in silicon photonic design: experimentally validated statistical models

Geoff Duggan¹, James Pond¹, Xu Wang¹, Ellen Schelew¹, Federico Gomez¹, Milad Mahpeykar¹, Ray Chung¹, Zequin Lu¹, Parya Samadian¹, Jens Niegemann¹, Adam Reid¹, Roberto Armenta¹, Dylan McGuire¹, Peng Sun², Jared Hulme², Mudit Jan² and Ashkan Seyedi²
¹Lumerical, US; ²Hewlett Packard Labs, US

Exhibition and Lunch Break
10.2 AUTONOMOUS SYSTEMS DESIGN INITIATIVE: UNCERTAINTY HANDLING IN SAFE AUTONOMOUS SYSTEMS (UHSAS)

Chair: Philipp Mundhenk, Autonomous Intelligent Driving GmbH, DE
Co-Chair: Ahmad Adee, Bosch Corporate Research, DE

1100 Making the Relationship between Uncertainty Estimation and Safety Less Uncertain
Peter Schlicht1, Vincent Aravantinos2 and Fabian Hüger1
1Volkswagen, DE; 2AID, DE

1130 System Theoretic View on Uncertainties
Roman Gansch and Ahmad Adee
Robert Bosch GmbH, DE

1200 Detection of False Negative and False Positive Samples in Semantic Segmentation
Hanno Gottschalk1, Matthias Rottmann1, Kira Maag1, Robin Chan1, Fabian Hüger2 and Peter Schlicht2
1School of Mathematics & Science and ICMD, DE; 2Volkswagen, DE

1230 Exhibition and Lunch Break

10.3 SPECIAL SESSION: NEXT GENERATION ARITHMETIC FOR EDGE COMPUTING

Chair: Farhad Merchant, RWTH Aachen University, DE
Co-Chair: Akash Kumar, TU Dresden, DE

Arithmetic is ubiquitous in today’s digital world, ranging from embedded to high-performance computing systems. With machine learning at fore in a wide range of application domains from wearables, automotive, avionics to weather prediction, sufficiently accurate yet low-cost arithmetic is the need for the day. Recently, there have been several advances in the domain of computer arithmetic like high-precision anchored numbers from ARM, posit arithmetic by John Gustafson, and bfloat16, etc. as an alternative to IEEE 754-2008 compliant arithmetic. Optimizations on fixed-point and integer arithmetic are also pursued actively for low-power computing architectures. Furthermore, approximate computing and transprecision/mixed-precision computing have been exciting areas for research forever.

While academic research in the domain of computer arithmetic has a long history, industrial adoption of some of these new data-types and techniques is in its early stages and expected to increase in future. bfloat16 is an excellent example of that. In this special session, we bring academia and industry together to discuss latest results and future directions for research in the domain of next-generation computer arithmetic.

1100 REALM: Reduced-Error Approximate Log-based Integer Multiplier
Hassaan Saadat1, Haris Javaid2, Aleksandar Ignjatovic1 and Sri Parameswaran1
1University of New South Wales, AU; 2Xilinx, SG

1130 A fast BDD Minimization Framework for Approximate Computing
Andreas Wendler and Oliver Keszocze
Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

1200 On the Design of High Performance HW Accelerator through High-level Synthesis Scheduling Approximations
Siyuan Xu and Benjamin Carrion Schaefer
University of Texas at Dallas, US

1215 Fast Kriging-based Error Evaluation for Approximate Computing Systems
Justine Bonnot1, Karol Desnos1 and Daniel Menard2
1Université de Rennes/ Inria/ IRISA, FR; 2INSA Rennes, FR

1230 Exhibition and Lunch Break
10.5  EMERGING MACHINE LEARNING APPLICATIONS AND MODELS

BAYYARD  1100 - 1230
Chair:  Mladen Berekovic, TU Braunschweig, DE
Co-Chair:  Sophie Quinton, INRIA, FR
This session presents new application domains and new models for neural networks, discussing two novel video applications: multi-view and surveillance, and discussing a Bayesian model approach for neural networks.

1100  Communication-efficient View-Pooling for Distributed Inference with Multi-View Neural Networks
Manik Singhal, Anand Raghunathan and Vijay Raghunathan
School of Electrical and Computer Engineering, Purdue University, US

1130  An Anomaly Comprehension Neural Network for Surveillance Videos on Terminal Devices
Yuan Cheng1, Guangtai Huang2, Peining Zhen1, Bin Liu2, Hai-Bao Chen1, Ngai Wong3 and Hao Yu2
1Shanghai Jiao Tong University, CN; 2Southern University of Science and Technology, CN; 3University of Hong Kong, HK

1200  BYNQNet: Bayesian Neural Network with Quadratic Activations for Sampling-Free Uncertainty Estimation on FPGA
Hiromitsu Awano and Masanori Hashimoto
Osaka University, JP

1230  Exhibition and Lunch Break

10.6  SECURE PROCESSOR ARCHITECTURE

LESDEGUÍÈRES  1100 - 1230
Chair:  Emanuel Regnath, TU Munich, DE
Co-Chair:  Erkay Savas, Sabanci University, TR
This session proposes an overview of new mechanisms to protect processor architectures, boot sequences, caches, and energy management. The solutions strive to address and mitigate a wide range of attack methodologies, with a special focus on new emerging attacks.

1100  Capturing and Obscuring Ping-Pong Patterns to Mitigate Continuous Attacks
Kai Wang1, Fengkai Yuan2, Rui Hou2, Zhenzhou Ji1 and Dan Meng2
1Harbin Institute of Technology, CN; 2Chinese Academy of Sciences, CN

1130  Mitigating Cache-Based Side-Channel Attacks through Randomization: A Comprehensive System and Architecture Level Analysis
Han Wang1, Hossein Sayadi1, Avesta Sasan1, Setareh Rafatirad1, Houman Homayoun1,3, Liang Zhao1 and Tinoosh Mohsenin2
1George Mason University, US; 2University of California, Davis, US

1200  Extending the RISC-V Instruction Set for Hardware Acceleration of the Post-Quantum Scheme LAC
Tim Fritzmann1, Georg Sigi1,2 and Johanna Sepúlveda3
1TU Munich, DE; 2Fraunhofer AISec, DE; 3Airbus Defence and Space, DE

1230  Exhibition and Lunch Break

10.7  ACCELERATORS FOR NEUROMORPHIC COMPUTING

BERLIOZ  1100 - 1230
Chair:  Michael Niemier, University of Notre Dame, US
Co-Chair:  Xunzhao Yin, Zhejiang University, CN
In this session, special hardware accelerators based on different technologies for neuromorphic computing will be presented. These accelerators
(i) improve the computing efficiency by using pulse widths to deliver information across memristor crossbars,
(ii) enhance the robustness of neuromorphic computing with unary coding and priority mapping, and
(iii) explore the modulation of light in transferring information so to push the performance of computing systems to new limits.

1100  A Pulse Width Neuron with Continuous Activation for Processing-In-Memory Engines
Shuhang Zhang1, Bing Li1, Hai (Helen) Li1,2 and Ulf Schlichtmann1
1TU Munich, DE; 2Duke University, US

1130  Go Unary: A Novel Synapse Coding and Mapping Scheme for Reliable ReRAM-based Neuromorphic Computing
Chang Ma, Yanan Sun, Weikang Qian, Ziqi Meng, Rui Yang and Li Jiang
Shanghai Jiao Tong University, CN

1200  LightBulb: A Photonic-Nonvolatile-Memory-based Accelerator for Binarized Convolutional Neural Networks
Farzaneh Zokaee1, Qian Lou1, Nathan Youngblood2, Weichen Liu3, Yiyuan Xie4 and Lei Jiang1
1Indiana University Bloomington, US; 2University of Pittsburgh, US; 3Nanyang Technological University, SG; 4Southwest University, CN

1230  Exhibition and Lunch Break
10.8 EXHIBITION THEATRE KEYNOTE AND PUBLISHER’S SESSION

EXHIBITION THEATRE 1100 – 1230

Organiser: Ahmed Jerraya, CEA Tech, FR

As special highlight, DATE 2020 Exhibition Theatre features an Exhibition Theatre Keynote providing everybody involved in the design of microelectronics products and applications with very valuable advice and with deep insight into the latest challenges addressed by the world-wide market leader STMicroelectronics. After the keynote researchers are invited to discuss with the leading publisher Springer how to publish their research work.

1100 Exhibition Theatre Keynote: Design-in-the-Cloud: Myth and Reality

Philippe Quinio
STMicroelectronics, FR

The Cloud is promising orders of magnitude savings in time to market for integrated circuits, owing to CPU elasticity. However, practical limitations still mandate a selective approach to the product design flow and the business models have yet to be fully defined by vendors. The economic equation of designing in the cloud is challenging. In addition, design houses, IDMs and OEM customers have to decide to what extent they want to rely on Cloud service providers to maintain the confidentiality of their IP or SOC databases and honor export control requirements, in a context where such concerns are increasingly relevant in EDA vendor and IC supplier selection. This keynote will explore those topics based on ST’s own experience and trials.

1200 Publisher’s Session: How to Publish Your Research Work

Charles Glaser
Springer, US

This publisher’s session invites all attendees to discuss how and why to publish their research work with Springer Nature. Charles Glaser, Editorial Director for Springer, will present his advice for collaboration in research dissemination. He will be available in this session, as well as the entire exhibition, to discuss the publication of your next book.

Springer is part of Springer Nature, which has over 13,000 employees in over 50 countries. Springer publishes a wide variety of scientific and technical book and journal content, including over 12,000 book titles per year and over 3,000 journals. Our content is distributed globally, via our online portal known as Springerlink, as well as in-print via springer.com and a variety of retail outlets, e.g., amazon.com. Our book publishing includes a variety of content types, including textbooks, professional books, research monographs, and major reference works. Since Springerlink is accessed by more than 15,000 academic and corporate institutions globally, our authors’ work has unparalleled, global reach. We offer our authors individualized, expert relationships, throughout the lifecycle of their publishing effort. This talk will describe the “how” and “why” of publishing with Springer.

1230 Exhibition and Lunch Break
1500  Formally-Specifiable Agent Behavior Models for Autonomous Vehicle Test Generation  
Jonathan DeCastro  
Toyota Research Institute, US

1530  Exhibition and Coffee Break

11.3 SPECIAL SESSION: EMERGING NEURAL ALGORITHMS AND THEIR IMPACT ON HARDWARE

AUTRANS  1400 - 1530

Chair: Ian O’Connor, École Centrale de Lyon, FR  
Co-Chair: Michael Niemier, University of Notre Dame, US

1400  Analog Resistive Crossbar Arrays for Neural Network Acceleration  
Martin Frank  
IBM, US

1430  In-Memory Computing for Memory Augmented Neural Networks  
X. Sharon Hu¹ and Anand Raghunathan²  
¹University of Notre Dame, US; ²Purdue University, US

1500  Hardware Challenges for Neural Recommendation Systems  
Udit Gupta  
Harvard University, US

1530  Exhibition and Coffee Break

11.4 RELIABLE IN-MEMORY COMPUTING

STENDHAL  1400 - 1530

Chair: Jean-Philippe Noel, CEA-Leti, FR  
Co-Chair: Kvatinsky Shahar, Technion, IL

This session deals with work on the reliability of computing in memories. This includes new design techniques to improve CNN computing in ReRAM going through the co-optimization between device and algorithm to improve the reliability of ReRAM-based Graph Processing. Moreover, this session also deals with work on the improvement of reliability of well-established STT-MRAM and PCM. Finally, early works presenting stochastic computing and disruptive image processing techniques based on memristor are also discussed.

1400  ReBoc: Accelerating Block-Circulant Neural Networks in ReRAM  
Yitu Wang¹, Fan Chen², Linghao Song², C.-J. Richard Shi³, Hai (Helen) Li²,⁴ and Yiran Chen²  
¹Fudan University, CN; ²Duke University, US; ³University of Washington, US; ⁴TU Munich, US

1430  GraphRSim: A Joint Device-Algorithm Reliability Analysis for ReRAM-based Graph Processing  
Chin-Fu Nien¹, Yi-Jou Hsiao², Hsiang-Yun Cheng¹, Cheng-Yu Wen³, Ya-Cheng Ko³ and Che-Ching Lin³  
¹Academia Sinica, TW; ²National Chiao Tung University, TW; ³National Taiwan University, TW

1500  STAIR: High Reliable STT-MRAM Aware Multi-Level I/O Cache Architecture by Adaptive ECC Allocation  
Mostafa Hadizadeh, Elham Cheshmikhani and Hossein Asadi  
Sharif University of Technology, IR

1515  Effective Write Disturbance Mitigation Encoding Scheme for High-density PCM  
Muhammad Imran, Taehyun Kwon and Joon-Sung Yang  
Sungkyunkwan University, KR

IPs IP5-6, IP5-7

1530  Exhibition and Coffee Break

11.5 COMPILATE TIME AND VIRTUALIZATION SUPPORT FOR EMBEDDED SYSTEM DESIGN

BAYARD  1400 - 1530

Chair: Nicola Bombieri, Università di Verona, IT  
Co-Chair: Rodolfo Pellizzoni, University of Waterloo, CA

The session leverages compiler support and novel architectural features, such as virtualization extensions and emerging memory structures, to optimize the design flow of modern embedded systems.

1400  Unified Thread- and Data-Mapping for Multi-Threaded Multi-Phase Applications on SPM Many-Cores  
Vanchinathan Venkataramani, Anuj Pathania and Tulika Mitra  
National University of Singapore, SG

1430  Generalized Data Placement Strategies for Racetrack Memories  
Asif Ali Khan, Andres Goens, Fazal Hameed and Jeronimo Castrillon  
TU Dresden, DE

1500  ARM-on-ARM: Leveraging Virtualization Extensions for Fast Virtual Platforms  
Lukas Jünger¹, Jan Luca Malte Bölke², Stephan Tobies², Rainer Leupers¹ and Andreas Hoffmann²  
¹RWTH Aachen University, DE; ²Synopsys GmbH, DE

IPs IP5-8, IP5-9

1530  Exhibition and Coffee Break

11.6 AGING: ESTIMATION AND MITIGATION

LESDIGUIÈRES  1400 - 1530

Chair: Arnaud Virazel, Université de Montpellier/ LIRMM, FR  
Co-Chair: Lorena Anghel, Université Grenoble Alpes, FR

This session shares improvements in aging calculations of emerging technologies and how to take these reliability aspects into account during power grid design and floorplanning of FPGAs.

1400  Impact of NBTI Aging on Self-Heating in Nanowire FET  
Om Prakash¹, Hussam Amrouch¹, Sanjeev Kumar Manhas² and Joerg Henkel¹  
¹Karlsruhe Institute of Technology, DE; ²IIT Roorkee, IN
many layers of abstraction within a system that makes it implementable, verifiable and, ultimately, explainable. However, while many layers of abstraction maximise the likelihood of a system to function correctly, this can prevent a design from making full use of the capabilities of current technology. Making systems brittle at a time where NoC- and SoC-based implementations are the only way to increase compute capabilities as clock speed limits are reached, devices are affected by variability and ageing, and heat-dissipation limits impose "dark silicon" constraints. Design challenges of electronic systems are no longer driven by making designs smaller but by creating systems that are ultra-low power, resilient and autonomous in their adaptation to anomalies including faults, timing violations and performance degradation. This gives rise to the idea of self-aware hardware, capable of adaptive behaviours or features taking inspiration from, e.g., biological systems, learning algorithms, factory processes. The challenge is to adopt and implement these concepts while achieving a "next generation" kind of electronic system which is considered at least as useful and trustworthy as its "classical" counterpart—plus additional essential features for future system design and operation. The goal of this Special Session is to present research from world-leading experts addressing state-of-the-art techniques and devices demonstrating the efficacy of concepts of self-awareness, adaptivity and bio-inspiration in the context of real-world hardware systems and applications with a focus on autonomous resource management at runtime, robustness and performance, and new computing architecture in embedded hardware systems.”

11.7 SYSTEM LEVEL SECURITY

BERLIOZ 1400 - 1530

Chair: Pascal Benoit, Université de Montpellier, FR
Co-Chair: David Hely, Université Grenoble Alpes, FR

The session focuses on topics of system-level security, especially related to authentication. The papers span topics of memory authentication and group-of-users authentication, with a focus on IoT applications.

1400 AMSA: Adaptive Merkle Signature Architecture
Emanuel Regnath and Sebastian Steinhorst
TU Munich, DE

1430 DISSECT: Dynamic Skew-and-Split Tree for Memory Authentication
Saru Vig1, Rohan Juneja2 and Siew Kei Lam1
1Nanyang Technological University, SG; 2Qualcomm, IN

1500 Design-flow Methodology for Secure Group Anonymous Authentication
Rashmi Agrawal1, Lake Bu2, Eliakin del Rosario1 and Michel Kinsv1
1Boston University, US; 2Draper Lab, US

1530 Exhibition and Coffee Break

11.8 SPECIAL SESSION: SELF-AWARE, BIOLOGICALLY-INSPIRED ADAPTIVE HARDWARE SYSTEMS FOR ULTIMATE DEPENDABILITY AND LONGEVITY

EXHIBITION THEATRE 1400 - 1530

Chair: Martin A Trefzer, University of York, GB
Co-Chair: Andy M. Tyrrell, University of York, GB

State-of-the-art electronic design allows the integration of complex electronic systems comprising thousands of high-level functions on a single chip. This has become possible and feasible because of the combination of atomic-scale semiconductor technology allowing VLSI of billions of transistors, and EDA tools that can handle their useful application and integration by following strictly hierarchical design methodology. This results in
### TECHNICAL SESSIONS – THURSDAY

#### IP5

**INTERACTIVE PRESENTATIONS**

**POSTER AREA**

1530 - 1600

Interactive Presentations run simultaneously during a 30-minute slot. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session.

**IP5-1**

**Statistical Model Checking of Approximate Circuits: Challenges and Opportunities**

*Josef Strnadl*

Brno University of Technology, CZ

**IP5-2**

**Runtime Accuracy-Configurable Approximate Hardware Synthesis Using Logic Gating and Relaxation**

*Tanfer Alan*¹, Andreas Gerstlauer² and Joerg Henkel¹

¹Karlsruhe Institute of Technology, DE; ²University of Texas at Austin, US

**IP5-3**

**Post-Quantum Secure Boot**

*Vinay B. Y. Kumar*¹, Naina Gupta², Anupam Chattopadhyay¹, Michael Kasper³, Christoph Krauss⁴ and Ruben Niederhagen⁴

¹Nanyang Technological University, SG; ²Indraprastha Institute of Information Technology, IN; ³Fraunhofer Singapore, SG; ⁴Fraunhofer SIT, DE

**IP5-4**

**ROQ: A Noise-Aware Quantization Scheme Towards Robust Optical Neural Networks with Low-bit Controls**

*Jiaqi Gu*¹, Zheng Zhao¹, Chenghao Feng¹, Hanqing Zhu², Ray T. Chen¹ and David Z. Pan¹

¹University of Texas at Austin, US; ²Shanghai Jiao Tong University, CN

**IP5-5**

**Statistical Training for Neuromorphic Computing using Memristor-based Crossbars Considering Process Variations and Noise**

*Ying Zhu*¹, Grace Li Zhang¹, Tianchen Wang², Bing Li², Yiyu Shi², Tsung-Yi Ho³ and Ulf Schlichtmann¹

¹TU Munich, DE; ²University of Notre Dame, US; ³National Tsing Hua University, TW

**IP5-6**

**Computational Restructuring: Rethinking Image Processing using Memristor Crossbar Arrays**

*Baogang Zhang*, Necati Uysal and *Rickard Ewetz*

University of Central Florida, US

**IP5-7**

**SCRIMP: A General Stochastic Computing Acceleration Architecture using ReRAM in-Memory Processing**

*Saransh Gupta*¹, Mohsen Imani¹, Joonseop Sim¹, Andrew Huang¹, Fan Wu¹, M. Hassan Najafi² and Tajana Rosing¹

¹University of California, San Diego, US; ²University of Louisiana, US

**IP5-8**

**TDO-CIM: Transparent Detection and Offloading for Computation In-memory**

*Kanishkan Vadivel¹, Lorenzo Chelini²*, Ali BanaGozari¹, Gagandip Singh², Stefano Corda², Roel Jordans² and Henk Corporaal¹

¹Eindhoven University of Technology, NL; ²IBM Research, CH

**IP5-9**

**BackFlow: Backward Edge Control Flow Enforcement for Low-End ARM Microcontrollers**

*Cyril Breschi¹*, David Hély¹ and Roman Lysecky²

¹LCIS - Grenoble INP, FR; ²University of Arizona, US

**IP5-10**

**Delay Sensitivity Polynomials Based Design-Dependent Performance Monitors for Wide Operating Ranges**

*Ruikai Shi*¹, Liang Yang² and Hao Wang²

¹Chinese Academy of Sciences/ University of Chinese Academy of Sciences, CN; ²Loongson Technology Corporation Ltd., CN

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### TECHNICAL SESSIONS – THURSDAY

#### IP5

**INTERACTIVE PRESENTATIONS**

**POSTER AREA**

1630 - 1700

**Mitigation of Sense Amplifier Degradation Using Skewed Design**

*Daniel Kraak*¹, Mottajiallah Taouil¹, Said Hamdioul¹, Pieter Weckx², Stefan Cosemans² and Francky Catthoor²

¹TU Delft, NL; ²Imec, BE

**IP5-11**

**Blockchain Technology Enabled Pay Per Use Licensing Approach for Hardware IPs**

*Krishnendu Guha*, Debasri Saha and Amlan Chakrabarti

University of Calcutta, IN

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### SPECIAL DAY ON "SILICON PHOTONICS": DESIGN AUTOMATION FOR PHOTONICS

**AMPHITHÉÂTRE JEAN PROUVE**

1600 - 1730

**Chair:** Dave Penkler, SCINTIL Photonics, US

**Co-Chair:** Luca Ramini, Hewlett Packard Labs, US

**1600**

**Opportunities for Cross-Layer Design in High-Performance Computing Systems with Integrated Silicon Photonic Networks**

Asif Mirza, Shadi Manafi Avari, Ebadollah Taheri, Sudeep Pasricha and *Mahdi Nikdast*

Colorado State University, US

**1630**

**Design and validation of photonic IP macros based on foundry PDKs**

*Ruping Cao*, François Chabert and Pieter Dumon

Luceda Photonics, BE

**1700**

**Efficient Optical Power Delivery System for Hybrid Electronic-Photonic Manycore Processors**

Shixi Chen, *Jiang Xu*, Xuanqi Chen, Zhifei Wang, Jun Feng, Jiaxu Zhang, Zhongyuan Tian and Xiao Li

Hong Kong University of Science and Technology, HK

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### AUTONOMOUS SYSTEMS DESIGN INITIATIVE: EMERGING APPROACHES TO AUTONOMOUS SYSTEMS DESIGN

**CHAMROUSSE**

1600 - 1730

**Chair:** Dirk Ziegenbein, Robert Bosch GmbH, DE

**Co-Chair:** Sebastian Steinhorst, TU Munich, DE

**1600**

**A Preliminary View on Automotive Cyber Security Management Systems**

*Christoph Schmittner¹*, Jürgen Dobaj², Georg Macher² and Eugen Brenner²

¹Austrian Institute of Technology, AT; ²TU Graz, AT

**1620**

**Towards Safety Verification of Direct Perception Neural Networks**

*Chih-Hong Cheng*¹, Chung-Hao Huang², Thomas Brunner² and Vahid Hashemi³

¹DENSO Automotive Deutschland GmbH, DE; ²Fortiss, DE; ³Audi AG, DE
Minimizing Execution Duration in the Presence of Learning-Enabled Components
Kunal Agrawal¹, Sanjoy Baruah¹, Alan Burns² and Abhishek Singh¹
¹Washington University in Saint Louis, US; ²University of York, GB

Discussion

Autonomous Systems Design Initiative: Reception
supported by AID – Autonomous Intelligent Driving GmbH
SALLE OISANS
Access for invited participants only.

12.3 RECONFIGURABLE SYSTEMS FOR MACHINE LEARNING
AUTRANS 1600 - 1730
Chair: Bogdan Pasca, Intel, FR
Co-Chair: Smail Niar, Université Polytechnique
Hauts-de-France, FR

Machine learning continues to attract significant research attention and reconfigurable systems offer ample flexibility for exploring new approaches to accelerating these workloads. In this session we explore how FPGAs can be used for a variety of machine learning workloads. We discuss memory optimisations for 3D convolutional neural networks (CNNs), design and implementation of binarised neural networks, and an approach for cascading hybrid precision datapaths to improve CNN classification latency.

1600 Exploration of Memory Access Optimization for FPGA-based 3D CNN Accelerator
Teng Tian, Xi Jin, Letian Zhao, Xiaotian Wang, Jie Wang and Wei Wu
University of Science and Technology of China, CN

1630 A Throughput-Lateness Co-Optimised Cascade of Convolutional Neural Network Classifiers
Alexandros Kouris¹, Stylianos Venieris² and Christos Bouganis¹
¹Imperial College London, GB; ²Samsung AI, GB

1700 OrthrusPE: Runtime Reconfigurable Processing Elements for Binary Neural Networks
Nael Fasfous¹, Manoj-Rohit Vemparala², Alexander Frickenstein² and Walter Stechele¹
¹TU Munich, DE; ²BMW Group, DE

12.4 APPROXIMATE COMPUTING WORKS!
APPLICATIONS & CASE STUDIES
STENDHAL 1600 - 1730
Chair: Oliver Keszocze, Friedrich-Alexander-University Erlangen-Nuremberg, DE
Co-Chair: Benjamin Carrion Schaefer, University of Texas at Dallas, US

Approximate computing leverages the fact that many applications are tolerant of incorrect results. This session highlights that by presenting methods and applications that optimize the tradeoff between area, power and output error. At the same time it is important to ensure that the approximation approaches are scalable because complex problems are addressed. While some of these approaches completely work at the application level, others are oriented towards optimizing key subcircuits.

1600 Towards Generic and Scalable Word-Length Optimization
Van-Phu Ha¹, Tomofumi Yuki² and Olivier Sentieys²
¹Université de Rennes/ Inria/ IRISA, FR; ²INRIA, FR

1630 Trading Sensitivity for Power in an IEEE 802.15.4 Conformant Adequate Demodulator
Paul Detterer¹, Cumhur Erdin¹, Jos Huiskens¹, Hailong Jiao¹, Majid Nabi¹, Twan Basten¹ and Jose Pineda de Gyvez²
¹Eindhoven University of Technology, NL; ²NXP Semiconductors, US

1700 Approximation Trade Offs in an Image-Based Control System
Sayandip De, Sajid Mohamed, Konstantinos Bimpidis, Dip Goswami, Twan Basten and Henk Corporaal
Eindhoven University of Technology, NL

12.5 CYBER-PHYSICAL SYSTEMS FOR MANUFACTURING AND TRANSPORTATION
BAYARD 1600 - 1730
Chair: Ulrike Thomas, Chemnitz University of Technology, DE
Co-Chair: Robert De Simone, INRIA, FR

Modeling and design of transportation and manufacturing systems from a cyber-physical system (CPS) perspective have lately attracted extensive attention and the session covers various aspects, from modelling of traffic intersections and control of traffic signals, to implementations of iterative learning controllers for control blocks. Other contributions deal with the selection of network architectures for manufacturing plants and the Digital Twin of production processes for validation.

1600 CPS-oriented Modeling and Control of Traffic Signals Using Adaptive Back Pressure
Wanli Chang¹, Debayan Roy², Shuai Zhao¹, Anuradha Annaswamy² and Samarjit Chakraborty²
¹University of York, GB; ²TU Munich, DE; ³Massachusetts Institute of Technology, US

1630 Network Synthesis for Industry 4.0
Enrico Fraccaroli, Alan Michael Padovani, Davide Quaglia and Franco Fummi
Università di Verona, IT
**TECHNICAL SESSIONS – THURSDAY**

**1700** Production Recipe Validation through Formalization and Digital Twin Generation  
**Stefano Spellini**, Roberta Chirico, Marco Panato, Michele Lora and Franco Fummi  
1Università di Verona, IT; 2Singapore University of Technology and Design, SG

**1715** Parallel Implementation of Iterative Learning Controllers on Multi-core Platforms  
**Mojtaba Haghi**, Yusheng Yao, Dip Goswami and Kees Goossens  
Eindhoven University of Technology, NL

**12.6 INDUSTRIAL EXPERIENCE: FROM WAFER-LEVEL UP TO IOT SECURITY**  
**LESDIGUIÈRES**  
1600 - 1730  
Chair: **Enrico Macii**, Politecnico di Torino, IT  
Co-Chair: **Norbert Wehn**, TU Kaiserslautern, DE  
This session addresses recent industrial experiences covering all Design Levels from Technology up to System Level

**1600** Wafer-Level Test Path Pattern Recognition and Test Characteristics for Test-Induced Defect Diagnosis  
Andrew Yi-Ann Huang, Katherine Shu-Min Li, Ken Chau-Cheung Cheng, Ji-Wei Li, Leon Li-Yang Chen, Nova Cheng-Yen Tsai, Sying-Jyan Wang, Chen-Shiun Lee, Leon Chou, Peter Yi-Yu Liao, Hsing-Chung Liang and Jwu E Chen  
1NXP Semiconductors Taiwan Ltd., TW; 2National Sun Yat-Sen University, TW; 3National Chung-Hsing University, TW; 4Chung Yuan Christian University, TW; 5National Central University, TW

**1615** A Method of Via Variation Induced Delay Computation  
Moonsu Kim, Yun Heo, Seungjae Jung, Kelvin Lee, Jongpil Lee, Youngmin Shin, Nathaniel Conos and Hanif Fatemi  
1Samsung, KR; 2Synopsys, US

**1630** Fully Automated Analog Sub-Circuit Clustering with Graph Convolutional Neural Networks  
**Keertana Settaluri** and Elias Fallon  
1University of California, Berkeley, US; 2Cadence Design Systems, US

**1645** EVPS: An Automotive Video Acquisition and Processing Platform  
**Christophe Flouzat**, Erwan Piriou, Mickael Guibert, Bojan Jovanovic and Mohamad Oussayran  
1CEA LIST, FR

**1700** An On-board Algorithm Implementation on an Embedded GPU: A Space Case Study  
**Ivan Rodriguez**, Leonidas Kosmidis, Olivier Notebaert, Francisco J Cazorla and David Steenari  
1UPC/ BSC, ES; 2BSC, ES; 3Airbus Defence and Space, FR; 4European Space Agency, NL

**1715** TLS-Level Security for Low Power Industrial IoT Network Infrastructures  
Jochen Mades, Gerd Ebel, Boris Janjic, Frederik Lauer, Carl Rheinländer and Norbert Wehn  
1KSB SE & Co. KGaA, DE; 2TU Kaiserslautern, DE

**TECHNICAL SESSIONS – THURSDAY**

**12.7 POWER-EFFICIENT MULTI-CORE EMBEDDED ARCHITECTURES**  
**BERLIOZ**  
1600 - 1730  
Chair: **Andreas Burg**, EPFL, CH  
Co-Chair: **Semeen Rehman**, TU Wien, AT  
This session has papers that provide power-efficiency solutions for multi-core embedded architectures. Techniques discussed in the session are related to the architectural measures as well as effectively controlling voltage-frequency settings using machine learning based on user experiences.

**1600** Tuning the ISA for increased heterogeneous computation in MPSoCs  
Pedro Henrique Exenberger Becker, Jeckson Dellagostin Souza and Antonio Carlos Schneider Beck  
Universidade Federal do Rio Grande do Sul, BR

**1630** User Interaction Aware Reinforcement Learning for Power and Thermal Efficiency of CPU-GPU Mobile MPSoCs  
**Somdip Dey**, Amit Kumar Singh, Xiaohang Wang and Klaus McDonald-Maier  
1University of Essex, GB; 2South China University of Technology, CN

**1700** Energy-Efficient Two-level Instruction Cache Design for an Ultra-Low-Power Multi-core Cluster  
**Jie Chen**, Igor Loi, Luca Benini and Davide Rossi  
1Università di Bologna, IT; 2GreenWaves Technologies, FR

**12.8 SPECIAL SESSION: EDA CHALLENGES IN MONOLITHIC 3D INTEGRATION: FROM CIRCUITS TO SYSTEMS**  
**EXHIBITION THEATRE**  
1600 - 1730  
Chair: **Pascal Vivet**, CEA-Leti, FR  
Co-Chair: **Mehdi Tahoori**, Karlsruhe Institute of Technology, DE  
Monolithic-3D integration (M3D) has the potential to improve the performance and energy efficiency of 3D ICs over conventional TSV-based counterparts. By using significantly smaller inter-layer vias (ILVs), M3D offers the “true” benefits of utilizing the vertical dimension for system integration: M3D provides ILVs that are 100x smaller than a TSV and have similar dimensions as normal vias in planar technology. This allows M3D to enable high-performance and energy-efficient systems through higher integration density, flexible partitioning of logic blocks across multiple layers, and significantly lower total wire-length. From a system design perspective, M3D is a breakthrough technology to achieve "More Moore and More Than Moore," and opens up the possibility of creating manycore chips with multi-tier cores and network routers by utilizing ILVs. Importantly, this allows us to create scalable manycore systems that can address the communication and computation needs of big data, graph analytics, and other data-intensive parallel applications. In addition, the dramatic reduction in via size and the resulting increase in density opens up numerous opportunities for design optimizations in the manycore domain.
1600  M3D-ADTCO: Monolithic 3D Architecture, Design and Technology Co-Optimization for High Energy-Efficient 3D IC
Sebastien Thuries, Olivier Billoint, Sylvain Choisent, Didier Lattard, Romain Lemaire and Perrine Batude
CEA-Leti, FR

1630  Design of a Reliable Power Delivery Network for Monolithic 3D ICs
Shao-Chun Hung and Krishnendu Chakrabarty
Duke University, US

1700  Power-Performance-Thermal Trade-offs in M3D-Enabled Manycore Chips
Shouvik Musavvir1, Anwesha Chatterjee1, Ryan Kim2, Daehyun Kim1, Janardhan Rao Doppa1 and Partha Pratim Pande1
1Washington State University, US; 2Colorado State University, US

3.8  SOLUTIONS FOR AI ON CHIP USING NEUROMORPHIC HARDWARE, FOR AI FROM EDGE TO CLOUD AND FOR POWER-EFFICIENCY
TUESDAY | 1430 – 1615 > SEE PAGE 052
In this session, Intel and Andes Technology will cover the implementation of AI highlighting neuromorphic hardware, RISC-V and AI from edge to cloud. Dolphin Design will show how to speed up the design of the required power-efficient SoC.

4.8  SOLUTIONS FOR SIP IMPLEMENTATION, IN-SYSTEM TEST AND NOC/SOC TEST
TUESDAY | 1700 – 1830 > SEE PAGE 061
In this session, Mentor, a Siemens Business, ATOS and Zuken will cover in-system test for automotive, test of scalable NoC/SoC and a co-design environment for SiP implementation.

5.8  SPECIAL SESSION: HIGH-LEVEL SYNTHESIS FOR AI HARDWARE
WEDNESDAY | 0830 – 1000 > SEE PAGE 068

6.8  SOLUTIONS FOR EDA DESIGN ENVIRONMENTS
WEDNESDAY | 1100 – 1230 > SEE PAGE 076
In this session, Altair and SEMI/ESDA will cover design environments and IP enabling for different levels of abstraction and multi-physics simulations, as well as the Heterogeneous Integration Roadmap (HIR) for connecting design, manufacturing and assembly.

Exhibition Theatre Chair: Jürgen Haase, edacentrum GmbH, DE
In addition to the conference programme, there will be 10 Exhibition Workshops as part of the exhibition. These workshops will feature technical presentations on the state-of-the-art in our industry, tutorials, a selection of special sessions from the conference and as a special highlight an Exhibition Theatre Keynote. The theatre is located next to the exhibition hall, close to the booths and the rooms of the technical conference.

The Exhibition Theatre sessions are open to conference delegates as well as to exhibition visitors.
7.8  SYSTEMC-BASED VIRTUAL PROTOTYPING: FROM SOC MODELING TO THE DIGITAL TWIN REVOLUTION
WEDNESDAY | 1430 – 1600  > SEE PAGE 081
SystemC-based virtual prototyping has been adopted and deployed for several years in the semiconductor industry, to implement the shift-left paradigm. While interest has been long focused on SoC modeling, the trends are now to extend the modeling activities to the next level, as part of the digital twin revolution. In this session, the multiple benefits of this approach are discussed, as well as the upcoming challenges, both from an industrial and an academic perspective.

8.8  MATHWORKS TUTORIAL
WEDNESDAY | 1700 – 1830  > SEE PAGE 088
Please see online programme for details.

9.8  SPECIAL SESSION – PANEL: VARIATION-AWARE ANALYZES OF MEGA-MOSFET MEMORIES, CHALLENGES AND SOLUTIONS
THURSDAY | 0830 – 1000  > SEE PAGE 094

10.8  EXHIBITION THEATRE KEYNOTE AND PUBLISHER’S SESSION
As special highlight, DATE 2020 Exhibition Theatre features an Exhibition Theatre Keynote providing everybody involved in the design of microelectronics products and applications with very valuable advice and with deep insight into the latest challenges addressed by the world-wide market leader STMicroelectronics. After the keynote, researchers are invited to discuss with the leading publisher Springer how to publish their research work.

EXHIBITION THEATRE KEYNOTE: DESIGN-IN-THE-CLOUD: MYTH AND REALITY
THURSDAY | 1100 – 1200  > SEE PAGE 102
The Cloud is promising orders of magnitude savings in time to market for integrated circuits, owing to CPU elasticity. However, practical limitations still mandate a selective approach to the product design flow and the business models have yet to be fully defined by vendors. The economic equation of designing in the cloud is challenging. In addition, design houses, IDMs and OEM customers have to decide to what extent they want to rely on Cloud service providers to maintain the confidentiality of their IP or SOC databases and honor export control requirements, in a context where such concerns are increasingly relevant in EDA vendor and IC supplier selection. This keynote will explore those topics based on ST’s own experience and trials.

11.8  SPECIAL SESSION: SELF-AWARE, BIOLOGICALLY INSPIRED ADAPTIVE HARDWARE SYSTEMS FOR ULTIMATE DEPENDABILITY AND LONGEVITY
THURSDAY | 1400 – 1530  > SEE PAGE 106

12.8  SPECIAL SESSION: EDA CHALLENGES IN MONOLITHIC 3D INTEGRATION: FROM CIRCUITS TO SYSTEMS
THURSDAY | 1600 – 1730  > SEE PAGE 113

12.8  PUBLISHER’S SESSION: HOW TO PUBLISH YOUR RESEARCH WORK
THURSDAY | 1200 – 1230  > SEE PAGE 102
This publisher’s session invites all attendees to discuss how and why to publish their research work with Springer Nature. Charles Glaser, Editorial Director for Springer, will present his advice for collaboration in research dissemination. He will be available in this session, as well as the entire exhibition, to discuss the publication of your next book.
A DIGITAL MICROFLUIDICS BIO-COMPUTING PLATFORM

Authors: Georgi Tanev, Luca Pezzarossa, Winnie Edith Svendsen and Jan Madsen
TU Denmark, DK

Timeslots:
UB02.2 | Tuesday, 10 March 2020 | 1230 - 1500
UB06.1 | Wednesday, 11 March 2020 | 1200 - 1400
UB08.2 | Wednesday, 11 March 2020 | 1600 - 1800

Abstract: Digital microfluidics is a lab-on-a-chip (LOC) technology used to actuate small amounts of liquids on an array of individually addressable electrodes. Microliter sized droplets can be programmatically dispensed, moved, mixed, split, in a controlled environment which combined with miniaturized sensing techniques makes LOC suitable for a broad range of applications in the field of medical diagnostics and synthetic biology. Furthermore, a programmable digital microfluidics platform holds the potential to add a “fluidic subsystem” to the classical computation model thus opening the doors for cyber-physical bio-processors. To facilitate the programming and operation of such bio-fluidic computing, we propose dedicated instruction set architecture and virtual machine. A set of digital microfluidic core instructions as well as classic computing operations are executed on a virtual machine, which decouples the protocol execution from the LOC functionality.

AT-SPEED DFT ARCHITECTURE FOR BUNDLED-DATA CIRCUITS

Authors: Ricardo Aquino Guazzelli and Laurent Fesquet
Université Grenoble Alpes, FR

Timeslots:
UB02.5 | Tuesday, 10 March 2020 | 1230 - 1500
UB05.7 | Wednesday, 11 March 2020 | 1000 - 1200

Abstract: At-speed testing for asynchronous circuits is still an open concern in the literature. Due to its timing constraints between control and data paths, Design for Testability (DfT) methodologies must test both control and data paths at the same time in order to guarantee the circuit correctness. As Process Voltage Temperature (PVT) variations significantly impact circuit design in newer CMOS technologies and low-power techniques such as voltage scaling, the timing constraints between control and data paths must be tested after fabrication not only under nominal conditions but through a range of operating conditions. This work explores an at-speed testing approach for bundled data circuits, targeting the micropipeline template. The main target of this test approach focuses on whether the sized delay lines in control paths respect the local timing assumptions of the data paths.

A BINARY TRANSLATION FRAMEWORK FOR AUTOMATED HARDWARE GENERATION

Authors: Nuno Paulino and João Canas Ferreira
INESC TEC / University of Porto, PT

Timeslots:
UB07.3 | Wednesday, 11 March 2020 | 1400 - 1600

Abstract: Hardware specialization is an efficient solution for maximization of performance and minimization of energy consumption. This work is based on automated detection of workload by analysis of a compiled application, and on the automated generation of specialized hardware modules. We will present the current version of the binary analysis and translation framework. Currently, our implementation is capable of processing ARMv8 and MicroBlaze (32-bit) Executable and Linking Format (ELF) files or instruction traces. The framework can interpret the instructions for these two ISAs, and detect different types of instruction patterns. After detection, segments are converted into CDFG representations exposing the underlying Instruction Level Parallelism which we aim to exploit via automated hardware generation. On-going work is addressing the extraction of cyclical execution traces or static code blocks, more methods of hardware generation.
ATECES: AUTOMATED TESTING THE ENERGY CONSUMPTION OF EMBEDDED SYSTEMS
Authors: Eduard Enoiu
Mälardalen University, SE
Timeslots:
UB10.10 | Thursday, 12 March 2020 | 1200 - 1430
UB11.1 | Thursday, 12 March 2020 | 1430 - 1630
Abstract: The demostrator will focus on automatically generating test suites by selecting test cases using random test generation and mutation testing is a solution for improving the efficiency and effectiveness of testing. Specifically, we generate and select test cases based on the concept of energy-aware mutants, small syntactic modifications in the system architecture, intended to mimic real energy faults. Test cases that can distinguish a certain behavior from its mutations are sensitive to changes, and hence considered to be good at detecting faults. We applied this method on a brake by wire system and our results suggest that an approach that selects test cases showing diverse energy consumption can increase the fault detection ability. This kind of results should motivate both academia and industry to investigate the use of automatic test generation for energy consumption.

BCFELEAM: BACKFLOW: BACKWARD EDGE CONTROL FLOW ENFORCEMENT FOR LOW END ARM REAL-TIME SYSTEMS
Authors: Bresch Cyril¹, David Héy¹, Roman Lysecky² and Stephanie Chollet¹
¹LCIS, FR; ²University of Arizona, US
Timeslots:
UB05.4 | Wednesday, 11 March 2020 | 1000 - 1200
UB07.2 | Wednesday, 11 March 2020 | 1400 - 1600
Abstract: The C programming language is one of the most popular languages in embedded system programming. Indeed, C is efficient, lightweight and can easily meet high performance and deterministic real-time constraints. However, these assets come at a certain price. Indeed, C does not provide extra features for memory safety. As a result, attackers can easily exploit spatial memory vulnerabilities to hijack the execution flow of an application. The demonstration features a real-time connected infusion pump vulnerable to memory attacks. First, we showcase an exploit that remotely takes control of the pump. Then, we demonstrate the effectiveness of BackFlow, an LLVM-based compiler extension that enforces control-flow integrity in low-end ARM embedded systems.

CATANIS: CAD TOOL FOR AUTOMATIC NETWORK SYNTHESIS
Authors: Davide Quaglia, Enrico Fraccaroli, Filippo Nevi and Sohail Mushtaq
Università di Verona, IT
Timeslots:
UB01.8 | Tuesday, 10 March 2020 | 1030 - 1230
UB05.8 | Wednesday, 11 March 2020 | 1000 - 1200
Abstract: The proliferation of communication technologies for embedded systems opened the way for new applications, e.g., Smart Cities and Industry 4.0. In such applications hundreds or thousands of smart devices interact together through different types of channels and protocols. This increasing communication complexity forces computer-aided design methodologies to scale up from embedded systems in isolation to the global inter-connected system. Network Synthesis is the methodology to optimally allocate functionality onto network nodes and define the communication infrastructure among them. This booth will demonstrate the functionality of a graphic tool for automatic network synthesis developed by the Computer Science Department of University of Verona. It allows to graphically specify the communication requirements of a smart space (e.g., its map can be considered) in terms of sensing and computation tasks together with a library of node types and communication protocols to be used.

BROOK SC: HIGH-LEVEL CERTIFICATION-FRIENDLY PROGRAMMING FOR GPU-POWERED SAFETY CRITICAL SYSTEMS
Authors: Marc Benito, Matina Maria Trompouki and Leonidas Kosmidis
BSC / UPC, ES
Timeslots:
UB04.7 | Tuesday, 10 March 2020 | 1730 - 1930
UB11.2 | Thursday, 12 March 2020 | 1430 - 1630
Abstract: Graphics processing units (GPUs) can provide the increased performance required in future critical systems, i.e. automotive and avionics. However, their programming models, e.g. CUDA or OpenCL, cannot be used in such systems as they violate safety critical programming guidelines. Brook SC (https://github.com/lkosmid/brook) was developed in UPC/BSC to allow safety-critical applications to be programmed in a CUDA-like GPU language, Brook, which enables the certification while increasing productivity. In our demo, an avionics application running on a realistic safety critical GPU software stack and hardware is show cased. In this Bachelor’s thesis project, which was awarded a 2019 HiPEAC Technology Transfer Award, an Airbus prototype application performing general-purpose computations with a safety-critical graphics API was ported to Brook SC in record time, achieving an order of magnitude reduction in the lines of code to implement the same functionality without performance penalty.
CSI-REPUTE: A LOW POWER EMBEDDED DEVICE CLUSTERING APPROACH TO GENOME READ MAPPING

Authors: Tousif Rahman¹, Sidharth Maheshwari¹, Rishad Shafik¹, Ian Wilson¹, Alex Yakovlev¹ and Amit Acharyya²

¹Newcastle University, GB; ²IIT Hyderabad, IN

Timeslots:
UB03.6 | Tuesday, 10 March 2020 | 1500 - 1730
UB04.6 | Tuesday, 10 March 2020 | 1730 - 1930

Abstract: The big data challenge of genomics is rooted in its requirements of extensive computational capability and results in large power and energy consumption. To encourage widespread usage of genome assembly tools there must be a transition from the existing predominantly software-based mapping tools, optimized for homogeneous high-performance systems, to more heterogeneous low power and cost-effective mapping systems. This demonstration will show a cluster system implementation for the REPUTE algorithm, (An OpenCL based Read Mapping Tool for Embedded Genomics) where cluster nodes are composed of low power single board computer (SBC) devices and the algorithm is deployed on each node spreading the genomic workload, we propose a working concept prototype to challenge current conventional high-performance many-core CPU based cluster nodes. This demonstration will highlight the advantage in the power and energy domains of using SBC clusters enabling potential solutions to low-cost genomics.

DEEPSENSE-FPGA: FPGA ACCELERATION OF A MULTIMODAL NEURAL NETWORK

Authors: Mehdi Trabelsi Ajili and Yuko Hara-Azumi
Tokyo Institute of Technology, JP

Timeslots:
UB07.7 | Wednesday, 11 March 2020 | 1400 - 1600
UB10.7 | Thursday, 12 March 2020 | 1200 - 1430

Abstract: Currently, Internet of Things and Deep Learning (DL) are merging into one domain and creating outstanding technologies for various classification tasks. Such technologies require complex DL networks that are mainly targeting powerful platforms with rich computing resources like servers. Therefore, for resource-constrained embedded systems, new challenges of size, performance and power consumption have to be considered, particularly when edge devices handle multimodal data, i.e., different types of real-time sensing data (voice, video, text, etc.). Our ongoing project is focused on DeepSense, a multimodal DL framework combining Convolutional Neural Networks (CNN) and Recurrent Neural Networks (RNN) to process time-series data, such as accelerometer and gyroscope to detect human activity. We aim at accelerating DeepSense by FPGA (Xilinx Zynq) in a hardware-software co-design manner. Our demo will show the latest achievements through latency and power consumption evaluations.

DESIGN AUTOMATION FOR EXTENDED BURST-MODE AUTOMATA IN WORKCRAFT

Authors: Alex Chan, Alex Yakovlev, Danil Sokolov and Victor Khomenko
Newcastle University, GB

Timeslots:
UB05.6 | Wednesday, 11 March 2020 | 1000 - 1200
UB07.6 | Wednesday, 11 March 2020 | 1400 - 1600

Abstract: Asynchronous circuits are known to have high performance, robustness and low power consumption, which are particularly beneficial for the area of so-called “little digital” controllers where low latency is crucial. However, asynchronous design is not widely adopted by industry, partially due to the steep learning curve inherent in the complexity of formal specifications, such as Signal Transition Graphs (STGs). In this demo, we promote a class of the Finite State Machine (FSM) model called Extended Burst-Mode (XBM) automata as a practical way to specify many asynchronous circuits. The XBM specification has been automated in the Workcraft toolkit (https://workcraft.org) with elaborate support for state encoding, conditionals and “don’t care” signals. Formal verification and logic synthesis of the XBM automata is implemented via conversion to the established STG model, reusing existing methods and CAD tools. Tool support for the XBM flow will be demonstrated using several case studies.

DISTRIBUTING TIME-SENSITIVE APPLICATIONS ON EDGE COMPUTING ENVIRONMENTS

Authors: Eudald Sabaté Creixell¹, Unai Perez Mendizabal¹, Eli Kartasakli², Maria A. Serrano Gracia³ and Eduardo Quiñones Moreno³

¹BSC/ UPC, ES; ²BSC, GR; ³BSC, ES

Timeslots:
UB04.10 | Tuesday, 10 March 2020 | 1730 - 1930
UB08.3 | Wednesday, 11 March 2020 | 1600 - 1800
UB11.3 | Thursday, 12 March 2020 | 1430 - 1630

Abstract: The proposed demonstration aims to showcase the capabilities of a task-based distributed programming framework for the execution of real-time applications in edge computing scenarios, in the context of smart cities. Edge computing shifts the computation close to the data source, alleviating the pressure on the cloud and reducing application response times. However, the development and deployment of distributed real-time applications is complex, due to the heterogeneous and dynamic edge environment where resources may not always be available. To address these challenges, our demo employs COMPSs, a highly portable and infrastructure-agnostic programming model, to efficiently distribute time-sensitive applications across the compute continuum. We will exhibit how COMPSs distributes the workload on different edge devices (e.g., NVIDIA GPUs and a Raspberry Pi), and how COMPSs re-adapts this distribution upon the availability (connection or disconnection) of devices.
DL PUF ENAU: DEEP LEARNING BASED PHYSICALLY UNCLONABLE FUNCTION ENROLLMENT AND AUTHENTICATION

**Authors:** Amir Alipour¹, David Hely², Vincent Berouille² and Giorgio Di Natale³

¹Grenoble INP/ LCIS, FR; ²Grenoble INP, FR; ³CNRS/ Grenoble INP/ TIMA, FR

**Abstract:** Physically Unclonable Functions (PUFs) have been addressed nowadays as a potential solution to improve the security in authentication and encryption process in Cyber Physical Systems. The research on PUF is actively growing due to its potential of being secure, easily implementable and expandable, using considerably less energy. To use PUF in common, the low level device Hardware Variation is captured per unit for device enrollment into a format called Challenge-Response Pair (CRP), and recaptured after device is deployed, and compared with the original for authentication. These enrollment + comparison functions can vary and be more data demanding for applications that demand robustness, and resilience to noise. In this demonstration, our aim is to show the potential of using Deep Learning for enrollment and authentication of PUF CRPs. Most importantly, during this demonstration, we will show how this method can save time and storage compared to other classical methods.

ECLT FPGA COMPONENT: EDGE-TO-CLOUD LOCATION-TRANSPARENT FPGA COMPONENT

**Authors:** Takeshi Ohkawa
Tokai University, JP

**Timeslots:**
UB06.5 | Wednesday, 11 March 2020 | 1200 - 1400
UB08.4 | Wednesday, 11 March 2020 | 1600 - 1800

**Abstract:** To exploit the benefits of FPGA, it is necessary to improve the usability of FPGA from the software system as well as the design productivity of FPGA circuitry itself. Therefore, an FPGA component technology is expected in which software can access FPGA circuitry easily and communicate with other FPGA/software components through the network in the whole edge-to-cloud system using a variety of communication protocols. In this demonstration, a location-transparent FPGA component which is capable of image recognition processing and communicating with ROS (Robot Operating System) protocol are exhibited. The FPGA component works in the ROS system and the component can be in an arbitrary location in the Edge-to-Cloud network system.

EEC: ENERGY EFFICIENT COMPUTING VIA DYNAMIC VOLTAGE SCALING AND IN-NETWORK OPTICAL PROCESSING

**Authors:** Ryosuke Matsuo¹, Jun Shiomi¹, Yutaka Masuda² and Tohru Ishihara²
¹Kyoto University, JP; ²Nagoya University, JP

**Timeslots:**
UB01.7 | Tuesday, 10 March 2020 | 1030 - 1230
UB09.7 | Thursday, 12 March 2020 | 1000 - 1200

**Abstract:** This poster demonstration will show results of our two research projects. The first one is on a project of energy efficient computing. In this project we developed a power management algorithm which keeps the target processor always running at the most energy efficient operating point by appropriately tuning the supply voltage and threshold voltage under a specific performance constraint. This algorithm is applicable to wide variety of processor systems including high-end processors and low-end embedded processors. We will show the results obtained with actual RISC processors designed using a 65nm technology. The second one is on a project of in-network optical computing. We show optical functional units such as parallel multipliers and optical neural networks. Several key techniques for reducing the power consumption of optical circuits will be also presented. Finally, we will show the results of optical circuit simulation, which demonstrate the light speed operation of the circuits.

ELSA: EIGENVALUE BASED HYBRID LINEAR SYSTEM ABSTRACTION: BEHAVIORAL MODELING OF TRANSISTOR-LEVEL CIRCUITS USING AUTOMATIC ABSTRACTION TO HYBRID AUTOMATA

**Authors:** Ahmad Tarraf and Lars Hedrich
University of Frankfurt, DE

**Timeslots:**
UB03.2 | Tuesday, 10 March 2020 | 1500 - 1730
UB04.2 | Tuesday, 10 March 2020 | 1730 - 1930
UB05.2 | Wednesday, 11 March 2020 | 1000 - 1200
UB06.2 | Wednesday, 11 March 2020 | 1200 - 1400

**Abstract:** Model abstraction of transistor-level circuits, while preserving an accurate behavior, is still an open problem. In this demo an approach is presented that automatically generates a hybrid automaton (HA) with linear states from an existing circuit netlist. The approach starts with a netlist at transistor level with full SPICE accuracy and ends at the system level description of the circuit in matlab or in Verilog-A. The resulting hybrid automaton exhibits linear behavior as well as the technology dependent nonlinear e.g. limiting behavior. The accuracy and speed-up of the Verilog-A generated models is evaluated based on several transistor level circuit abstractions of simple operational amplifiers up to a complex filters. Moreover, we verify the equivalence between the generated model and the original circuit. For the generated models in matlab syntax, a reachability analysis is performed using the reachability tool cora.
EUCLID-NIR GPU: AN ON-BOARD PROCESSING GPU-ACCELERATED SPACE CASE STUDY DEMONSTRATOR
Authors: Ivan Rodriguez and Leonidas Kosmidis
BSC / UPC, ES
Timeslots:
UB05.3 | Wednesday, 11 March 2020 | 1000 - 1200
Abstract: Embedded Graphics Processing Units (GPUs) are very attractive candidates for on-board payload processing of future space systems, thanks to their high performance and low-power consumption. Although there is significant interest from both academia and industry, there is no open and publicly available case study showing their capabilities, yet. In this master thesis project, which was performed within the GPU4S (GPU for Space) ESA-funded project, we have parallelised and ported the Euclid NIR (Near Infrared) image processing algorithm used in the European Space Agency’s (ESA) mission to be launched in 2022, to an automotive GPU platform, the NVIDIA Xavier. In the demo we will present in real-time its significantly higher performance achieved compared to the original sequential implementation. In addition, visitors will have the opportunity to examine the images on which the algorithm operates, as well as to inspect the algorithm parallelisation through profiling and code inspection.

FASTHERMSIM: FAST AND ACCURATE THERMAL SIMULATIONS FROM CHIPLETS TO SYSTEM
Authors: Yu-Min Lee, Chi-Wen Pan, Li-Rui Ho and Hong-Wen Chiou
National Chiao Tung University, TW
Timeslots:
UB01.5 | Tuesday, 10 March 2020 | 1030 - 1230
UB03.10 | Tuesday, 10 March 2020 | 1500 - 1730
UB08.8 | Wednesday, 11 March 2020 | 1600 - 1800
Abstract: Recently, owing to the scaling down of technology and 2.5D/3D integration, power densities and temperatures of chips have been increasing significantly. Though commercial computational fluid dynamics tools can provide accurate thermal maps, they may lead to inefficiency in thermal-aware design with huge runtime. Thus, we develop the chip/package/system-level thermal analyzer, called FasThermSim, which can assist you to improve your design under thermal constraints in pre/post-silicon stages. In FasThermSim, we consider three heat transfer modes, conduction, convection, and thermal radiation. We convert them to temperature-independent terms by linearization methods and build a compact thermal model (CTM). By applying numerical methods to the CTM, the steady-state and transient thermal profiles can be solved efficiently without loss of accuracy. Finally, an easy-to-use thermal analysis tool is implemented for your design, which is flexible and compatible, with the graphic user interface.

FLETCHER: TRANSPARENT GENERATION OF HARDWARE INTERFACES FOR ACCELERATING BIG DATA APPLICATIONS
Authors: Zaid Al-Ars, Johan Pettenburg, Jeroen van Straten, Matthijs Brobbel and Joost Hoozemans
TU Delft, NL
Timeslots:
UB02.1 | Tuesday, 10 March 2020 | 1230 - 1500
UB03.1 | Tuesday, 10 March 2020 | 1500 - 1730
UB04.1 | Tuesday, 10 March 2020 | 1730 - 1930
Abstract: This demo created by TUDelft is a software-hardware framework to allow for an efficient integration of FPGA hardware accelerators both on edge devices as well as in the cloud. The framework is called Fletcher, which is used to automatically generate data communication interfaces in hardware based on the widely used big data format Apache Arrow. This provides two distinct advantages. On the one hand, since the accelerators use the same data format as the software, data communication bottlenecks can be reduced. On the other hand, since a standardized data format is used, this allows for easy-to-use interfaces on the accelerator side, thereby reducing the design and development time. The demo shows how to use Fletcher for big data acceleration to decompress Snappy compressed files and perform filtering on the whole Wikipedia body of text. The demo enables 25 GB/s processing throughput.

FPGA-DSP: A PROTOTYPE FOR HIGH QUALITY DIGITAL AUDIO SIGNAL PROCESSING BASED ON AN FPGA
Authors: Bernhard Riess and Christian Epe
University of Applied Sciences Düsseldorf, DE
Timeslots:
UB02.4 | Tuesday, 10 March 2020 | 1230 - 1500
UB03.4 | Tuesday, 10 March 2020 | 1500 - 1730
Abstract: Our demonstrator presents a prototype of a new digital audio signal processing system which is based on an FPGA. It achieves a performance that up to now has been preserved to costly high-end solutions. Main components of the system are an analog/digital converter, an FPGA to perform the digital signal processing tasks, and a digital/analog converter implemented on a printed circuit board. To demonstrate the quality of the audio signal processing, infinite impulse response, finite impulse response filters and a delay effect were realized in VHDL. More advanced signal processing systems can easily be implemented due to the flexibility of the FPGA. Measured results were compared to state of the art audio signal processing systems with respect to size, performance and cost. Our prototype outperforms systems of the same price in quality, and outperforms systems of the same quality at a maximum of 20% of the price. Examples of the performance of our system can be heard in the demo.
FU: LOW POWER AND ACCURACY CONFIGURABLE APPROXIMATE ARITHMETIC UNITS
Authors: Tomoaki Ukezono and Toshinori Sato
Fukuoka University, JP
Timeslots:
UB05.10 | Wednesday, 11 March 2020 | 1000 - 1200
UB09.10 | Thursday, 12 March 2020 | 1000 - 1200
Abstract: In this demonstration, we will introduce the approximate arithmetic units such as adder, multiplier, and MAC that are being studied in our system-architecture laboratory. Our approximate arithmetic units can reduce delay and power consumption at the expense of accuracy. Our approximate arithmetic units are intended to be applied to IoT edge devices that can process images, and are suitable for battery-driven and low-cost devices. The biggest feature of our approximate arithmetic units is that the circuit is configured so that the accuracy is dynamically variable, and the trade-off relationship between accuracy and power can be selected according to the usage status of the device. In this demonstration, we show the power consumption according to various accuracy-requirements based on actual data and claim the practicality of the proposed arithmetic units.

FUZZING EMBEDDED BINARIES LEVERAGING SYSTEMC-BASED VIRTUAL PROTOTYPES
Authors: Vladimir Herdt¹, Daniel Grosse² and Rolf Drechsler²
¹DFKI, DE; ²University of Bremen/DFKI GmbH, DE
Timeslots:
UB01.1 | Tuesday, 10 March 2020 | 1030 - 1230
UB03.7 | Tuesday, 10 March 2020 | 1500 - 1730
Abstract: Verification of embedded Software (SW) binaries is very important. Mainly, simulation-based methods are employed that execute (randomly) generated test-cases on Virtual Prototypes (VPs). However, to enable a comprehensive VP-based verification, sophisticated test-case generation techniques need to be integrated. Our demonstrator combines state-of-the-art fuzzing techniques with SystemC-based VPs to enable a fast and accurate verification of embedded SW binaries. The fuzzing process is guided by the coverage of the embedded SW as well as the SystemC-based peripherals of the VP. The effectiveness of our approach is demonstrated by our experiments, using RISC-V SW binaries as an example.

GENERATING ASYNCHRONOUS CIRCUITS FROM CATAPULT
Authors: Yoan Decoudu¹, Jean Simatic², Katell Morin-Allory¹ and Laurent Fesquet¹
¹Université Grenoble Alpes, FR; ²HawAI.Tech, FR
Timeslots:
UB02.7 | Tuesday, 10 March 2020 | 1230 - 1500
UB06.7 | Wednesday, 11 March 2020 | 1200 - 1400
UB10.8 | Thursday, 12 March 2020 | 1200 - 1430
UB11.8 | Thursday, 12 March 2020 | 1430 - 1630
Abstract: In order to spread asynchronous circuit design to a large community of designers, High-Level Synthesis (HLS) is probably a good choice because it requires limited design technical skills. HLS usually provides an RTL description, which includes a data-path and a control-path. The desynchronization process is only applied to the control-path, which is a Finite State Machine (FSM). This method is sufficient to make asynchronous the circuit. Indeed, data are processed step by step in the pipeline stages, thanks to the desynchronized FSM. Thus, the data-path computation time is no longer related to the clock period but rather to the average time for processing data into the pipeline. This tends to improve speed when the pipeline stages are not well-balanced. Moreover, our approach helps to quickly designing data-driven circuits while maintaining a reasonable cost, a similar area and a short time-to-market.

INTACT: A 96-CORE PROCESSOR WITH 6 CHIPLETS 3D-STACKED ON AN ACTIVE INTERPOSER AND A 16-CORE PROTOTYPE RUNNING GRAPHICAL OPERATING SYSTEM
Authors: Eric Guthmuller¹,², Pascal Vivet¹,², César Fuguet¹,², Yvain Thonnart¹,², Gaël Pillonnet¹,³ and Fabien Clermidy¹,²
¹Université Grenoble Alpes; ²CEA List, FR; ³CEA-Leti, FR
Timeslots:
UB01.6 | Tuesday, 10 March 2020 | 1030 - 1230
UB02.6 | Tuesday, 10 March 2020 | 1230 - 1500
Abstract: We built a demonstrator for our 96-cores cache coherent 3D processor and a first prototype featuring 16 cores. The demonstrator consists in our 16-cores processor running commodity operating systems such as Linux and NetBSD on a PC-like motherboard with user-friendly devices such as a HDMI display, keyboard and mouse. A graphical desktop is displayed, and the user will interact with it through the keyboard and mouse. The demonstrator is able to run parallel applications to benchmark its performance in terms of scalability. The main innovation of our processor is its scalable cache coherent architecture based on distributed L2-caches and adaptive L3-caches. Additionally, the energy consumption is also measured and displayed by reading dynamically from the monitors of power-supply devices. Finally we will also show open packages of the 3D processor featuring 6 16-core chiplets (28 nm FDSOI) on an active interposer (65 nm) embedding Network-on-Chips, power management and IO controllers.
JOINTER: JOINING FLEXIBLE MONITORS WITH HETEROGENEOUS ARCHITECTURES

Authors: Giacomo Valente¹, Tiziana Fanni², Carlo Sau³, Claudio Rubattu², Francesca Palumbo² and Luigi Pomante¹

¹Università degli Studi dell’Aquila, IT; ²Università degli Studi di Sassari, IT; ³Università degli Studi di Cagliari, IT

Timeslots:
UB01.10 | Tuesday, 10 March 2020 | 1030 - 1230
UB02.10 | Tuesday, 10 March 2020 | 1230 - 1500
UB06.10 | Wednesday, 11 March 2020 | 1200 - 1400

Abstract: As embedded systems grow more complex and shift toward heterogeneous architectures, understanding workload performance characteristics becomes increasingly difficult. In this regard, run-time monitoring systems can support on obtaining the desired visibility to characterize a system. This demo presents a framework that allows to develop complex heterogeneous architectures composed of programmable processors and dedicated accelerators on FPGA, together with customizable monitoring systems, keeping under control the introduced overhead. The whole development flow (and related prototypical EDA tools), that starts with the accelerators creation using a data-flow model, in parallel with the monitoring system customization using a library of elements, showing also the final joining, will be shown. Moreover, a comparison among different monitoring systems functionalities on different architectures developed on Zynq7000 SoC will be illustrated.

LAGARTO: FIRST SILICON RISC-V ACADEMIC PROCESSOR DEVELOPED IN SPAIN

Authors: Guillem Cabo Pitarch¹, Cristobal Ramirez Lazo¹, Julian Pavon Rivera¹, Vatistas Kostalabros¹, Carlos Rojas Morales¹, Miquel Moreto¹, Jaume Abella¹, Francisco J. Cazorla¹, Adrian Cristal¹, Roger Figuera¹, Alberto Gonzalez¹, Carles Hernandez¹, Cesar Hernandez², Neiel Leyva³, Joan Marimon¹, Ricardo Martinez³, Jonnatan Mendoza¹, Francesc Moll², Marco Antonio Ramirez², Carlos Rojas¹, Antonio Rubio⁴, Abraham Ruiz¹, Nehir Sonmez¹, Lluis Teres³, Osman Unsal⁵, Mateo Valero¹, Ivan Vargas¹ and Luis Villa²

¹BSC/ UPC, ES; ²CIC-IPN, MX; ³IMB-CNM (CSIC), ES; ⁴UPC, ES; ⁵BSC, ES

Timeslots:
UB01.3 | Tuesday, 10 March 2020 | 1030 - 1230
UB04.4 | Tuesday, 10 March 2020 | 1730 - 1930
UB08.1 | Wednesday, 11 March 2020 | 1600 - 1800
UB10.5 | Thursday, 12 March 2020 | 1200 - 1430
UB11.5 | Thursday, 12 March 2020 | 1430 - 1630

Abstract: Open hardware is a possibility that has emerged in recent years and has the potential to be as disruptive as Linux was once, an open source software paradigm. If Linux managed to lessen the dependence of users in large companies providing software and software applications, it is envisioned that hardware based on ISAs open source can do the same in their own field. In the Lagarto tapeout four research institutions were involved: Centro de Investigación en Computación of the Mexican IPN, Centro Nacional de Microelectrónica of the CSIC, Universitat Politècnica de Catalunya (UPC) and Barcelona Supercomputing Center (BSC). As a result, many bachelor, master and PhD students had the chance to achieve real-world experience with ASIC design and achieve a functional SoC. In the booth, you will find a live demo of the first ASIC and prototypes running on FPGA of the next versions of the SoC and core.
LEARNV: A RISC-V BASED EMBEDDED SYSTEM DESIGN FRAMEWORK FOR EDUCATION AND RESEARCH DEVELOPMENT

Authors: Noureddine Ait Said and Mounir Benabdenbi
TIMA Laboratory, FR

Timeslots:
UB03.5 | Tuesday, 10 March 2020 | 1500 - 1730
UB04.5 | Tuesday, 10 March 2020 | 1730 - 1930
UB06.8 | Wednesday, 11 March 2020 | 1200 - 1400
UB08.5 | Wednesday, 11 March 2020 | 1600 - 1800
UB11.7 | Thursday, 12 March 2020 | 1430 - 1630

Abstract: Designing a modern System on a Chip is based on the joint design of hardware and software (co-design). However, understanding the tight relationship between hardware and software is not straightforward. Moreover to validate new concepts in SoC design from the idea to the hardware implementation is time-consuming and often slowed by legacy issues (intellectual property of hardware blocks and expensive commercial tools). To overcome these issues we propose to use the open-source Rocket Chip environment for educational purposes, combined with the open-source LowRisc architecture to implement a custom SoC design on an FPGA board. The demonstration will present how students and engineers can take benefit from the environment to deepen their knowledge in HW and SW co-design. Using the LowRisc architecture, an image classification application based on the use of CNNs will serve as a demonstrator of the whole open-source hardware and software flow and will be mapped on a Nexys A7 FPGA board.

MDD-COP: A PRELIMINARY TOOL FOR MODEL-DRIVEN DEVELOPMENT EXTENDED WITH LAYER DIAGRAM FOR CONTEXT-ORIENTED PROGRAMMING

Authors: Harumi Watanabe1, Chinatsu Yamamoto1, Takeshi Ohkawa1, Mikiko Sato1, Nobuhiko Ogura2 and Mana Tabei1
1Tokai University, JP; 2Tokyo City University, JP

Timeslots:
UB07.10 | Wednesday, 11 March 2020 | 1400 - 1600
UB08.10 | Wednesday, 11 March 2020 | 1600 - 1800

Abstract: This presentation introduces a preliminary tool for Model-Driven development (MDD) to generate programs for Context-Oriented Programming (COP). In modern embedded systems such as IoT and Industry 4.0, their software began to process multiple services by following the changing surrounding environments. COP is helpful for programming such software. In COP, we can consider the surrounding environments and multiple services as contexts and layers. Even though MDD is a powerful technique for developing such modern systems, the works of modeling for COP are limited. There are no works to mention the relation between UML (Unified Modeling Language) and COP. To solve this problem, we provide a COP generation from a layer diagram extended the package diagram of UML by stereotypes. In our approach, users draw a layer diagram and other UML diagrams, then xtUML, which is a major tool of MDD, generates XML code with layer information for COP; finally, our tool generates COP code from XML code.

PA-HLS: HIGH-LEVEL ANNOTATION OF ROUTING CONGESTION FOR XILINX VIVADO HLS DESIGNS

Authors: Osama Bin Tariq1, Junnan Shan1, Luciano Lavagno1, Georgios Floros2, Mihai Teodor Lazarescu1, Christos Sotiriou2 and Mario Roberto Casu1
1Politecnico di Torino, IT; 2University of Thessaly, GR

Timeslots:
UB07.9 | Wednesday, 11 March 2020 | 1400 - 1600
UB08.9 | Wednesday, 11 March 2020 | 1600 - 1800
UB09.9 | Thursday, 12 March 2020 | 1000 - 1200
UB10.9 | Thursday, 12 March 2020 | 1200 - 1430

Abstract: We will demo a novel high-level backannotation flow that reports routing congestion issues at the C++ source level by analyzing reports from FPGA physical design (Xilinx Vivado) and internal debugging files of the Vivado HLS tool. The flow annotates the C++ source code, identifying likely causes of congestion, e.g., on-chip memories or the DSP units. These shared resources often cause routing problems on FPGAs because they cannot be duplicated by physical design. We demonstrate on realistic large designs how the information provided by our flow can be used to both identify congestion issues at the C++ source level and solve them using HLS directives. The main demo steps are: 1-Extraction of the source-level debugging information from the Vivado HLS database 2-Generation of a list of net names involved in congestion areas and of their relative significance from the Vivado post global-routing database 3-Visualization of the C++ code lines that contribute most to congestion.
PAFUSI: PARTICLE FILTER FUSION ASIC FOR INDOOR POSITIONING

Authors: Christian Schott, Marko Rößler, Daniel Froß, Marcel Putsche and Ulrich Heinkel
TU Chemnitz, DE

Timeslots:
UB03.3 | Tuesday, 10 March 2020 | 1500 - 1730
UB09.3 | Thursday, 12 March 2020 | 1000 - 1200

Abstract: The meaning of data acquired from IoT devices is heavily enhanced if global or local position information of their acquirement is known. Infrastructure for indoor positioning as well as the IoT device involve the need of small, energy efficient but powerful devices that provide the location awareness. We propose the PAFUSI, a hardware implementation of an UWB position estimation algorithm that fulfills these requirements. Our design fuses distance measurements to fixed points in an environment to calculate the position in 3D space and is capable of using different positioning technologies like GPS, DecaWave or Nanotron as data source simultaneously. Our design comprises of an estimator which processes the data by means of a Sequential Monte Carlo method and a microcontroller core which configures and controls the measurement unit as well as it analyses the results of the estimator. The PAFUSI is manufactured as a monolithic integrated ASIC in a multi-project wafer in UMC’s 65nm process.

PARALLEL ALGORITHM FOR CNN INFEERENCE AND ITS AUTOMATIC SYNTHESIS

Authors: Takashi Matsumoto, Yukio Miyasaka, Xinpei Zhang and Masahiro Fujita
University of Tokyo, JP

Timeslots:
UB01.4 | Tuesday, 10 March 2020 | 1030 - 1230
UB05.9 | Wednesday, 11 March 2020 | 1000 - 1200
UB09.6 | Thursday, 12 March 2020 | 1000 - 1200

Abstract: Recently, Convolutional Neural Network (CNN) has surpassed conventional methods in the field of image processing. This demonstration shows a new algorithm to calculate CNN inference using processing elements arranged and connected based on the topology of the convolution. They are connected in mesh and calculate CNN inference in a systolic way. The algorithm performs the convolution of all elements with the same output feature in parallel. We demonstrate a method to automatically synthesize an algorithm, which simultaneously performs the convolution and the communication of pixels for the computation of the next layer. We show with several sizes of input layers, kernels, and strides and confirmed that the correct algorithms were synthesized. The synthesis method is extended to the sparse kernel. The synthesized algorithm requires fewer cycles than the original algorithm. There were the more chances to reduce the number of cycles with the sparser kernel.

PRE-IMPACT FALL DETECTION ARCHITECTURE BASED ON NEUROMUSCULAR CONNECTIVITY STATISTICS

Authors: Giovanni Mezzina, Sardar Mehboob Hussain and Daniela De Venuto
Politecnico di Bari, IT

Timeslots:
UB01.9 | Tuesday, 10 March 2020 | 1030 - 1230
UB02.9 | Tuesday, 10 March 2020 | 1230 - 1500

Abstract: In this demonstration, we propose an innovative multi-sensor architecture operating in the field of pre-impact fall detection (PIFD). The proposed architecture jointly analyzes cortical and muscular involvement when unexpected slippages occur during steady walking. The EEG and EMG are acquired through wearable and wireless devices. The control unit consists of an STM32L4 microcontroller and a Simulink modeling. The µC implements the EMG computation, while the cortical analysis and the final classification were entrusted to the Simulink model. The EMG computation block translates EMGs into binary signals, which are used both to enable cortical analyses and to extract a score to distinguish “standard” muscular behaviors from anomalous ones. The Simulink model evaluates the cortical responsiveness in five bands of interest and implements the logical-based network classifier. The system, tested on 6 healthy subjects, shows an accuracy of 96.21% and a detection time of ~371 ms.
RESCUED: A RESCUE DEMONSTRATOR FOR INTERDEPENDENT ASPECTS OF RELIABILITY, SECURITY AND QUALITY TOWARDS A COMPLETE EDA FLOW

Authors: Nevin George¹, Guilherme Cardoso Medeiros², Junchao Chen³, Josie Esteban Rodriguez Condia⁴, Thomas Lange⁵, Aleksa Damjanovic⁶, Raphael Segabinazzi Ferreira¹, Aneesh Balakrishnan⁶, Xinhui Lai⁷, Shayesteh Masoumian⁷, Dmytro Petryk⁵, Troya Cagil Koylu³, Felipe Augusto da Silva⁸, Ahmet Cagil Bagbaba³, Cemil Cem Gürsoy³, Said Hamdioui⁵, Mottagiallah Taouil⁵, Milos Krstic⁶, Peter Langendoerfer⁵, Zoya Dyka³, Marcelo Brandalero¹, Michael Hübner¹, Jörg Nolte¹, Heinrich Theodor Vierhaus¹, Matteo Sonza Reorda¹, Giovanni Squillero⁴, Luca Sterpone³, Jaan Raik⁶, Dan Alexandrescu⁸, Maximilian Glorieux⁵, Georgios Selimis⁷, Geert-Jan Schrijen⁷, Anton Klotz⁸, Christian Sauer⁸ and Maksim Jenihhin⁶

¹Brandenburg University of Technology Cottbus-Senftenberg, DE; ²TU Delft, NL; ³Leibniz-Institut für innovative Mikroelektronik, DE; ⁴Politecnico di Torino, IT; ⁵IROC Technologies, FR; ⁶Tallinn University of Technology, EE; ⁷Intrinsic ID, NL; ⁸Cadence Design Systems GmbH, DE

Timeslots:
UB09.2 | Thursday, 12 March 2020 | 1000 - 1200
UB10.2 | Thursday, 12 March 2020 | 1200 - 1430

Abstract: The demonstrator highlights the various interdependent aspects of Reliability, Security and Quality in nanoelectronics system design within an EDA toolset and a processor architecture setup. The compelling need of attention towards these three aspects of nanoelectronic systems have been ever more pronounced over extreme miniaturization of technologies. Further, such systems have exploded in numbers with IoT devices, heavy and analogous interaction with the external physical world, complex safety-critical applications, and Artificial intelligence applications. RESCUE targets such aspects in the form, Reliability (functional safety, ageing, soft errors), Security (tamper-resistance, PUF technology, intelligent security) and Quality (novel fault models, functional test, FMEA/FMECA, verification/debug) spanning the entire hardware software system stack. The demonstrator is brought together by a group of PhD students under the banner of H2020-MSCA-ITN RESCUE European Union project.

RETINE: A PROGRAMMABLE 3D STACKED VISION CHIP ENABLING LOW LATENCY IMAGE ANALYSIS

Authors: Stéphane Chevobbe¹, Maria Lepecq¹ and Laurent Millet²

¹CEA LIST, FR; ²CEA-Leti, FR

Timeslots:
UB07.4 | Wednesday, 11 March 2020 | 1400 - 1600
UB08.7 | Wednesday, 11 March 2020 | 1600 - 1800
UB10.3 | Thursday, 12 March 2020 | 1200 - 1430

Abstract: We have developed and fabricated a 3D stacked imager called RETINE composed with 2 layers based on the replication of a programmable 3D tile in a matrix manner providing a highly parallel programmable architecture. This tile is composed by a 16x16 BSI binned pixels array with associated readout and 16 column ADC on the first layer coupled to an efficient SIMD processor of 16 PE on the second layer. The prototype of RETINE achieves high video rates, from 5500 fps in binned mode to 340 fps in full resolution mode. It operates at 80 MHz with 720 mW power consumption leading to 85 GOPS/W power efficiency. To highlight the capabilities of the RETINE chip we have developed a demonstration platform with an electronic board embedding a RETINE chip that films rotating disks. Three scenarios are available: high speed image capture, slow motion and composed image capture with parallel processing during acquisition.

RUMORE: A FRAMEWORK FOR RUNTIME MONITORING AND TRACE ANALYSIS FOR COMPONENT-BASED EMBEDDED SYSTEMS DESIGN FLOW

Authors: Vittoriano Muttillo¹, Luigi Pomante¹, Giacomo Valente¹, Hector Posadas², Javier Merino² and Eugenio Villar²

¹Università degli Studi dell’Aquila, IT; ²University of Cantabria, ES

Timeslots:
UB03.9 | Tuesday, 10 March 2020 | 1500 - 1730
UB04.9 | Tuesday, 10 March 2020 | 1730 - 1930
UB11.9 | Thursday, 12 March 2020 | 1430 - 1630

Abstract: The purpose of this demonstrator is to introduce runtime monitoring infrastructures and to analyze trace data. The goal is to show the concept among different monitoring requirements by defining a general reference architecture that can be adapted to different scenarios. Starting from design artifacts, generated by a system engineering modeling tool, a custom HW monitoring system infrastructure will be presented. This sub-system will be able to generate runtime artifacts for runtime verification. We will show how the RUMORE framework provides round-trip support in the development chain, injecting monitoring requirements from design models down to code and its execution on the platform and trace data back to the models, where the expected behavior will then compared with the actual behavior. This approach will be used towards optimizing design models for specific properties (e.g., for system performance).
SKELETOR: AN OPEN SOURCE EDA TOOL FLOW FROM HIERARCHY SPECIFICATION TO HDL DEVELOPMENT

**Authors:** Ivan Rodriguez, Guillem Cabo, Javier Barrera, Jeremy Giesen, Alvaro Jover and Leonidas Kosmidis

BSC/ UPC, ES

**Timeslots:**
- UB01.2 | Tuesday, 10 March 2020 | 1030 - 1230
- UB09.4 | Thursday, 12 March 2020 | 1000 - 1200

**Abstract:** Large hardware design projects have high overhead for project bootstrapping, requiring significant effort for translating hardware specifications to hardware design language (HDL) files and setting up their corresponding development and verification infrastructure. Skeletor (https://github.com/jaquerinte/Skeletor) is an open source EDA tool developed as a student project at UPC/BSC, which simplifies this process, by increasing developer’s productivity and reducing typing errors, while at the same time lowers the bar for entry in hardware development. Skeletor uses a C/verilog-like language for the specification of the modules in a hardware project hierarchy and their connections, which is used to generate automatically the required skeleton of source files, their development and verification testbenches and simulation scripts. Integration with KiCad schematics and support for syntax highlighting in code editors simplifies further its use. This demo is linked with workshop W05.

SRSN: SECURE RECONFIGURABLE TEST NETWORK

**Authors:** Vincent Reynaud\(^1\), Emanuele Valea\(^2\), Paolo Maistri\(^1\), Regis Leveugle\(^1\), Marie-Lise Flottes\(^2\), Sophie Dupuis\(^2\), Bruno Rouzeyle\(^2\) and Giorgio Di Natale\(^1\)

\(^1\)TIMA Laboratory, FR; \(^2\)LIRMM, FR

**Timeslots:**
- UB04.3 | Tuesday, 10 March 2020 | 1730 - 1930
- UB06.6 | Wednesday, 11 March 2020 | 1200 - 1400
- UB08.6 | Wednesday, 11 March 2020 | 1600 - 1800
- UB10.6 | Thursday, 12 March 2020 | 1200 - 1430
- UB11.6 | Thursday, 12 March 2020 | 1430 - 1630

**Abstract:** The critical importance of testability for electronic devices led to the development of IEEE test standards. These methods, if not protected, offer a security backdoor to attackers. This demonstrator illustrates a state-of-the-art solution that prevents unauthorized usage of the test infrastructure based on the IEEE 1687 standard and implemented on an FPGA target.

SUBRISC+: IMPLEMENTATION AND EVALUATION OF AN EMBEDDED PROCESSOR FOR LIGHTWEIGHT IOT EHEALTH

**Authors:** Mingyu Yang and Yuko Hara-Azumi

Tokyo Institute of Technology, JP

**Timeslots:**
- UB07.8 | Wednesday, 11 March 2020 | 1400 - 1600
- UB09.8 | Thursday, 12 March 2020 | 1000 - 1200

**Abstract:** Although the rapid growth of Internet of Things (IoT) has enabled new opportunities for eHealth devices, the further development of complex systems is severely constrained by the power and energy supply on the battery-powered embedded systems. To address this issue, this work presents a processor design called “SubRISC+” targeting lightweight IoT eHealth. SubRISC+ is a processor design to achieve low power/energy consumption through its unique and compact architecture. As an example of lightweight eHealth applications on SubRISC+, we are working on the epileptic seizure detection using the dynamic time wrapping algorithm to deploy on wearable IoT eHealth devices. Simulation results show that 22% reduction on dynamic power and 50% reduction on leakage power and core area are achieved compared to Cortex-M0. As an ongoing work, the evaluation on a fabricated chip will be done within the first half of 2020.

SYSTEMC-CT/DE: A SIMULATOR WITH FAST AND ACCURATE CONTINUOUS TIME AND DISCRETE EVENTS INTERACTIONS ON TOP OF SYSTEMC.

**Authors:** Breytner Joseph Fernandez-Mesa, Liliana Andrade and Frédéric Pétrot

Université Grenoble Alpes / CNRS / TIMA Laboratory, FR

**Timeslots:**
- UB06.4 | Wednesday, 11 March 2020 | 1200 - 1400
- UB09.5 | Thursday, 12 March 2020 | 1000 - 1200

**Abstract:** We have developed a continuous time (CT) and discrete events (DE) simulator on top of SystemC. Systems that mix both domains are critical and their proper functioning must be verified. Simulation serves to achieve this goal. Our simulator implements direct CT/DE synchronization, which enables a rich set of interactions between the domains: events from the CT models are able to trigger DE processes; events from the DE models are able to modify the CT equations. DE-based interactions are, then, simulated at their precise time by the DE kernel rather than at fixed time steps. We demonstrate our simulator by executing a set of challenging examples: they either require a superdense model of time or include Zeno behavior or are highly sensitive to accuracy errors. Results show that our simulator overcomes these issues, is accurate, and improves simulation speed w.r.t. fixed time steps; all of these advantages open up new possibilities for the design of a wider set of heterogeneous systems.
**TAPASCO: THE OPEN-SOURCE TASK-PARALLEL SYSTEM COMPOSER FRAMEWORK**

**Authors:** Carsten Heinz, Lukas Sommer, Lukas Weber, Jaco Hofmann and Andreas Koch
TU Darmstadt, DE

**Timeslots:**
UB05.1 | Wednesday, 11 March 2020 | 1000 - 1200
UB09.1 | Thursday, 12 March 2020 | 1000 - 1200
UB10.1 | Thursday, 12 March 2020 | 1200 - 1430

**Abstract:** Field-programmable gate arrays (FPGA) are an established platform for highly specialized accelerators, but in a heterogeneous setup, the accelerator still needs to be integrated into the overall system. The open-source TaPaSCo (Task-Parallel System Composer) framework was created to serve this purpose: The fast integration of FPGA-based accelerators into compute platforms or systems-on-chip (SoC) and their connection to relevant components on the FPGA board. TaPaSCo can support developers in all steps of the development process: from cores resulting from High-Level Synthesis or cores written in an HDL, a complete FPGA-design can be created. TaPaSCo will automatically connect all processing elements to the memory- and host-interface and generate a complete bitstream. The TaPaSCo Runtime API allows to interface with accelerators from software and supports operations such as transferring data to the FPGA memory, passing values and controlling the execution of the accelerators.

**UWB ACKATCK: HIJACKING DEVICES IN UWB INDOOR POSITIONING SYSTEMS**

**Authors:** Baptiste Pestourie, Vincent Beroulle and Nicolas Fourty
Université Grenoble Alpes, FR

**Timeslots:**
UB05.5 | Wednesday, 11 March 2020 | 1000 - 1200
UB07.5 | Wednesday, 11 March 2020 | 1400 - 1600

**Abstract:** Various radio-based Indoor Positioning Systems (IPS) have been proposed during the last decade as solutions to GPS inconsistency in indoor environments. Among the different radio technologies proposed for this purpose, 802.15.4 Ultra-Wideband (UWB) is by far the most performant, reaching up to 10 cm accuracy with 1000 Hz refresh rates. As a consequence, UWB is a popular technology for applications such as assets tracking in industrial environments or robots/drones indoor navigation. However, some security flaws in 802.15.4 standard expose UWB positioning to attacks. In this demonstration, we show how an attacker can exploit a vulnerability on 802.15.4 acknowledgment frames to hijack a device in a UWB positioning system. We demonstrate that using simply one cheap UWB chip, the attacker can take control over the positioning system and generate fake trajectories from a laptop. The results are observed in real-time in the 3D engine monitoring the positioning system.

**VIRTUAL PLATFORMS FOR COMPLEX SOFTWARE STACKS**

**Authors:** Lukas Jünger and Rainer Leupers
RWTH Aachen University, DE

**Timeslots:**
UB02.3 | Tuesday, 10 March 2020 | 1230 - 1500
UB06.3 | Wednesday, 11 March 2020 | 1200 - 1400

**Abstract:** This demonstration is going to showcase our “AVP64” Virtual Platform (VP), which models a multi-core ARMv8 (Cortex A72) system including several peripherals, such as an SDHCI and an ethernet controller. For the ARMv8 instruction set simulation a dynamic binary translation based solution is used. As the workload, the Xen hypervisor with two Linux Virtual Machines (VMs) is executed. Both VMs are connected to the simulation hosts’ network subsystem via a virtual ethernet controller. One of the VMs executes a NodeJS-based server application offering a REST API via this network connection. An AngularJS client application on the host system can then connect to the server application to obtain and store data via the server’s REST API. This data is read and written by the server application to the virtual SD Card connected to the SDHCI. For this, one SD card partition is passed to the VM through Xen’s block device virtualization mechanism.

**WALLANCE: AN ALTERNATIVE TO BLOCKCHAIN FOR IOT**

**Authors:** Loic Dalmasso, Florent Bruguier, Pascal Benoit and Achraf Lamlihi
Université de Montpellier, FR

**Timeslots:**
UB02.8 | Tuesday, 10 March 2020 | 1230 - 1500
UB03.8 | Tuesday, 10 March 2020 | 1500 - 1730
UB04.8 | Tuesday, 10 March 2020 | 1730 - 1930
UB06.9 | Wednesday, 11 March 2020 | 1200 - 1400

**Abstract:** Since the expansion of the Internet of Things (IoT), connected devices became smart and autonomous. Their exponentially increasing number and their use in many application domains result in a huge potential of cybersecurity threats. Taking into account the evolution of the IoT, security and interoperability are the main challenges, to ensure the reliability of the information. The blockchain technology provides a new approach to handle the trust in a decentralized network. However, current blockchain implementations cannot be used in IoT domain because of their huge need of computing power and storage utilization. This demonstrator presents a lightweight distributed ledger protocol dedicated to the IoT application, reducing the computing power and storage utilization, handling the scalability and ensuring the reliability of information.

See you at the University Booth!

University Booth Co-Chairs
Frédéric Pétrot, IMAG, FR and Andreas Vörg, edacentrum, DE
university-booth@date-conference.com
Despite the slowdown of Moore’s Law, applications from machine learning and edge computing to scientific computing and mobile computing continuously demand more performance under tighter cost, energy, and size constraints. Silicon-based photonic technologies advanced rapidly in the last two decades and have become promising solutions to complement electronic technologies. OPTICS (optical/photonic interconnects for computing systems) workshop aims at discussing the latest advances in optics/photronics for computing systems, covering topics from fabrications, photonic devices, photonic circuits, architectures, system integrations, and design automation and optimization. The workshop targets researchers and engineers working on optics/photronics, electronics, architectures, systems, applications and design automations.

Topics to be discussed include but are not limited to:

- PEDa (Photonic-Electronic Design Automation): layout, placement and routing, floorplan, crosstalk, thermal, process variation, etc.
- Photonic-electronic system integration and application: data center, HPC, automobile, aviation, etc.
- Photonics-based architecture: optical neural network, rack-scale optical network, inter/intra-chip optical network, optical switching, etc.
- Photonic/optic circuits: OE conversion, optical interconnect, optical computing circuit, etc.
- Photonic device and fabrication: laser, photodetector, modulator, switch, filter, etc.
FRIDAY WORKSHOPS

0830–0840 Introduction to OPTICS
0840–0940 [Keynote] Silicon photonics design for new computing paradigms: neuromorphic and quantum computing
   Speaker: Lukas Chrostowski, University of British Columbia, CA
0940–1000 Moving photonics design light-years ahead: optimizing photonic components for manufacturability with inverse design
   Speaker: Geoff Duggan, Lumerical, GB

1000–1030 Coffee Break

1030–1050 Tolerating errors in nanophotonic interconnects for a better energy efficiency
   Speaker: Cédric Killian, INRIA Rennes, FR
1050–1110 Automatic Topology Generation and Bandwidth Optimization for Wavelength-Routed Optical Networks-on-Chips
   Speaker: Ulf Schlichtmann, TU Munich, DE
1110–1130 Specification-driven photonics circuit design
   Speaker: Ruping Cao, Luceda, BE
1130–1150 Machine learning for smart silicon photonic spectrometers
   Speaker: Carlos Ramos, C2N, FR
1150–1200 Poster presentations

1200–1300 Lunch Break in Salon des Médaillés

1300–1320 Neuromorphic Photonic Architectures
   Speaker: George Dabos, Aristotle University of Thessaloniki, GR
1320–1340 An Optical Neural Network Architecture based on Light Speed Approximate Parallel Multipliers
   Speaker: Jun Shiom, Kyoto University, JP
1340–1400 Driving photonic implementation through automation
   Speaker: Tom Daspit, Mentor Graphics, US
1400–1420 From Photonic Integration to Electronic-Photonic Heterogeneouslyconverging IC with Applications to Optical/Photonic Interconnects
   Speaker: Min Tan, Huazhong University of Science and Technology, CN
1420–1430 Poster presentations
1430–1500 Coffee Break

1500–1520 CMOS integrated silicon ring modulators for photonic interconnects: the future of HPC
   Speaker: Derek Van Orden, Ayar Labs, US
1520–1540 Optical Integration in Data centers and high performance computers, going beyond moore’s law
   Speaker: Liron Gantz, Mellanox, US
1540–1600 Optical Circuit Switching and Control for Heterogeneous and Disaggregated Data Centres
   Speaker: Georgios Zervas, University College London, GB
1600–1620 Silicon Photonics in Memory Hard Systems
   Speaker: Alan Mickelson, University of Colorado Boulder, US
1620–1640 Invited Talk
1640–1730 Panel
1730 Closing remarks

W02 COMPUTATION-IN-MEMORY (CIM): FROM DEVICE TO APPLICATIONS

BERLIOZ 0830 – 1730

General Co-Chairs
Said Hamdioui, TU Delft, NL
Alberto Bosio, Lyon Institute of Nanotechnology, FR
Programme Chair: Elena Ioana Vatajelu, TIMA, FR

Webpage: http://perso.ec-lyon.fr/alberto.bosio/CIMW

All issues with which the architectures and technologies are face today have led to the slowdown of the traditional device scaling. In order for computing systems to continue deliver sustainable benefits for the foreseeable future, alternative computing architectures and notions have to be explored in the light of emerging new device technologies. This workshop aims at providing a forum to discuss Computation-in-Memory (as an alternative architecture) in the light of emerging non-volatile devices (such as RRAM, PCM and STT-MRAM), and its potential applications. It also aims at reinforcing the CIM community and at offering a holistic vision of this emerging computing paradigm to the electronic design, automation and test communities.

The workshop covers all aspects of CIM based on non-volatile devices including (but not limited to):

- Device and technology: physics and modeling, device technologies, device characterization.
- Novel logic and circuit design concepts using NV devices: Boolean logic, threshold logic, arithmetic circuits, multi-level based logic, memories, PUF technology, TRNG design.
- System architectures and new computing paradigms: resistive computing, neuro-inspired computing, novel architectures and CMOS integration, cellular automata and array computing.
- Applications exploiting NV devices: signal processing, chaos and complex networks, sensors applications, AI applications.
- Automation and CAD tools: mapping tools, compilers, logic synthesis tools, design space exploration tools.
- Test and Reliability: test and reliability solutions for circuits and architectures.
0830–0930 OPENING SESSION & KEYNOTE ADDRESS
   Opening Session
   Speakers:
   Alberto Bosio, Lyon Institute of Nanotechnology, FR
   Said Hamdioui, TU Delft, NL
   Elena-Ioana Vatajelu, TIMA, FR
   Keynote Address
0930–1000 INVITED TALK
1000–1030 Coffee Break
1030–1200 PANEL COMPUTATION-IN-MEMORY (CIM): FROM DEVICE TO APPLICATIONS
   Panel Chair: Ian O’Connor, INL, FR
   Panellists:
   Henri-Pierre Charles, CEA-Leti, FR
   Shahar Kvatinsky, Technion, IL
   Alexandre Levisse, EPFL, CH
   Georgios Sirakoulis, University of Thrace, GR
1200–1300 Lunch Break in Salon des Médaillés
1300–1430 SESSION SCIENTIFIC PRESENTATIONS
   Impact of On-Chip Interconnect on In-Memory Acceleration of Deep Neural Networks
   Authors: Gokul Krishnan*, Sumit K. Mandal*, Chaitali Chakrabarti, Jae-sun Seo, Umit Y. Ogras, Yu Cao
   School of Electrical, Computer and Energy Engineering, Arizona State University, US
   Conversion-in-Memory Using Floating-Gate Memristive Neural Networks
   Authors: Loai Danial, Shahar Kvatinsky
   Viterbi Faculty of Electrical Engineering, Technion - Israel Institute of Technology, IL
   Exact Stochastic Computing Multiplication in Memristive Memory
   Authors: Mohsen Riahi Alam¹, M. Hassan Najafi¹, Nima TaheriNajad²
   ¹University of Louisiana at Lafayette, US; ²TU Wien, AT
   Efficient 8-bit matrix multiplication on Computational SRAM architecture
   Authors: Mambu Kévin, Charles Henri-Pierre, Kooli Maha
   Université Grenoble Alpes, CEA LIST, FR
1430–1500 Coffee Break
1500–1730 SESSION SCIENTIFIC PRESENTATIONS
   Simulation and experimental characterization of memristive crossbar arrays for computation-in-memory
   Authors: J. Mohr, C. Bengel, M. Abu, S. Hamdioui, D.J. Wouters, S. Menzel, R. Waser
   Sensing and Processing in Memristive Arrays
   Authors: Saurabh Khandelwal¹, Shahar Kvatinsky², Marco Ottavi², Eugenio Martinelli², Abusaleh Jabir¹
   ¹School of ECM, Oxford Brookes University, GB; ²Viterbi Faculty of Electrical Engg., Technion - Israel Institute of Technology, IL
   Exploration of a Scalable Vector-Tile-based In-Memory Computing Architecture
   Authors: Roman Gauchi¹, Valentin Egloff¹, Maha Kooli¹, Jean-Philippe Noel¹, Bastien Giraud¹, Pascal Vivet¹, Subhasish Mitra², Henri-Pierre Charles¹
   ¹Université Grenoble Alpes, CEA LIST, FR; ²Stanford University, US
   Reuse-aware architecture and synthesis flow for NVM-based FPGAs
   Authors: João Paulo Cardoso de Lima, Rafael Fão de Moura, Luigi Carro
   Departamento de Informática Aplicada Instituto de Informática – UFRGS, BR
   Toward CIM architecture with a new tile-level simulator
   Authors: Mahdi Zahedi, Stephan Wong, Said Hamdioui
   Computer Engineering Laboratory, Delft University of Technology, NL
FRIDAY WORKSHOPS

W03  SECOND DATE WORKSHOP ON AUTONOMOUS SYSTEMS DESIGN (ASD 2020)  CHAMROUSSE  0830 – 1730
Organisers
Sebastian Steinhorst, Technical University of Munich, DE
Jyotirmoy Deshmukh, University of Southern California, US

Webpage: http://asd.userweb.mwn.de/workshop.html

ASD 2020 is the 2nd international workshop on Autonomous Systems Design. It is part of a two-day special initiative at DATE on Autonomous Systems Design. The goal of the workshop is to explore recent industrial and academic methods and methodologies in autonomous systems design.

0830–0845 Opening Remarks
Organisers:
Sebastian Steinhorst, Technical University of Munich, DE
Jyotirmoy Deshmukh, University of Southern California, US

0845–0930 Keynote “Autonomy: one step beyond on commercial aviation”
Speaker: Pascal Traverse, Airbus, FR

0930–1000 Introduction to Demos

- UNICARagil project
- Mathworks
- Alexandre Donzé (Decyphir): Breach
- Philipp Weiβ (Technical University of Munich): Fail-operational Automotive Software
- Christian Laugier (INRIA Grenoble): Autonomous Driving Demonstration: Focus on the Embedded Bayesian Perception component
- Andy Pimentel (University of Amsterdams), Martina Maggio (Lund University), Juan Valverde (United Technology Research Center): Autonomous Adaption and Morphing of Embedded Systems

1000–1030 Coffee Break

1030–1200 AUTONOMY IN AUTOMOTIVE

1030–1100 Fusion: A Safe and Secure Software Platform for Autonomous Driving
Authors: Philipp Mundhenk, Enrique Parodi, Roland Schabenberger
Autonomous Intelligent Driving GmbH, DE

1100–1130 Towards a Reliable and Context-Based System Architecture for Autonomous Vehicles
Authors: Tobias Kain¹, Julian-Steffen Müller¹, Philipp Mundhenk², Hans Tompits³, Maximilian Wesche¹, Hendrik Decke¹
¹Volkswagen AG, DE; ²Autonomous Intelligent Driving GmbH, DE; ³TU Wien, AT

1130–1200 Embedded Bayesian Perception and Decision-making system for Autonomous Vehicles
Speaker: Christian Laugier, INRIA Grenoble, FR

1200–1300 Lunch Break in Salon des Médailleurs

1300–1400 Keynote “VoloCity: Considerations for a Safe Transitions from Manned to Unmanned”
Speaker: Florian Michael Adolf, Volocopter, DE

1400–1430 Safety-Critical Heterogeneous Computing for Aerospace
Speaker: Juan Valverde, United Technologies Research Centre Ireland (UTRC), IE

1430–1500 Coffee Break

1500–1630 ENGINEERING OF AUTONOMOUS SYSTEMS

1500–1530 BreachFlows: Systematic Simulation-Based Testing with Formal Requirements For CPS
Speaker: Alexandre Donze, Decyphir, US

1530–1600 Agile Requirement Engineering for a Cloud System for Automated and Networked Vehicles
Authors: Armin Mokhtarian, Alexandru Kampmann, Bassam Alrifaee, Bastian Lampe, Lutz Eckstein, Stefan Kowalewski
RWTH Aachen University, DE

1600–1630 Systematic Physical-World Testing of Autonomous Driving Systems
Speaker: Cong Liu, University of Texas at Dallas, US

1630–1730 Open Floor Panel: Autonomy in Avionics and Automotive: Happy Marriage or Consensual Divorce?
Field-programmable gate array (FPGA) technology is becoming more and more relevant: recent examples include Intel’s acquisition of Altera in 2015, Amazon’s 2016 announcement of FPGAs within their AWS cloud infrastructure, and Microsoft’s statement in 2018 that more than 100K FPGAs were deployed in their Azure cloud for machine learning acceleration. With traditional cloud infrastructure -- which are mainly processor based -- software engineers have a choice of open-source (e.g. GNU GCC, Clang) and proprietary compilers (Microsoft, Intel) to use. However, the wide availability of FPGA technology contrasts with the narrow ways in which one can access them -- through proprietary tools.

There is no doubt that proprietary EDA tools are successful, mature, and are fundamental for hardware development. However, the “walled garden” approach created by closed-source toolflows can hamper novel FPGA-based applications and EDA innovation alike by requiring that researchers either operate within the limits of what has already been imagined, or require that they attempt to simulate their effects on incomplete models, potentially leading to incorrect conclusions. For such an off-the-shelf field-programmable technology, unlike fixed-function ASICs, this seems like a lost opportunity.

Another recent development has been growing activity in the open-source community to produce open equivalents of EDA tools, as well as efforts to document FPGA architectures. For instance, Yosys has been widely used for behavioral synthesis since 2012 and Project IceStorm, the first fully open-source FPGA design flow has been available since 2015; together they enabled Trenz Electronic’s icoBOARD, a Raspberry Pi accessory that could be programmed entirely using its ARM CPU, a platform not otherwise supported by the vendor. The availability of low-cost FPGA development boards such as the icoBOARD, TinyFPGA, IceZUM Alhambra, amongst others have also played a part in fostering this “Open FPGA” movement. The advantages of open design automation -- as Linux has provided for operating systems -- are many: unrestricted research and development, improved quality due to competition, teaching benefits, as well as lowering the barrier and risk to entry, and time to market, of start-ups for building novel FPGA applications, tools, and silicon. With such an open-source ecosystem in place, reprogrammable logic could achieve the same success and inspire the next generation of hardware engineers as the Raspberry Pi has done for software engineers.

This workshop intends to provide an avenue for industry, academics, and hobbyists to collaborate, network, and share their latest visions and open-source contributions, with a view to promoting reproducibility and reusability in the design automation space. DATE provides the ideal venue to reach this audience since it is the flagship European conference in this field -- particularly poignant due to the recent efforts across the European Union (and beyond) that mandate “open access” for publicly funded research to both published manuscripts as well as software code necessary for reproducing its conclusions. A secondary objective of this workshop is to provide a peer-reviewed forum for researchers to publish “enabling” technology such as infrastructure or tooling as open-source contributions -- standalone technology that would not normally be regarded as novel by traditional conferences -- such that others inside and outside of academia may build upon it.
The OSVVM Verification IP Library is a growing set of transaction based models. Currently Looking to improve your VHDL FPGA verification methodology? OSVVM provides a complete solution for VHDL ASIC or FPGA verification. There is no new language to learn. It is simple, powerful, and concise. Each piece can be used separately. Hence, you can learn and adopt pieces as you need them.

0945–1000 Pitch talks for the poster session

1000–1030 Coffee break (and poster session)

VERIFICATION BLOCK 2

1030–1115 GHDL recent developments and the future of EDA FOSS

Speaker: Tristan Gingold

GHDL is an open-source VHDL simulator that fully supports VHDL 93 and many features of VHDL 2008. Last year, I got many requests (including at least one at OSDA) to support synthesis. Although this is work in progress, it is now possible to use GHDL as a synthesis front-end for Yosys and to handle non-trivial designs like the microwatt Power cpu. On many fronts, the EDA FOSS is making progress but there are missing features like analog mixed simulation, vhdl/verilog mixed designs or constraints based simulation.

1115–1200 Verilator, Accelerated

Speaker: Wilson Snyder

In this talk Wilson Snyder will present a quick summary of Verilator, the big 4th simulator, and recent accelerations in feature development, followed by examples of accelerating the simulation runtime of a real RISC-V design.

1200–1300 Lunch break (and poster session)

ASIC BLOCK

1300–1345 Coriolis2

Speaker: Jean-Paul Chaput

Starting in 1990, Sorbonne Université-CNRS/LIP6 developed Alliance, a complete VLSI CAD toolchain released under GPL. In this spirit, we are assembling an upgraded design flow for ASICs based on FOSS tools like GHDL & Yosys for logical synthesis and Coriolis2 for physical design. We will present the flow with a focus on the Coriolis2 part. Its main features are mixed design (digital/analog), symbolic layout (for digital parts) and a comprehensive Python interface. The use of symbolic layout allows portability across a wide range of nodes and foundries, and most importantly, frees us up from NDA preventing the sharing/reuse of the design layout. This should be an important milestone toward the creation of an open hardware community.

1345–1430 Open All the Way

Speaker: Tim Edwards

“Open hardware” is traditionally thought of as pertaining to HDL source code for FPGAs. But open EDA tools exist for taking HDL all the way to the foundry to produce a working ASIC. I present several flows for this task, including qflow and OpenROAD; and Ravenna, efabless’ new 2nd-generation RISC-V processor built end-to-end with open EDA tools.

1430–1500 Coffee break (and poster session)

FPGA BLOCK

1500–1545 Adapting nextpnr to Xilinx FPGAs

Speaker: David Shah

nextpnr is an open source FPGA place and route framework which began development in mid 2018, initially containing support for two different Lattice FPGA families but aimed at supporting any real-world architecture. Recent work has focussed on supporting the popular Xilinx 7-series and UltraScale+ FPGAs using two other open source projects, RapidWright and Project X-ray. These larger and more advanced FPGAs have provided some interesting challenges in packing, placement, routing and even bitstream generation. Although support is still experimental, nextpnr is now capable at building complex real-world designs for these architectures such as 64-bit SoCs with DDR3 memory.

1545–1645 The Yosys ecosystem

Speaker: Claire Wolf

Yosys is an open source HDL synthesis tool and more, with applications in synthesis for FPGAs and ASICs, and formal verification. This presentation gives a broad overview over the Yosys ecosystem, with a closer look at FPGA synthesis for Lattice iCE40 (with Project Icestorm), Lattice ECP5 (with Project Trellis), and Xilinx devices (with Project X-Ray and Project Leuctra), as well as formal verification (SBY, MCY). The low cost of the open source formal verification tools, as well as the low cost of commercial tools based on that open source infrastructure, allows the use of formal verification techniques in new ways, beyond traditional use-cases for formal hardware verification tools.

1645–1700 Workshop closing

1700–1730 (Optional) Holistic plenary discussion on the workshop and future directions of OSDA
POSTER SESSION

Platform independent CPU-FPGA co-design framework: application to cascaded finite impulse response filter synthesis

SystemVerilog support in Open Source Tool
Zeller, H.

Skeleton: An Open Source EDA Tool Flow from Hierarchy Specification to HDL Development
Rodriguez-Ferrandez, I.; Cabo, G.; Barrera, J.; Giesen, J.; Jover-Alvarez, A. & Kosmidis, L.

Towards a Hardware DSL Ecosystem: RubyRTL and Friends
Le Lann, J.-C.; Badier, H. & Kermarrec, F.

ComBlock: a simple core for FPGA-processors communication

PyFPGA: a Python Package to abstract the use of FPGA development tools
Melo, R. A. & Valinoti, B.

W06 STOCHASTIC COMPUTING FOR NEUROMORPHIC ARCHITECTURES (SCONA)
AUTRANS 1 0900 – 1630

Organisers
Ilia Polian, University of Stuttgart, DE
John P. Hayes, University of Michigan, Ann Arbor, US
Weikang Qian, Shanghai Jiao Tong University, CN

Webpage: https://www.scona2020.uni-stuttgart.de

The workshop’s topics include, but not limited to, the following:
- Stochastic primitives for neural networks and other neuromorphic architectures
- Neuromorphic hardware architectures based on stochastic computing
- Methods for design, synthesis, analysis, and verification of stochastic circuits
- Stochastic circuits and architectures based on emerging technologies
- Applications of neuromorphic stochastic architectures and case studies

0900–1000 WORKSHOP INTRODUCTION
0900–0915 Workshop introduction
0915–1000 Keynote: Stochastic Computing for Machine Learning towards an Intelligent Edge
Speaker: Warren Gross, McGill University, CA

1000–1030 Coffee Break

1030–1200 STOCHASTIC APPROACHES FOR ARTIFICIAL INTELLIGENCE
1030–1100 PASCA: PArallel Stochastic Computing based Neural Network Accelerators
Speaker: Runsheng Wang, Peking University, CN

1100–1130 Tsetlin Machine: A New Paradigm for Pervasive AI
Authors: Adrian Wheeldon¹, Rishad Shafik¹, Alex Yakovlev¹, Jonathan Edwards¹, Ibrahim Haddadi¹, Ole-Christoffer Granmo²
¹Newcastle University, GB; ²University of Agder, NO

1130–1200 Stochastic Neural Networks: Approaches and New Challenges
Speaker: Florian Neugebauer, University of Stuttgart, DE

1200–1300 Lunch Break in Salon des Médaillés

1300–1430 EMERGING ARCHITECTURES FOR STOCHASTIC COMPUTING
1300–1430 Introduction to Dynamic Stochastic Computing
Speaker: Siting Liu, Jie Han, University of Alberta, CA

1330–1400 From Unary to Low-Discrepancy: Deterministic Bit-streams Revolutionize Stochastic Computing
Speaker: Hassan Najafi, University of Louisiana in Lafayette, US

1400–1430 On the Simulation of Software-Driven Stochastic Computing for Emerging Applications
Authors: Sercan Aygun¹,², Ece Olcay Gunes²
¹Yildiz Technical University, TR; ²Istanbul Technical University, TR

1430–1500 Coffee Break
1500–1630  NANOTECHNOLOGY FOR STOCHASTIC COMPUTING
1500–1530  Stochastic magnetic devices for cognitive computing
Speaker: Kaushik Roy, Purdue University, US
1530–1600  Stochastic learning in CMOS integrated HfO2 based memristive arrays
Authors: F. Zahari¹, M. K. Mahadevaiah², E. Perez², E. Perez-Bosch Quesada³, H. Kohlstedt¹, Ch. Wenger²³⁴, M. Ziegler⁴
¹Kiel University, DE; ²IHP, DE; ³Brandenburg Medical School Theodor Fontane, DE; ⁴TU Ilmenau, DE
1600–1630  Unary Computing Meets ReRAM Crossbar: A Novel Solution for Reliable ReRAM-based Neuromorphic Computing
Speaker: Weikang Qian, Shanghai Jiao Tong University, Shanghai, CN
1630  WORKSHOP WRAP-UP
The topics of the TRUDEVICE workshop include, but are not limited to:

- Manufacturing Test of Secure Devices
- Trustworthy Manufacturing of Secure Devices
- PUFs and TRNGs
- Hardware Trojans in IPs and ICs
- Reconfigurable Devices for Security
- Fault Attack Injection, Detection and Protection
- Validation and Evaluation Methodologies for Physical Security
- Side Channel Attacks and Countermeasures

0900–0910 OPENING SESSION: WELCOME AND GREETINGS
0910–1000 KEYNOTE SPEECH
  
  Security in the Quantum Era: Quantum-secure Solutions for Critical Infrastructures
  
  Speaker: Johanna Sepúlveda, Airbus Defence and Space, DE

  Abstract: The advent of quantum computers represents a threat for secure communications. In order to prepare for such an event, critical infrastructures must integrate quantum-secure capabilities. Quantum-Key-Distribution (QKD) and Post-Quantum Cryptography (PQC) promise to protect current and future systems against classical and quantum attacks. However, the efficient, safe and secure integration of such technologies is still a challenge. In this talk I discuss the requirements and constraints of the critical infrastructures, the opportunities and challenges of the adoption of such quantum-secure solution and the future of this area.

1000–1030 Coffee Break

1000–1030 POSTER SESSION
  
  Design time Assessment of Robustness against Physical Attacks
  
  Authors: Felipe Valencia, Ilia Polian and Francesco Regazzoni

  Creating Trusted Security Sensors for Anomaly Detection Systems using Hardware components
  
  Authors: Apostolos Fournaris and Charalambos Dimopoulos

1030–1100 SECURITY OF HARDWARE PLATFORMS
  
  1030–1045 Side-channel Leakage Assessment On RISC-V Architecture
  
  Authors: Ezinam Bertrand Talaki, Mathieu Bouvier Des Noes, Olivier Savry and David Hely

  1045–1100 Secure Update of FPGA-based Secure Elements using Partial Reconfiguration
  
  Authors: Florian Unterstein, Tolga Sel, Thomas Zeschg, Nisha Jacob, Michael Tempelmeier, Michael Pehl and Fabrizio De Santis

1100–1200 CYBERSECURITY @NANOEOLEC - AN INDUSTRIAL PERSPECTIVE TO CYBERSECURITY ISSUES FROM THE IRT NANOEOLEC
  
  Talk from IRT Nanoelec team on “Industry’s Perspective to Cybersecurity Issues”

1200–1300 Lunch Break in Salon des Médailles

1300–1350 KEYNOTE SPEECH: ON-CHIP POWER DISTRIBUTION NETWORK AS UNINTENTIONAL CHANNEL FOR PASSIVE AND ACTIVE ATTACKS
  
  Speaker: Falk Schellenberg, Ruhr University Bochum, DE

1350–1430 PHYSICAL ATTACKS AND COUNTERMEASURES
  
  1350–1410 A Systematic Approach for Hardware Security Assessment of Secured IoT Applications
  
  Authors: Zahra Kazemi, Cyril Bresch, Mahdi Fazeli, David Hely and Vincent Beroulle

  1410–1430 On Resilience of Security-oriented Error Detecting Architectures Against Power Analysis
  
  Authors: Osnat Keren and Ilia Polian

1430–1500 Coffee Break

1430–1500 POSTER SESSION
  
  Design time Assessment of Robustness against Physical Attacks
  
  Authors: Felipe Valencia, Ilia Polian and Francesco Regazzoni

  Creating Trusted Security Sensors for Anomaly Detection Systems using Hardware components
  
  Authors: Apostolos Fournaris and Charalambos Dimopoulos

1500–1600 PHYSICALLY UNCLONABLE FUNCTIONS (PUFS)
  
  1500–1520 Electromagnetic Enclosure PUF for Tamper Proofing Commodity Hardware and other Applications
  
  Authors: Johannes Tobisch, Christian Zenger and Christof Paar

  1520–1540 Power of Prediction: Advantages of Deep Learning Modeling as Replacement for Traditional PUF CRP Enrollment
  
  Authors: Amir Alipour, David Hely, Vincent Beroulle and Giorgio Di Natale

  1540–1600 An Efficient Implementation of A Delay-Based PUF Construction
  
  Authors: Nicolas Sklavos and Elif Bilge Kavun

1600–1620 HARDWARE TROJANS
  
  FlowGuard: Securing Design Flow to Prevent Hardware Trojan
  
  Authors: Junghee Lee and Wooil Kim

1620–1630 CLOSING SESSION: FAREWELL
Quantum computers promise substantial speedups over conventional computers for many practical relevant applications such as quantum chemistry, optimization, machine learning, cryptography, quantum simulation, systems of linear equations, and many more. While considered „dreams of the future“ for a long time, recent years have shown impressive accomplishments -- as witnessed by the recent discussions on whether quantum advantage compared to classical devices has been achieved. At the same time, research in this area requires to bring together experts from different fields such as physics, math, theory, computer science, and, of course, design automation.

This workshop aims to provide a forum for that. It features invited talks by leading experts covering the broad range of the area including the physical realization of quantum computers, the software needed to run quantum algorithms on it, applications showing the benefits of the technology, as well as further challenges such as noise and fault tolerance to deal with. Besides that, participants are encouraged to present own contributions in a dedicated poster session (see call for contributions below). By this, the workshop shall provide an informal venue for both, researchers already working in the area but also researchers interested in the topic.
W09  IRT NANOELEC WORKSHOP: BRIDGING THE GAP BETWEEN SEMICONDUCTOR TECHNOLOGIES AND ARCHITECTURE DESIGN

ALPE D’HUEZ 0830 – 1210

Organisers
Didier Louis, IRT Nanoelec, FR
François Legrand, IRT Nanoelec, FR

This workshop will introduce IRT Nanoelec as a key player in Grenoble ecosystem by sharing results and vision on imaging solutions, photonic components and cyber security innovations.

0830–0900  INTRODUCTION AND KEYNOTE
IRT Nanoelec at a glance
Speaker: Hugues Metras, IRT Nanoelec, FR
IRT Nanoelec: how to combine multi-partner technology and application research in innovative technical fields, while getting concrete results in the end
Speaker: Dominique Thomas, STMicroelectronics, FR

0900–0930  3D INTEGRATION
0900–0920  3D Technologies and Architectures for High Performance Computing
Speaker: Pascal Vivet, CEA-Leti, FR

0920–0940  Benefits of 3D stacking process for Event Based sensors
Speaker: Jean-Luc Jaffard, Prophesee, FR

0940–1000  CAD tool for Smart Imager
Speaker: Christophe Vinard, Mentor Graphics, FR

1000–1015  Coffee Break

1015–1030  PHOTONICS
1015–1030  Driving photonics implementation through automation
Speaker: Tom Daspit, Mentor Graphics, FR

1030–1045  CEA-Leti versatile silicon photonics platform
Speaker: Quentin Wilmart, CEA-Leti, FR

1045–1100  Enabling Technologies for Field Programmable Photonic Gated Arrays
Speaker: José Capmany Francoy, iTEAM Research Institute, Universitat Politècnica de València, ES

1110–1210  CYBERSECURITY
1110–1210  Why is the Industrial IoT such a complex playground for cybersecurity?
Speaker: Jacques Fournier, CEA-Leti, FR

1130–1150  Challenges of a PKI for industrial systems
Speaker: Jean-Michel Brun, Schneider Electric, FR

1150–1210  A scalable security offer for components of the Industrial IoT
Speaker: Nicolas Anquet, STMicroelectronics, FR

1210–1330  Lunch Break in Salon des Médaillés

FRINGE MEETINGS

A number of specialist interest groups will be holding their meetings at DATE 2020. The following meetings are scheduled at the moment. A complete list of fringe meetings can also be found on the DATE homepage www.date-conference.com

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<td>MON</td>
<td>1300 – 1800</td>
<td>FDSOI IP SoC Day</td>
<td>Saint-Nizier</td>
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<tr>
<td>MON</td>
<td>1400 – 1800</td>
<td>Half-day Forum on “Advancing Diversity in EDA”, supported by IEEE CEDA and ACM SIGDA</td>
<td>Alpe d’Huez</td>
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<td>MON</td>
<td>1800 – 2100</td>
<td>Welcome Reception &amp; PhD Forum, hosted by EDAA, ACM SIGDA and IEEE CEDA</td>
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<td>TUE</td>
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<td>TUE</td>
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<td>EDAA General Assembly</td>
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<td>TUE</td>
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<td>WED</td>
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<td>Meeting of the IFIP Working Group 10.5</td>
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<td>1230 – 1330</td>
<td>DATE Sister Events Meeting</td>
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MON  FDSOI IP SOC DAY
SAINT-NIZIER 1300 – 1800
Organiser: Gabrièle Saucier, Design And Reuse, FR
Fully Depleted Silicon On Insulator (FD-SOI) technology, an European invention, offers the industry the lowest power consuming blocks especially for aeronautics and automotive. To fully take advantage of this technology, Asic designers need a consistent choice of IP/SoC in a proven ecosystem.
FDSOI half-day session, March 9th will provide a short and dense presentation of proven IP and Soc from the worldwide community of IP providers as well as the most innovative features of associated design environment.

MON  HALF-DAY FORUM ON “ADVANCING DIVERSITY IN EDA”, SUPPORTED BY IEEE CEDA AND ACM SIGDA
ALPE D’HUEZ 1400 – 1800
Organisers:
Chengmo Yang, University of Delaware, US
Nele Mentens, KU Leuven, BE
Ayse Coskun, Boston University, US
This is the third edition of a half-day forum, including talks, panels, structured mentoring sessions, and more. The goal of this event is to help facilitate women and underrepresented minorities (URM) to advance their careers in academia and industry, and hence, to help increase diversity in the EDA community.
Fringe Meetings

Through an interactive medium, the forum will provide practical tips to women and URM on how to succeed and overcome possible hurdles in their career growth, while at the same time, connecting senior and junior researchers in networking and mentoring sessions.

The event is jointly sponsored by IEEE CEDA and ACM SIGDA. Previous editions of the forum were held at DATE 2018 and DAC 2019.

1400 Welcome and Introduction

Organisers:
Nele Mentens, KU Leuven, BE
Chengmo Yang, University of Delaware, US
Ayse Coskun, Boston University, US

Keynote: Title TBC
Keynote Speaker: Heike Riel, IBM Research, CH

1445 Panel 1: Negotiating: Practical Strategies for Women and URM in Tech
Moderator: Andrea Cathelin, STMicroelectronics, FR
Panellists:
David Atienza, EPFL, CH
Johanna Sepúlveda, Airbus Defence and Space, DE
Aida Todri-Sanial, French National Council of Scientific Research (CNRS), FR

This panel discusses negotiation in the EDA industry and academia at various job levels, including for addressing the gender and minority pay gap, when seeking promotions, or for increasing personal visibility at the workplace and in the community. The panellists will provide practical strategies as well as their broader insights and experiences.

1530 Coffee Break

1600 Panel 2: Career Paths After PhD
Moderator: Mike Hutter, Cryptography Research, US
Panellists:
Elif Bilge Kavun, The University of Sheffield, GB
Chenchen Liu, University of Maryland Baltimore County, US
Marie-Minerve Louerat, CNRS and Sorbonne Université, FR

This panel discusses different possible career paths after PhD. Each path has specific challenges, but also specific rewards. The panellists will give insights on how they experienced career choices in academia and industry right after their PhD and during career path changes later on.

1645 Panel 3: How to Juggle Different Tasks at Your (Academic) Job
Moderator: Ingrid Verbauwhede, KU Leuven, BE
Panellists:
Marina Zapater, EPFL, CH
Sharon Hu, University of Notre Dame, US
Gabriela Nicolescu, École Polytechnique de Montréal, CA
Valeria Bertacco, University of Michigan Ann Arbor, US

This panel discusses the challenges that arise in an academic job with respect to the balance between teaching, student advising, proposal writing, and professional service. The panellists will share their personal approach towards an efficient division of time among these different tasks. While most panellists are from academia, the strategies and challenges apply to many industry jobs as well.

1730 Speed Mentoring Session
This structured mentoring session will match each mentee with a few mentors throughout the session, with the goals of getting quick tips and feedback, as well as identifying good mentor-mentee matches for longer term mentorship

1800 Closing Remarks, followed by DATE Welcome Reception & PhD Forum

MON
WELCOME RECEPTION & PHD FORUM,
HOSTED BY EDAA, ACM SIGDA AND IEEE CEDA
LUNCH AREA 1800 – 2100
PhD Forum Chair:
Robert Wille, Johannes Kepler University Linz, AT

All registered conference delegates and exhibition visitors are kindly invited to join the DATE 2020 Welcome Reception and subsequent PhD Forum, which will take place on Monday, 9 March 2020, from 1800 to 2100 at the DATE venue in the Lunch Area. The PhD Forum of the DATE Conference is a poster session and a buffet style dinner hosted by the European Design Automation Association (EDAA), the ACM Special Interest Group on Design Automation (SIGDA), and the IEEE Council on Electronic Design Automation (CEDA). The purpose of the PhD Forum is to offer a forum for PhD students to discuss their thesis and research work with people of the design automation and system design community. It represents a good opportunity for students to get exposure on the job market and to receive valuable feedback on their work.

FM01.1 Networks-on-Chip for Heterogeneous 3D Systems-on-Chip
Author: Jan Moritz Joseph, Otto-von-Guericke Universität Magdeburg, DE

FM01.2 Intelligent Scheduling Algorithms for Energy Optimization in Smart Grid
Author: Nilotpal Chakraborty, IIT Patna, IN

FM01.3 Enhanced Detection and Prevention Techniques to Ensure a Secured Hardware with Improved Performance Metrics
Author: Sree Ranjani, IIT Madras, IN

FM01.4 QoS-aware Cross-layer Reliability-integrated Design of Heterogeneous Embedded Systems
Author: Siva Satyendra Sahoo, Technische Universität Dresden, DE

FM01.5 Design and implementation aspects of post-quantum cryptography
Author: Angshuman Karmakar, IMEC-COSIC, KU Leuven, BE

FM01.6 Security implications of power management systems in multicore devices
Author: Philipp Miedl, ETH Zurich, CH

FM01.7 Towards Sustainable Logic Encryption in an Age of Mistrust
Author: Amin Rezaei, Northwestern University, US

FM01.8 Architectures And Automation For Beyond-CMOS Technologies
Author: Debiyoti Bhattacharjee, Nanyang Technological University, SG

FM01.9 On-chip Thermal Monitoring and Optimization for New-generation Manycore Systems
Author: Mengquan Li, Nanyang Technological University, SG
FRINGE MEETINGS

FM01.1.10  Instruction-Level Abstraction (ILA): A Uniform Specification for System-on-Chip (SoC) Verification  
Author: Bo-Yuan Huang, Student, TW

FM01.1.11  A Formal Approach towards Pattern Guided Scheduling in Embedded Control Systems  
Author: Sumana Ghosh, TU Munich, DE

FM01.1.12  Design and Evaluation of Ethernet-based E/E-Architectures for Latency- and Safety-critical Applications  
Author: Fedor Smirnov, Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), DE

FM01.1.13  System-Level Mapping, Analysis, and Management of Real-Time Applications in Many-Core Systems  
Author: Behnaz Pourmohseni, Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), DE

FM01.1.14  Self Aware Nature Inspired Approaches Ensuring Embedded Security  
Author: Krishnendu Guha, University of Calcutta, IN

FM01.1.15  CAD Frameworks for Advancing Design IP Protection  
Author: Satwik Patnaik, New York University, US

FM01.1.16  Design Automation for Error-Tolerant Sample Preparation with Digital Microfluidic Biochips  
Author: Sudip Poddar, National Taiwan University of Science and Technology, TW

FM01.1.17  Automated Test Generation with SystemC Designs for Pre-Silicon Validation  
Author: Bin Lin, Portland State University, US

FM01.1.18  Dynamic Energy Management of Mixed-Criticality Real-Time Networks-on-Chip  
Author: Thawra Kadeed, TU Braunschweig, DE

FM01.1.19  Proving Correctness of Industrial Multipliers using Symbolic Computer Algebra  
Author: Alireza Mahzoon, University of Bremen, DE

FM01.1.20  A Holistic Approach to Functional Safety for Networked Cyber-Physical Systems  
Author: Enrico Fraccaroli, Università di Verona, IT

FM01.1.21  Automated Analysis of Virtual Prototypes at the Electronic System Level–Design Understanding and Applications–  
Author: Mehran Goli, University of Bremen, DE

FM01.1.22  A Novel Test Flow for Approximate Digital Circuits  
Author: Marcello Traiola, LIRMM, FR

FM01.1.23  Heterogeneous HW/SW Techniques for Reliable Systems  
Author: Florian Kriebel, TU Wien, AT

FM01.1.24  Efficient Scale-Up and Scale-Out of Beam Longitudinal Dynamics Simulations  
Author: Konstantinos Iliakis, National Technical University of Athens, GR

FM01.1.25  On Improving Statistical Model Checking by Qualitative Verification  
Author: Tim Gonschorek, Otto von Guericke University Magdeburg, DE

FM01.1.26  Verifying Multipliers using Computer Algebra  
Author: Daniela Kaufmann, Johannes Kepler University Linz, AT

FM01.1.27  Energy-efficient Photonic Architectures for Large-scale Computing  
Author: Dharanidhar Dang, University of California, San Diego, US

FM01.1.28  Energy Efficient and Reliable Deep Learning Accelerator Design  
Author: Jeff Zhang, New York University, US

FM01.1.29  Connecting the Dots: From Theory to Application of IP Protection  
Author: Abhrajit Sengupta, New York University, US

FM01.1.30  Realistic Scheduling Models and Analyses for Advanced Real-Time Embedded Systems  
Author: Georg von der Brüggen, TU Dortmund, DE

FM01.1.31  Energy-efficient and Performance-driven Implementation of Computational Pipelines of Whole Genome Sequencing on Embedded Platforms  
Author: Sidharth Maheshwari, Newcastle University, GB

FM01.1.32  Complexity Reduction for Embedded System-Level Design  
Author: Valentina Richthammer, Ulm University, DE

TUE  ETTTC MEETING  
VILLARD DE LANS 2  1330 – 1430  
Organiser: Alberto Bosio, Lyon Institute of Nanotechnology, FR

The European Test Technology Technical Council (eTTTC) is the European section of the TTTC. eTTTC is a volunteer professional organization sponsored by the IEEE Computer Society. TTTC’s goals are to contribute to our members’ professional development and advancement, to help them solve engineering problems in electronic test, and to help advance the state-of-the-art. This meeting provides all actors involved in test technology to share information on upcoming events and projects.

TUE  EDAA GENERAL ASSEMBLY  
VILLARD DE LANS 2  1600 – 1800  
Organiser: Norbert Wehn, University of Kaiserslautern, DE

General assembly meeting for the members of EDAA, open to everyone interested in Electronic Design Automation.

TUE  ETS STEERING COMMITTEE MEETING  
VILLARD DE LANS 2  1600 – 1800  
Organiser: Matteo Sonza Reorda, Politecnico di Torino, IT

Meeting of the Steering Committee of the IEEE European Test Symposium.

WED  MEETING OF THE IFIP WORKING GROUP 10.5  
VILLARD DE LANS 2  1230 – 1430  
Organiser: Masahiro Fujita, University of Tokyo, JP

International Federation for Information Processing (IFIP) is the leading multinational, non-political organization in Information & Communications Technologies and Sciences and is recognized by United Nations and other world bodies. It has over 100 Working Groups and 13 Technical Committees. This is a meeting organized by WG10.5 (VLSI related technologies).

THU  DATE SISTER EVENTS MEETING  
LUNCH AREA  1230 – 1330  
Organiser: Norbert Wehn, University of Kaiserslautern, DE

Meeting of the representatives from ASP-DAC, ICCAD, DAC and DATE
EXHIBITION GUIDE - LIST OF EXHIBITORS

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AID – AUTONOMOUS INTELLIGENT DRIVING GMBH
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AID-Autonomous Intelligent Driving is bringing together the world’s top software, robotics, AI and automotive talents to build a future where autonomous driving is embraced by humans. By understanding the human challenges as well as the engineering ones, the technology we are testing today on the streets of Munich will become the backbone of a universal self-driving system – capable of improving life in urban environments for millions of people. With the agility of a start-up and the support of Audi (VW Group), AID is free to craft an autonomous world that works for everyone – from manufacturers to passengers, from city planners to pedestrians. For us, the future isn’t about merely making vehicles more autonomous, it’s about making people more autonomous. To find out more, please visit aid-driving.eu

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Altair Innovation Solutions
Altair is a global technology company that provides software and cloud solutions in the areas of product development, high performance computing (HPC) and data analytics. Altair is dedicated to bring forward technologies, business models and products, delivering value to our clients by continually looking beyond the horizon to where new insights, ideas and possibilities are created.

Altair PBS Works speeds up semiconductor development processes with innovative solutions that maximize simulation throughput in HPC environments. These solutions enhance the business value of restricted availability, high cost semiconductor simulation software licences by managing license availability and scheduling workload for maximal utilisation of both HPC and software assets.

Altair HyperWorks is the most comprehensive, open-architecture engineering simulation platform on the market. Altair’s semiconductor simulation technologies solve problems related to design automation, circuit design and analysis, electromagnetic compatibility and structural integrity of end-user products. Product development is driven forward at system level specification and detailed subsystem engineering stages of the product life cycle.

ANDES TECHNOLOGY
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Andes Technology Corporation is a public listed company with well-established technology and teams to develop innovative high-performance/low-power 32/64-bit processor cores and associated development environment to serve worldwide rapidly growing embedded system applications.

The company delivers the best super low power CPU cores, including the new RISC-V series with integrated development environment and associated software and hardware solutions for efficient SoC design. Up to the end of 2018, the cumulative volume of Andes-Embedded™ SoCs has reached 3.5 billion with 2018 alone contributing over 1 billion.

To meet the demanding requirements of today’s electronic devices, Andes Technology delivers configurable software/hardware IP and scalable platforms to respond to customers’ needs for quality products and faster time-to-market. Andes Technology’s comprehensive CPU includes entry-level, mid-range, high-end, extensible and security families to address the full range of embedded electronics products, especially for connected, smart and green applications. From 2017, Andes expands its product line to RISC-V processors and provides a total solution in V5 family cores, including N22, N25F/NX25F, D25F, A25/AX25, A25MP/AX25MP, A27/AX27/NX27V, A45/D45/N45 and AX45/DX45/NX45.

For more information about Andes Technology, please visit www.andestech.com
COMPANY PROFILES

ASIC and SOC Design: Behavioural Modelling & Simulation | Design Entry | Power & Optimisation | Synthesis | Verification
System-Level Design: Behavioural Modelling & Analysis | Hardware/Software Co-Design
Test: Logic Analysis
Services: Design Consultancy | Prototyping | Training
Embedded Software Development: Compilers | Debuggers | Real Time Operating Systems | Software/Modelling
Hardware: Development Boards | FPGA & Reconfigurable Platforms

CADENCE ACADEMIC NETWORK
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The aim of Cadence Academic Network is to promote the proliferation of leading-edge technologies and methodologies at universities renowned for their engineering and design excellence. A knowledge network among selected universities, research institutes, industry advisors and Cadence established to facilitate the sharing of technology expertise in the areas of verification, design and implementation of microelectronic systems.

Cadence Academic Network is sponsoring the DATE Interactive Presentations (IPs) again.

CEA List
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List, a CEA Tech institute, carries out research on smart digital systems. Its R&D programs, all with potentially major economic and social implications, focus on advanced manufacturing, cyberphysical systems, artificial intelligence and technologies for digital patient. By developing cutting-edge technological research, the List helps its industrial partners to enhance their competitiveness through innovation and technology transfer.

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Leti, a technology research institute at CEA Tech, is a global leader in miniaturization technologies enabling smart, energy-efficient and secure solutions for industry. Founded in 1967, Leti pioneers micro- & nanotechnologies, tailoring differentiating applicative solutions for global companies, SMEs and startups. CEA-Leti tackles critical challenges in healthcare, energy and digital migration. From sensors to data processing and computing solutions, CEA-Leti’s multidisciplinary teams deliver solid expertise, leveraging world-class pre-industrialization facilities. With a staff of more than 1,900, a portfolio of 2,700 patents, 10,000 sq. m. of cleanroom space and a clear IP policy, the institute is based in Grenoble, France, and has offices in Silicon Valley and Tokyo.

CEA-Leti has launched 65 startups and is a member of the Carnot Institutes network.
Follow us on www.leti-cea.com and @CEA_Leti.

ASIC and SOC Design: Analogue and Mixed-Signal Design | Behavioural Modelling & Simulation | Design Entry | MEMS Design | Physical Analysis (Timing, Thermal, Signal) | RF Design | Verification
System-Level Design: Behavioural Modelling & Analysis | Physical Analysis | Acceleration & Emulation | Hardware/Software Co-Design | Package Design | PCB & MCM Design
Test: Design for Test | Logic Analysis | Mixed-Signal Test | System Test
Embedded Software Development: Software/Modelling
Hardware: Development Boards | Workstations & IT Infrastructure
Semiconductor IP: Configurable Logic IP | CPUs & Controllers | Embedded Software IP | Encryption IP | Memory IP | Physical Libraries | Test IP | Verification IO

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Circuits Multi-Projects (CMP) is a manufacturing broker for ICs and MEMS, for prototyping and low volume production. Since 1981, more than 640 Institutions from 71 countries have been served, more than 8300 projects have been prototyped through 1142 manufacturing runs, and 74 different technologies have been interfaced. Integrated Circuits are available on CMOS, SiGe BiCMOS, HV-CMOS, CMOS-Opto from STMicroelectronics and ams down to 28 nm FDSOI. Design kits for most IC CAD tools and Engineering kits for MEMS are available. Assembling is provided in a wide range of plastic and ceramic packages.

Services Foundry & Manufacturing | Training | Prototyping

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ClearSy was founded on January 1st, 2001 by a group of engineers that had industrialized the formal modeling tool referred to as Atelier B, used in the rail transport industry to create safety software.

Clearsy was created on the basis of two principal objectives:
- To develop formal type methods and tools
- To develop software and systems that justify the use of formal methods

System-Level Design: Behavioural Modelling & Analysis | Hardware/Software Co-Design
Test: Design for Test | System Test | Test Automation (ATPG, BIST)
Services: Design Consultancy
Embedded Software Development: Debuggers | Real Time Operating Systems | Software/Modelling
Hardware: FPGA & Reconfigurable Platforms
Application-Specific IP: Data Communication | Digital Signal Processing | Security | Wireless Communication

DEFACHTO TECHNOLOGIES
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Defacto Technologies is an innovative chip design software company providing breakthrough RTL platforms to enhance integration, verification and Signoff of IP cores and System on Chips.

New segment markets such as automotive, mobile, virtual reality and artificial intelligence require leading edge SoCs with greater functionality, higher performance and much lower consumption. Meeting time-to-market requirements and lowering the overall cost including design steps is becoming a critical factor of success.

By adopting Defacto’s STAR design platform, major semiconductor companies are continuously moving from traditional and painful SoC design tasks to the Defacto’s joint “Build & Signoff” design methodology. The related ROI has been proven for hundreds of projects.

ASIC and SOC Design: Design Entry
Test: Design for Test
DOLPHIN DESIGN
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Headquartered in France, Dolphin Design, previously known as Dolphin Integration, is a semiconductor company employing 160 people, including 140 highly qualified engineers.

Their IP clusters, available for various technological processes and optimized for the best Energy Efficiency, feed their tailored, scalable and modular Power Management and Processing platforms to deliver fast and securely ASICs, either designed by or for their clients.

By the side of their clients, now exceeding 500 companies, they focus on human, inventive and long-term collaboration to enable them to bring products and devices, powered by innovative and accessible integrated circuits that minimize environmental impact, to the hands of billions of people everyday. In consumer markets including IoT, AI and 5G, or in high reliability markets, they unleash SoC designer creativity to deliver differentiation.

Tell them your biggest dream. Dare the impossible. We tech it on.

Semiconductor IP: Configurable Logic IP | Memory IP | Physical Libraries | Processor Platforms | Analogue & Mixed Signal IP
Application-Specific IP: Analogue & Mixed Signal IP

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Eurolab4HPC is a 2-year Horizon 2020 funded project committed to make Europe excel in academic research and innovation in HPC technology.
To reach this goal it has defined 4 actions:
1. To structure the HPC community by adding members to develop a community of excellence that engages in focused high-quality cross-stack activity.
2. To promote entrepreneurship by building an innovation pipeline from general purpose entrepreneurial training, business prototyping, business plan development and helping with funding. Take a look at our events calendar.
3. To stimulate technology transfer by connecting with other technology transfer activities and providing competitive seed funding for HPC technology transfer. Find out more about at our funded HPC innovation projects or take a look at our latest video: www.eurolab4hpc.eu.
4. To disseminate community news by investing substantial resources in dissemination activities, creating a stronger Eurolab4HPC brand.

For further information visit: eurolab4hpc.eu and don’t forget to come by and say hello at the Eurolab4HPC stand here at DATE 2020!

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EUROPRACTICE was launched by the European Commission in 1989 to help companies improve their competitive position in world markets by adopting ASIC, Multi-Chip Module or Microsystems solutions in their products. The program helps to reduce the perceived risks and costs associated with these technologies by offering potential users a range of services, including initial advice and ongoing support, reduced entry costs and a clear route to chip manufacture and product supply.
Since its creation, EUROPRACTICE has bridged the gap between academia and industry in the high-tech world by offering more than 600 European universities and research institutes affordable access to the latest IC (Integrated Circuits) design tools and technologies. This is reflected in the training provided by universities from which the best IC design engineers emerge, essential for the SMEs innovation in new IC products.

The ultimate goal of EUROPRACTICE is to enhance European industrial competitiveness in the global marketplace. The EUROPRACTICE services are open to industrial companies (especially SMEs), research institutes and academic users.

SERVICES OFFERED TO EUROPEAN SMEs AND ACADEMIC INSTITUTIONS:
The mission statement of EUROPRACTICE is to provide the European industry and academia with a platform to develop smart integrated systems, from advanced prototype design to volume production. The latter is achieved by providing affordable and easier access to a wide range of state-of-the-art industry-grade fabrication technologies and design tools complemented with training and support to the customer in all critical steps which are needed.

- Affordable access to industry-standard and state-of-the-art design (CAD) tools
- Distribution and full support of high-quality cell libraries and design kits for the most popular CAD tools
- Low-cost prototyping in various technologies (both ASIC and More than Moore) via MPW runs
- Access to advanced packaging and smart system integration
- Training courses in advanced design flows and on various technologies

IC SERVICES OFFERED TO THE GLOBAL INDUSTRY:
EUROPRACTICE also offers industry worldwide access to microelectronic and microsystem design services, MPW prototyping, small volume production, packaging and test operations. Note, this does not include access to design tools.

Industry from all over the world have rapidly discovered the benefits of using the EUROPRACTICE IC service to help bring new product designs to market quickly and cost-effectively. The EUROPRACTICE ASIC route supports especially those companies who do not always need the full range of services or high production volumes. Those companies will gain from the flexible access to silicon prototype and production capacity at leading foundries, design services, high quality support and manufacturing expertise. This you can get all from EUROPRACTICE IC service, a service that is already established for 20 years in the market.

THE EUROPRACTICE SERVICES ARE OFFERED BY THE FOLLOWING CENTERS:
- imec (Belgium)
- Fraunhofer-Institut für Integrierte Schaltungen (Fraunhofer IIS) (Germany)
- STFC Rutherford Appleton Laboratory (United Kingdom)
- CMP (France)
- Tyndall National Institute (Ireland)

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The scope of Fractal Technologies products is to check consistency and validate all different data formats used in designs and subsequently improve the Quality of Standard Cell Libraries, IO libraries and general purpose IP blocks (Digital, Mixed Signal, Analog and Memories). Fractal Technologies offers Crossfire software and IPdelta software. Our mission is simple: make the Quality of your Design Formats an asset for your business.

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The rise of cyberattacks constitutes a major challenge for our societies, with an estimated cost of $6 trillion per year by 2021 (Forbes). In addition to their disastrous economic and social impact, these attacks weaken the confidence of citizens in the digital transition of activities and cause serious international tensions. As a consequence, the development of new sustainable solutions that enable end-to-end security, privacy and infrastructure resilience is now a multi-dimension challenge: technical, business, scientific and social.

The Grenoble Alpes Cybersecurity Institute – in short, Cyber@Alps – aims at undertaking ground-breaking interdisciplinary research in order to address these cybersecurity and privacy protection challenges. Our main technical focus are on cost effective secure elements, security of critical infrastructures all along their life cycle, vulnerability analysis and global challenges in terms of risk analysis and validation of large systems, including practical resilience across the industry and the society. Our approach to cybersecurity is holistic, encompassing technical, legal, law-enforcement, economic, social, diplomatic, military and intelligence-related aspects with strong partnerships with the private sector and robust national and international cooperation with leading institutions in France and abroad.
HIPEAC - EUROPEAN NETWORK ON HIGH PERFORMANCE AND EMBEDDED ARCHITECTURE AND COMPILATION

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HiPEAC (High Performance and Embedded Architecture and Compilation) is the premier focal point for networking, dissemination, training, and collaboration activities in Europe for researchers, industry, and policy related to computing systems. Today, its network, the biggest of its kind in Europe, numbers over 2,000 specialists.

HiPEAC’s mission is to advance computer architecture and computing systems research and development as a discipline in Europe. Its objectives are to:

- Secure and strengthen a leading position for Europe in computing systems that support all aspects of modern society by advancing computing systems as a discipline.
- Prepare the next generation of world-class computing systems scientists and engineers in Europe by supporting their academic and professional development.
- Build a dynamic ecosystem for the design and implementation of computing systems in Europe by bringing together European research, industry, small/medium enterprises (SMEs), and policy.
- Align research efforts in computing systems and strengthen research impact in Europe by identifying long-term challenges in computing systems and articulating their impact on modern society.

To join for free email membership@hipeac.net.

For further information visit www.hipeac.net/network/#/ and don’t forget to visit our stand here at DATE 2020!

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HiSilicon is a global leading fabless semiconductor and IC design company that is dedicated to providing comprehensive connectivity and multimedia chipset solutions. As a prominent industry leader, HiSilicon paves the way for innovations in global connectivity and end-to-end ultra-HD video technologies.

From high-speed communications, smart devices, and IoT to video applications, HiSilicon chipsets and solutions have been proven and certified in more than 100 countries and regions in the world.

Headquartered in Shenzhen, China, HiSilicon has over 7,000 employees in offices and research centers in Beijing, Shanghai, Chengdu, Wuhan, Singapore, South Korea, Japan, Europe and other regions across the world. After 20 years of research and development, HiSilicon has built up a strong portfolio of IC design and verification technologies, developed an advanced EDA design platform, and is responsible for the setup of several development processes and regulations. Over the years, HiSilicon has successfully developed more than 200 models with proprietary IPR and filed over 8,000 patents. HiSilicon has also established strategic partnerships with global leaders in the ecosystem, specifically for engineering (wafer manufacturing), packaging, and testing within a reliable supply chain.

The mission of HiSilicon is to provide the best-quality solutions and services with a prompt response to our customers – HiSilicon is customer-centric and is always committed to creating values for our customers.
IEEE COUNCIL ON ELECTRONIC DESIGN AUTOMATION
(IEEE CEDA)
Sponsor

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The Council on Electronic Design Automation (CEDA) was established to foster design automation of electronic circuits and systems at all levels. The Council’s field of interest spans the theory, implementation, and use of EDA/CAD tools to design integrated electronic circuits and systems. This includes tools that automate all levels of the design, analysis, and verification of hardware and embedded software up to and including complete working systems. CEDA enables the exchange of technical information by sponsoring publications, conferences and workshops and through local chapters for volunteers activities.

If you are interested please contact admin@ieee-ceda.com or check our website for more information about our activities and how to become a member for free.

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Intel is the largest semiconductor chip maker with platforms designed to work together - seamless, connected and puts the user at the center. The range of computing products based on Intel® architecture goes beyond PCs and servers and extends to tablets, consumer electronics devices, and more. Over the last decade, Intel has evolved from a company that largely serves the PC industry, to a company that increasingly provides the vital intelligence inside all things computing. Hardware and software products by Intel power most of the world’s data centers, connect hundreds of millions of cellular handsets and help secure and protect computers, mobile devices and corporate and government IT systems. Intel Labs Europe (ILE) is a central division within Intel that deals with research-oriented topics, which are supposed to be brought into future Intel products in a three to ten years timeframe. ILE has a worldwide presence and has some important Labs in Europe, among which the ones in Germany (Munich, Karlsruhe and Darmstadt). ILE deals with medium and long-term research related topics like quantum computing, Artificial Intelligence (AI), dependable systems, autonomous driving, and security and safety, among others.

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Nanoelec Research Technological Institute (IRT), headed by CEA-Leti, conducts research and development in the field of information and communication technologies (ICT) and, specifically, micro- and nanoelectronics. Based in Grenoble, France, IRT Nanoelec leverages the area’s proven innovation ecosystem to create the technologies that will power the nanoelectronics of tomorrow, drive new product development and inspire new applications. The R&D conducted at IRT Nanoelec provides early insight into how emerging technologies will affect integrated circuits.

IRT Nanoelec pursues three objectives: The first is technology development for future generations of integrated circuits. Our researches are main focused on 3D integrated circuits, silicon photonics, power devices and characterization, currently IRT Nanoelec’s four silicon-based technology research programs.

Our second objective is to transfer new technologies to businesses through the 2 IRT Nanoelec diffusion programs. The capacity to translate research into marketable products is a much more relevant way to assess our capacity for innovation.

Finally, our third objective is to create new educational and training programs and content that meet the future human resources needs expressed by IRT Nanoelec’s industrial partners. We also strive to ensure that learners who complete IRT Nanoelec courses have acquired the skills necessary for successful career placement. Visit www.irtnanoelec.fr

ASIC and SOC Design: Physical Analysis (Timing, Thermal, Signal) | Power & Optimisation | Verification
Test: Design for Manufacture and Yield | Design for Test | Logic Analysis | System Test
Semiconductor IP: Analogue & Mixed Signal IP | Memory IP | Test IP | Verification IO
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MNEMOSENE is an ambitious Research and Innovation Action addressing the theme „Development of new approaches to scale functional performance of information processing and storage substantially beyond the state-of-the-art technologies with a focus on ultra-low power and high performance“ of the European Union’s Horizon 2020 ICT research and innovation programme.
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Coordinated by Delft Technical University (NL), the project consortium includes eight other partners from six different countries: Eindhoven University of Technology and IMEC (NL), ETH Zurich and IBM Research – Zurich (CH), Arm (GB), RWTH Aachen University (DE), INRIA (FR) and Intelligentsia Consultants (LU).

The MNEMOSENE Project has received funding from the European Union’s Horizon 2020 research and innovation programme under grant agreement number 780215.

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**ASIC and SOC Design:** Design Entry
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DATE 2021 – CALL FOR PAPERS

CONFERENCE AND EXHIBITION
22 – 26 MARCH 2021
MADRID EXPOSICIONES Y EVENTOS URBANOS (MEEU), MADRID, SPAIN

SCOPE OF THE EVENT
The 24th DATE conference and exhibition is the main European event bringing together designers and design automation users, researchers and vendors as well as specialists in hardware and software design, test and manufacturing of electronic circuits and systems. DATE puts strong emphasis on both technology and systems, covering ICs/SoCs, emerging technologies, embedded systems and embedded software.

STRUCTURE OF THE EVENT
The five-day event consists of a conference with plenary invited papers, regular papers, panels, hot-topic sessions, tutorials, workshops, special focus days and a track for executives. The scientific conference is complemented by a commercial exhibition showing the state-of-the-art in design and test tools, methodologies, IP and design services, reconfigurable and other hardware platforms, embedded software and (industrial) design experiences from different application domains, such as automotive, wireless, telecom and multimedia applications. The organisation of user group meetings, fringe meetings, a university booth, a PhD forum, vendor presentations and social events offers a wide variety of extra opportunities to meet and exchange information on relevant issues for the design automation, design test and communities. Special space will also be allocated for EU-funded projects to show their results.


AREAS OF INTEREST
Within the scope of the conference, the main areas of interest are: design automation, design tools and hardware architectures for electronic and embedded systems; test and dependability at system, chip, circuit and device level for analogue and digital electronics; modelling, analysis, design and deployment of embedded software and cyber-physical systems; application design and industrial design experiences.

Topics of interest include, but are not restricted to:
- System Specification and Modelling
- System-level Design Methodologies and High-Level Synthesis
- System Simulation and Validation
- Formal Methods and Verification
- Design and Test for Analogue and Mixed-Signal Circuits and Systems, and MEMS
- Design and Test of Secure Systems
- Network on Chip and Communication-Centric Design
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All papers have to be submitted electronically by Monday, 14 September 2020, as abstracts and by Monday, 21 September 2020 as full papers via: https://www.date-conference.com/
Papers can be submitted either for standard oral presentation or for interactive presentation. The Program Committee also encourages proposals for Special Sessions, Tutorials, Friday Workshops, University Booth Demonstrations, PhD Forum and Exhibition Theatre.

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