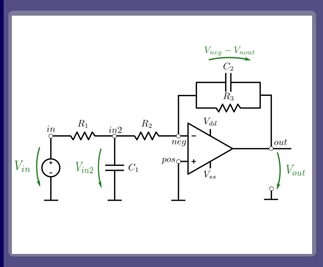
Ahmad Tarraf
Institute for Computer Science,
tarraf@em.cs.uni-frankfurt.de

Electronic Design Methodology

Formal Abstraction and Verification of Analog Circuits

Netlist



Spice netlist with full BSIM transistor accuracy. Verilog-A netlist descriptions are also supported

Model Abstraction

VERA → ELSA

State space sampler

Abstraction core

Abstracted Model

Hybrid automaton generated in Verilog-A, Matlab or SystemC-AMS syntax. The model is simulated or a reachability analysis is performed in the reduced state space ($\mathcal{S}_\lambda$). Via a back transformation, all nodal voltages and currents can be obtained in the original state space ($\mathcal{S}_o$)

VERA

- Samples the state space at full BSIM accuracy for a predefined input range
- Set up the nonlinear differential algebraic system
- Linearizes the system and computes the Kronecker from
- Performs a dominant Pole order reduction according to a specified frequency range of interest

state space vector in the reduced state space $\mathcal{S}_\lambda$ ← → Eigenvalue matrix

$$s\begin{bmatrix}\mathbf{I} & \mathbf{0}\\ \mathbf{0} & \mathbf{0}\end{bmatrix}\begin{bmatrix}\mathbf{x}_\lambda\\ \mathbf{x}_\infty\end{bmatrix}+\begin{bmatrix}\mathbf{\Lambda} & \mathbf{0}\\ \mathbf{0} & \mathbf{I}\end{bmatrix}\begin{bmatrix}\mathbf{x}_\lambda\\ \mathbf{x}_\infty\end{bmatrix}=\begin{bmatrix}\tilde{\mathbf{b}}_\lambda\\ \tilde{\mathbf{b}}_\infty\end{bmatrix}\cdot u$$

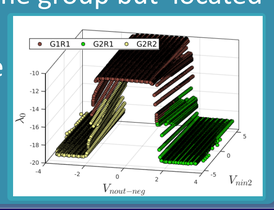
ELSA: Eigenvalue-based hybrid linear system abstraction

Task: find a HA that describes the system in the reduced state space

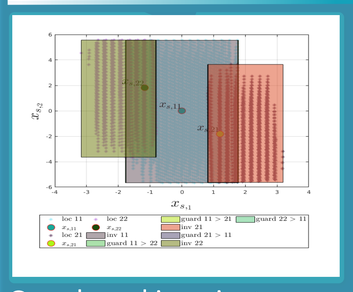
Location Identification

A location is uniquely identified by a group and a region: $loc = g(j)r(k)$

Eigenvalues are clustered into groups. Points in the same group but located in different partitions of the state space are separated into regions



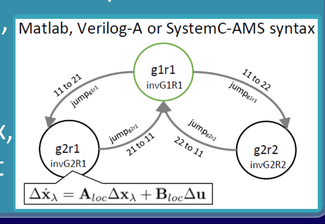
Guards and Invariants



Guards and invariants are determined in the $\mathcal{S}_\lambda$ space

System Description

In each location, the system behavior is described linearly. Δ-values are used in each location as the system is linearized around an operating point. Once the system leaves a location via a guard, a reset is applied, and a new system matrix, input matrix, and operating point are used

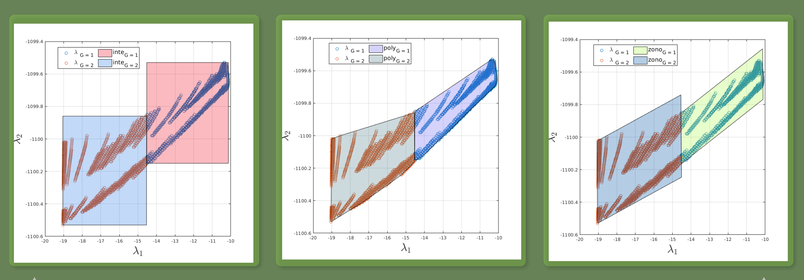


Extensions

Model With Parameter Variations

Model With Abstraction Variations

Instead of describing the system behavior via a matrix $\mathbf{A}_{loc}$ formed by taking the mean of the eigenvalues, a matrix zonotope or interval matrix is used to hull all the eigenvalues of a location for the Matlab (*Cora* [2]) models

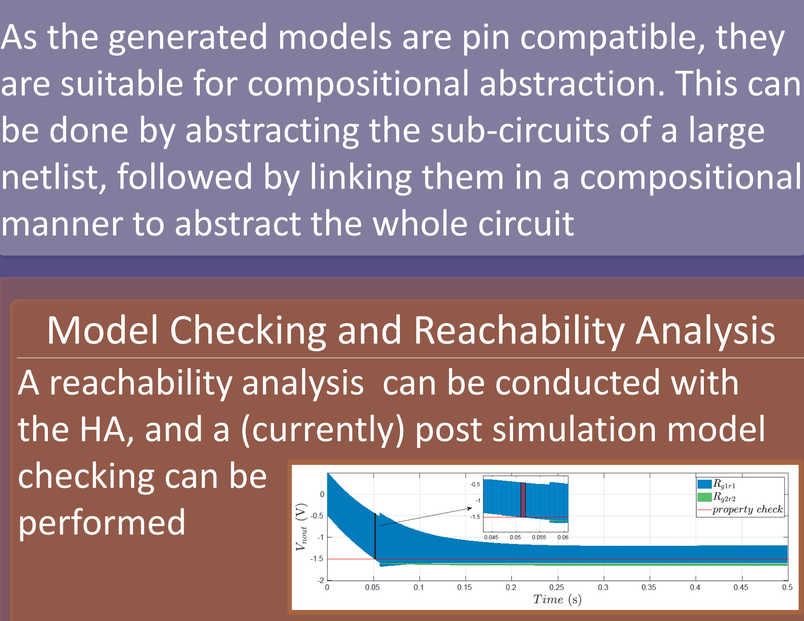


$$\Delta\dot{\mathbf{x}}_\lambda = \mathbf{\Lambda}_{[z/i],loc}\Delta\mathbf{x}_\lambda + \mathbf{B}_{loc}\Delta\mathbf{u}$$

$$\mathbf{\Lambda}_{[z]} = \{\mathbf{\Lambda}^{(0)} + \sum_{i=1}^{k} p_i \cdot \mathbf{\Lambda}^{(i)}\} \quad | p_i \in [-1,1]$$

$$\mathbf{\Lambda}_{[i]} = [\mathbf{\Lambda}, \overline{\Lambda}]$$

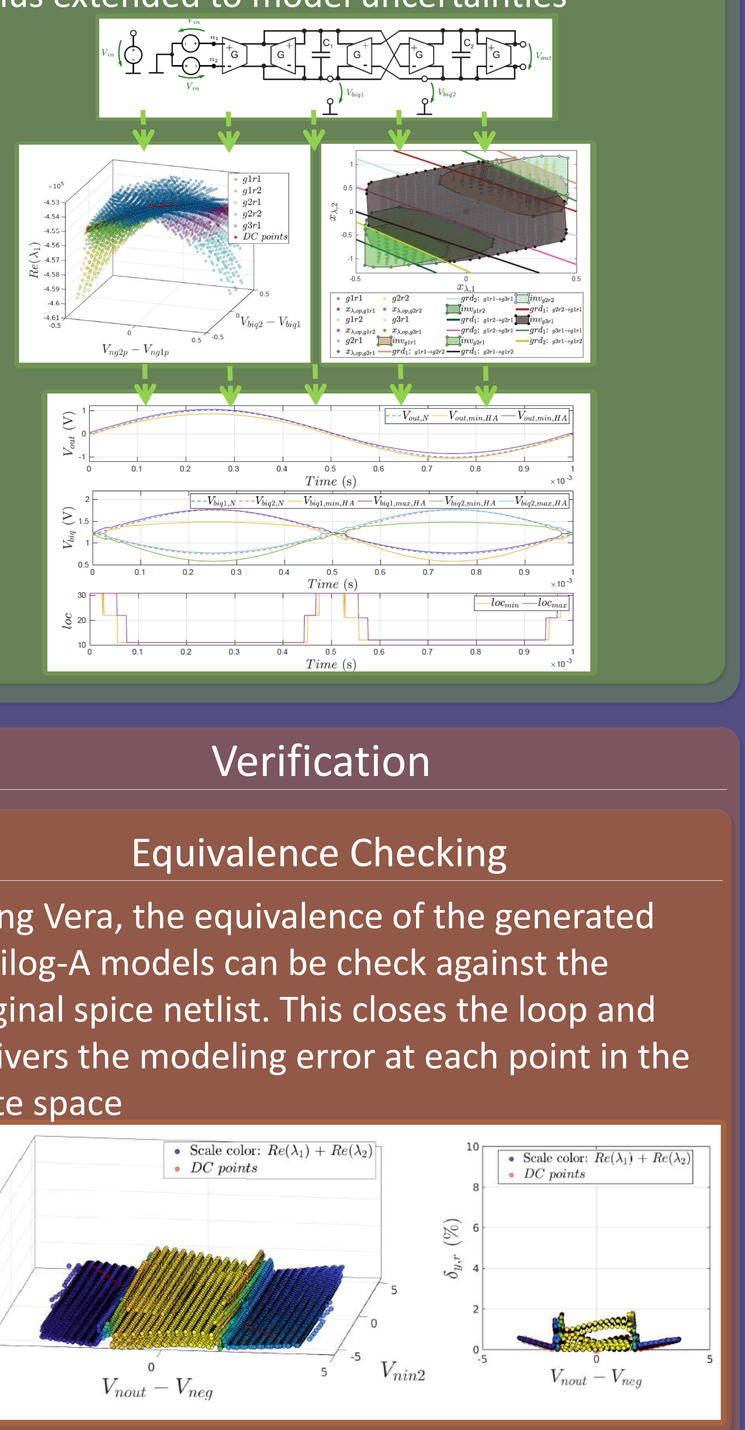
Model With Process Parameter Variations



Vera generates randomly, in a Monte-Carlo fashion, various versions of the netlist with different parameters according to the specified process parameters. The netlists are afterwards sampled in parallel and passed to Elsa, which in turn generates a HA from every netlist. This process is executed in parallel in Matlab. Finally, the generated HAs are merged into a unified model

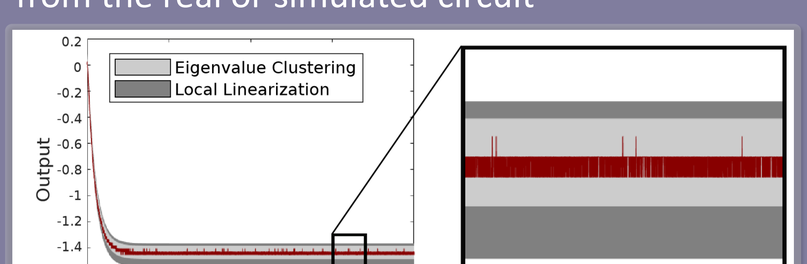
Extended SystemC-AMS Models

For the SystemC-AMS models a similar approach is possible using the AADD library [1]. The models are thus extended to model uncertainties



Conformance Model

Applies reachset conformant synthesis to add nondeterminism to piecewise-linear circuit models so that they enclose all recorded behaviors of the real system. By that, the model is extended to capture the recorded measurements from the real or simulated circuit



Compositional Automaton

As the generated models are pin compatible, they are suitable for compositional abstraction. This can be done by abstracting the sub-circuits of a large netlist, followed by linking them in a compositional manner to abstract the whole circuit

Model Checking and Reachability Analysis

A reachability analysis can be conducted with the HA, and a (currently) post simulation model checking can be performed

Verification

Equivalence Checking

Using Vera, the equivalence of the generated Verilog-A models can be check against the original spice netlist. This closes the loop and delivers the modeling error at each point in the state space

Publications

Ahmad Tarraf and Lars Hedrich, "From transistor level to cyber physical/hybrid systems: Formal verification using automatic compositional abstraction", it - Information Technology
Ahmad Tarraf and Lars. Hedrich, "Modeling Circuits with Parameter Variation by ELSA: Eigenvalue Based Linear Hybrid System Abstraction", 17. GMM/ITG-Fachtagung ANALOG, 2020
A. Tarraf, N. Kochdumper, M. Rechmal, L. Hedrich, and M. Olbrich, "Equivalence Checking Methods for Analog Circuits Using Continuous Reachable Sets", In IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Limassol, Cyprus, 2020
Ahmad Tarraf and Lars Hedrich, "Verification of modeling: metrics and methodologies", Modelling methodologies in analogue integrated circuit design,G. Dündar and M. B. Yelten, Eds., Institution of Engineering & Technology, 2020, pp. 95-116
N. Kochdumper, A. Tarraf, M. Rechmal, M. Olbrich, L. Hedrich, and M. Althoff, "Establishing Reachset Conformance for the Formal Analysis of Analog Circuits," ASP-DAC, 2020
Ahmad Tarraf and Lars Hedrich :"Automatic Modeling of Transistor Level Circuits by Hybrid Systems with Parameter Variable Matrices", SMACD, Lausanne, Switzerland, July 2019
Ahmad Tarraf and Lars Hedrich :"Behavioral Modeling of Transistor-Level Circuits using Automatic Abstraction to Hybrid Automata, DATE,Florence,2019
Ahmad Tarraf and Lars Hedrich :"Automatic Abstraction of Analog Circuits to Hybrid Automata", 16. GMM/ITG-Fachtagung ANALOG, 2018
Ahmad Tarraf and Lars Hedrich: "Automatic Abstraction of Transistor Level Circuits to Hybrid Automata", Frontiers in Analog Circuit Design (FAC), Wien, 2018

[1] C. Radojicic, C. Grimm, A. Jantsch, and M. Rathmair, "Towards verification of uncertain cyber-physical systems," in SNR@ETAPS, 2017
[2] M. Althoff, "An Introduction to CORA 2015," Proc. of the Workshop on Applied Verification for Continuous and Hybrid Systems, 2015

This poster presents result of the project faveAC funded by the DFG under the project number 286525601