Design Automation for Field-coupled Nanotechnologies

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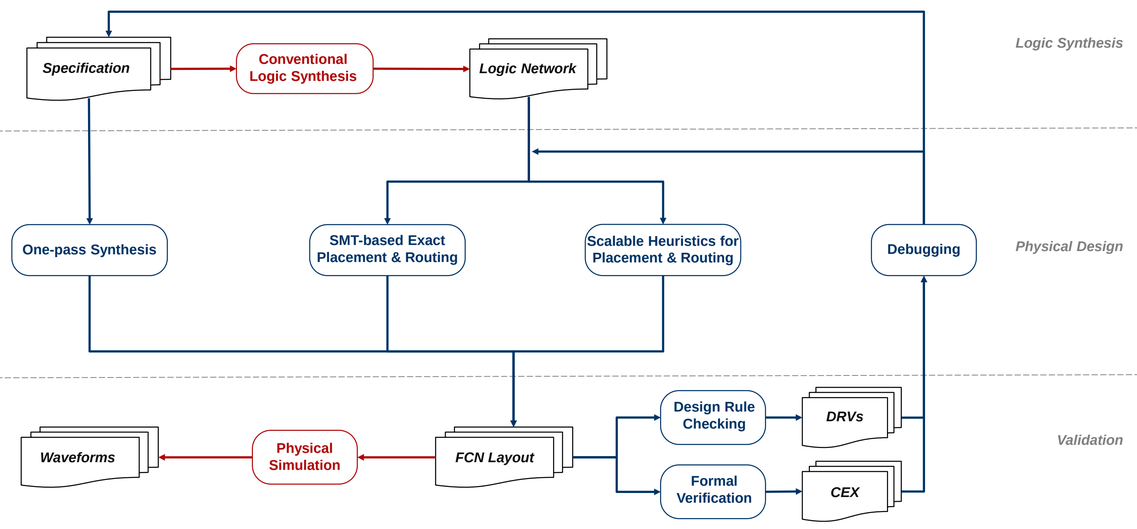
Abstract

As a class of emerging post-CMOS technologies, **Field-coupled Nanocomputing (FCN)** [1] promises computation with tremendously low energy dissipation. Even though ground breaking advances in several physical implementations like **Quantum-dot Cellular Automata (QCA)** or **Nanomagnet Logic (NML)** have been made in the last couple of years, design automation for FCN is still in its infancy and often still relies on manual labor. This thesis presents the first comprehensive flow for design automation in the FCN domain covering aspects of and providing **algorithms** for Synthesis, Physical Design, Validation, and Formal Verification. All approaches have been made publicly available as an open-source framework called ***fiction***, which provides a basis for future research in the field.

Proposed Design Automation Flow

For almost two decades, FCN design employed **mostly manual labor** for obtaining circuit layouts. Some greedy heuristics existed as well, which generated mediocre results in terms of quality and poor results in terms of scalability.

The following chart depicts the proposed design automation flow for automatic physical design of FCN circuit layouts. Conventional methods are shown in **red** and novel proposed methods in **blue**.



Even though scalability of existing solutions for FCN physical design was rather limited already, no optimality with respect to some cost metric could be guaranteed. Consequently, the absolute quality of these solutions remained unclear.

The proposed **SMT-based Exact Placement & Routing** [2] is highly parameterizable and is guaranteed to find the optimum FCN layout in terms of area under a given set of parameters and optimization criteria. Those can for instance be the clocking scheme and gate library to use and whether or not to utilize wire crossings.

Also, scalability was a huge issue with existing methods. This drawback is tackled by **Scalable Heuristics for Placement & Routing** [3], which provide a 2000+ times improvement in processable gate count at a runtime that is magnitudes faster compared to the greedy heuristics that have been state-of-the-art just a few years ago.

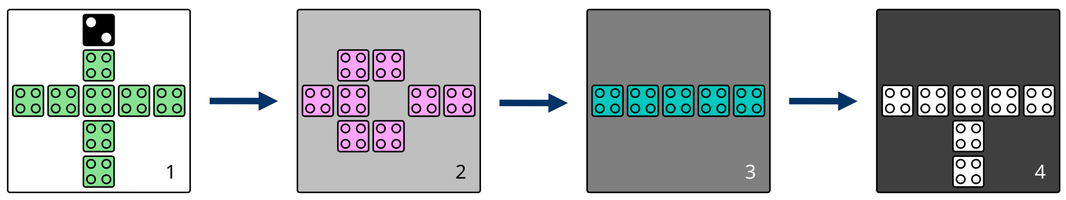
While these approaches yield layouts for given networks, specialized **One-pass Synthesis** [4] combines logic synthesis with placement & routing into a single step, fine-tuned to the distinct FCN design constraints. This yields optimum layouts for given logical specifications.

Since cells interact with each other on a quantum level, logical simulation is no trivial task. Furthermore, clocking affects timing directly leading to possible desynchronized signals throughout the layout. The usage of well-established, carefully simulated gate libraries allows to abstract from quantum effects, which can be determined via **Design Rule Checking** [5].

DRV-free circuits are the basis for proposed **Formal Verification** [5] that integrates both logical and timing aspects via a combination of SAT solvers and Integer Linear Programming to check against specifications.

Preliminaries on FCN Design

- Computations and data transfer is realized via repelling forces on a quantum level between nanoscale **cells arranged in patterned arrays**.
- Data flow is only possible due to shifted and **consecutively numbered external clocks**.
- FCN cells can be grouped in **tiles** controlled by the same external clock and thereby **forming logic elements**.

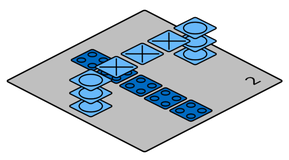


AND INV Wire Fan-out

Challenges

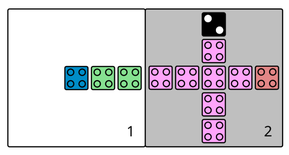
- Wires and gates are **equally expensive**.
- Data flow must be **synchronized** locally and globally.
- Area, delay, and the use of crossings is to be **minimized**.
- Placement, routing, and timing are strongly **interdependent**.
- Conventional methods from CMOS are **not applicable**.
- Specialized **logic synthesis** is still missing.

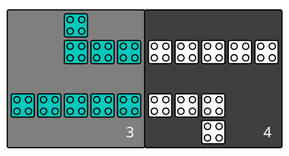
Holistic Open-Source Framework *fiction*



FCN technologies are often considered to be planar with limited crossing capabilities. Since non-planar logic networks cannot be realized crossing-free, ***fiction*** offers support for **multi-layer crossings**.

In the literature, both can be found: pin cells as part of gate structures and **designated I/O elements** located outside of gates. Both approaches are fully supported and available in all algorithms.

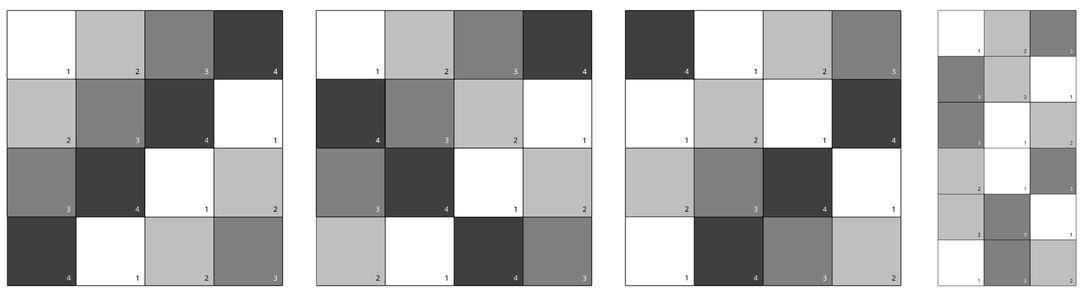




Gate-level abstraction has its limits. Often, chip area is wasted when only using a single wire per tile. In ***fiction***, **multi-wires** are supported allowing for more flexible physical design approaches.

Clocking Schemes

Clocking schemes (floor plans) can help pruning the search space during physical design. Several ones are predefined in ***fiction***, irregular clockings are supported, and custom ones can easily be implemented.



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Selected Publications

[1] N. G. Anderson and S. Bhanja. Field-coupled Nanocomputing: Paradigms, Progress, and Perspectives. *Springer*, New York (2014).

[2] M. Walter, R. Wille, D. Große, F. Sill Torres, and R. Drechsler. An Exact Method for Design Exploration of Quantum-dot Cellular Automata. *DATE* (2018).

[3] M. Walter, R. Wille, F. Sill Torres, D. Große, and R. Drechsler. Scalable Design for Field-coupled Nanocomputing Circuits. *ASP-DAC* (2019).

[4] M. Walter, W. Haaswijk, R. Wille, F. Sill Torres, and R. Drechsler. One-pass Synthesis for Field-coupled Nanotechnologies. *ASP-DAC* (2021).

[5] M. Walter, R. Wille, F. Sill Torres, D. Große, and R. Drechsler. Verification for Field-coupled Nanocomputing Circuits. *DAC* (2020).

Scan me!

https://github.com/marcelwa/fiction