Universität Bremen - Computer Architecture

Next Generation Design For Testability, Debug and Reliability Using Formal Techniques

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Motivation and Contributions

New measures are strictly required to pave the way for the next generation of integrated circuit designs to integrate them successfully and reliably in even safety-critical applications.

This thesis proses several novel approaches that combine formal techniques – like *Boolean Satisfiability* (SAT) problem, *Pseudo-Boolean Optimization* (PBO) techniques with *Bounded Model Checking* (BMC) - to address the arising challenges concerning the increase in test data volume, test application time, and the required reliability.
The main **contributions** are summarized as follows:

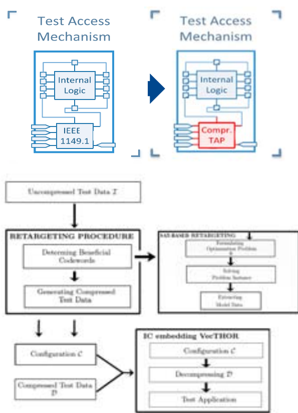
I. A lightweight embedded compression architecture (VecTHOR) for IEEE 1149.1 test access ports that combines a codeword-based compression approach with a dynamically configurable dictionary. VecTHOR provides a SAT-based retargeting framework orchestrating PBO techniques.

II. A novel hybrid compression architecture substituting the costly *bypass structure* of state-of-the-art circuit test as required, for instance, for low-pin count test applications enforcing a zero defect policy.

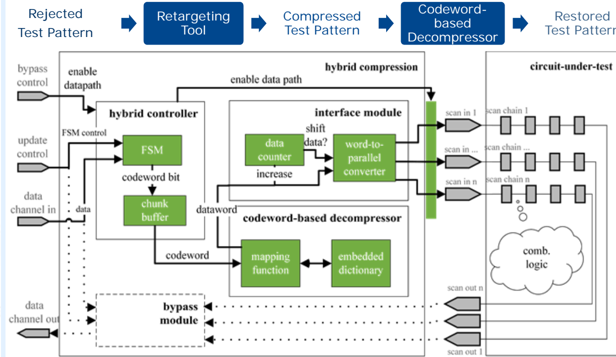
III. A new methodology that allows to significantly enhance the robustness of sequential circuits against (single) transient fault while neither introducing a large hardware overhead nor measurably impacting the circuit's latency. In particular, application-specific knowledge of the circuit is derived by applying SAT-based techniques and BMC, yielding the synthesis of a highly effective fault detection mechanism.

New Techniques for Test, Debug and Reliability

VecTHOR's Framework

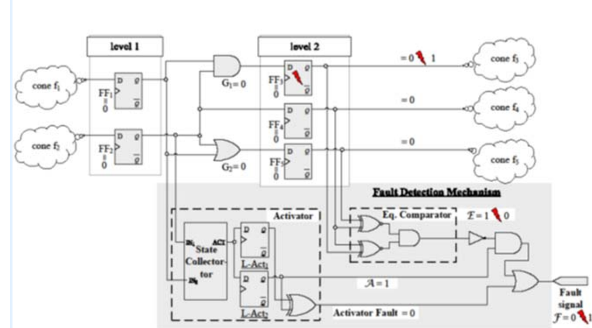


Hybrid Compression



Hybrid Compression Architecture replacing the regular *bypass module* (state-of-the-art embedded test compression) to take advantage of the codeword-based compression during the transfer of rejected test patterns. Consists of (a) *hybrid controller*, (b) *interface module*, and (c) *codeword-based decompressor*.

Reliability Enhancement

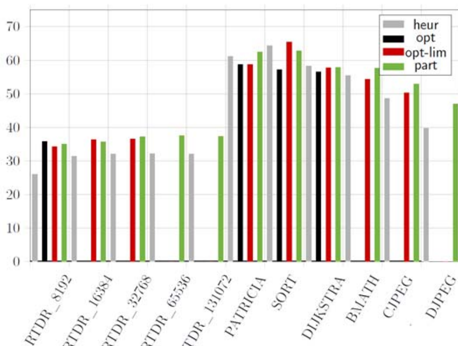


Proposed fault detection mechanism for (single) transient faults; demonstrated for an exemplary **Equivalence Property**. Consists of (a) *Equivalence Comparator* for a partition of flip-flops (determined by SAT-based methods) and (b) *Activator* observing the current state of the circuit (derived from BMC-driven analysis).

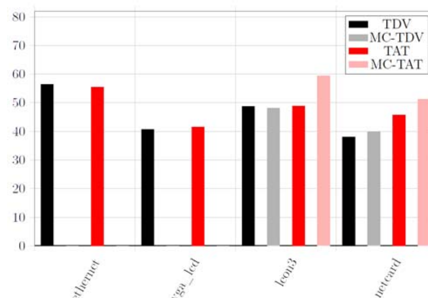
Experimental Evaluation and Conclusion

Test Data Volume (TDV) and Test Application Time (TAT) reduction ratio [%]

IEEE 1149.1 with Embedded Compression

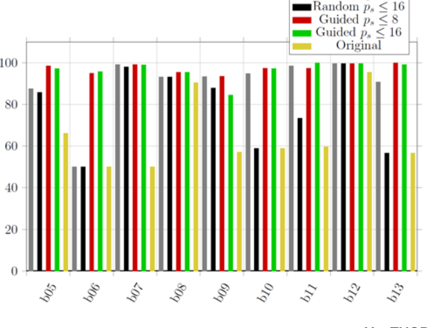


Hybrid Multichannel (MC) Compression for Low-Pin Count Test Applications



Robustness of Design [%]

Single Event Upset Faults



The experimental evaluation of industrial-sized designs clearly shows that a significant compression ratio by up to 67.4% and a test application time reduction by up to 65.7% can be achieved for both IEEE 1149.1 with embedded compression and state-of-the-art embedded compression techniques that utilize the hybrid architecture. The proposed reliability measure allows for enhancing the robustness of benchmark circuits by up to 98%.

VecTHOR's Retargeting Framework

References and Acknowledgment

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