Karlsruhe Institute of Technology

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Chair for Embedded Systems

Automated Design of Approximate Accelerators

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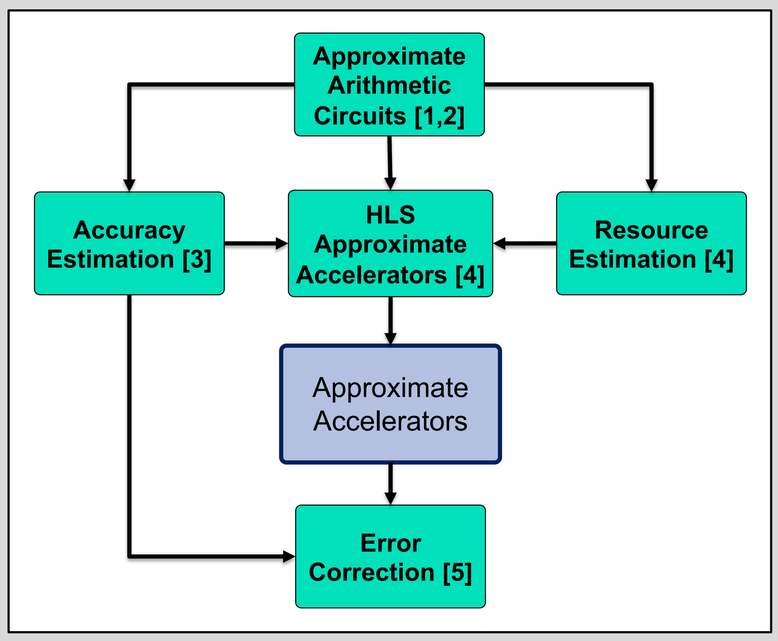
Motivation and Contribution

With the emergence of the approximate computing paradigm, many approximate functional units have been reported in the literature, mainly approximate adders and multipliers.

Challenge:
Given a design for an error-tolerant application and a set of approximate components, which approximate arithmetic circuits should be used to minimize the computational effort (e.g., energy), while satisfying a defined accuracy?

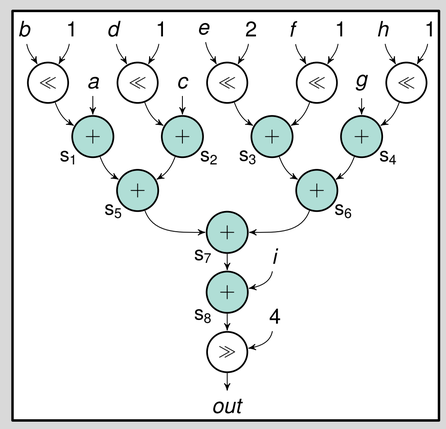


Contributions

Accuracy Estimation

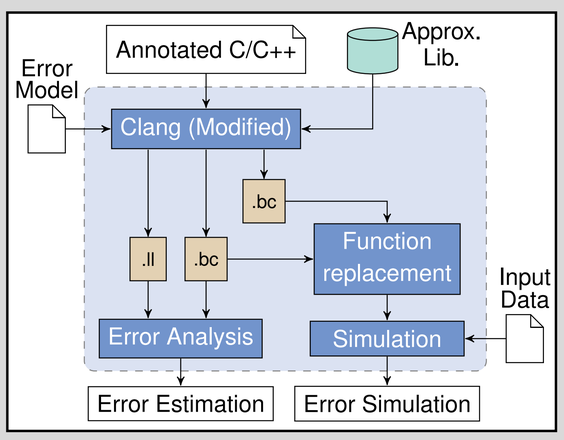
The design of approximate accelerators, particularly using approximate arithmetic circuits, requires methods to estimate the accuracy at the output.

- How the errors introduced by an approximate addition propagate up to the output?
- How these and other errors interact with other accurate and approximate computations.
- Models to define how errors propagate are required.



3x3 Gaussian filter

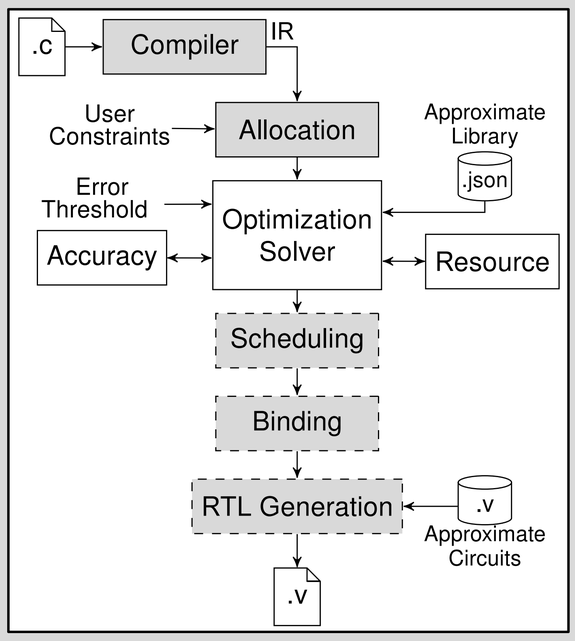
Goal: Automate the accuracy evaluation of approximate designs without requiring exhausting simulations [3].



- CEDA: Compiler-driven Error Analysis for Designing Approximate Accelerators
- Software model of accelerator is used.
- DFG representation is extracted from LLVM IR.
- Then analysis is performed.

High-Level Synthesis Generation

Repetitive gate-level simulations and circuit synthesis consume a significant time to explore many, or even all, possible designs for an approximate accelerator, given set of approximate arithmetic circuits.



Goal: automated framework for HLS of approximate accelerators using a given library of approximate arithmetic circuits and relying on analytical models [4].

DSE methodology finds Pareto-optimal solutions for approximate accelerator designs, minimizing the required resources while meeting accuracy constraints.

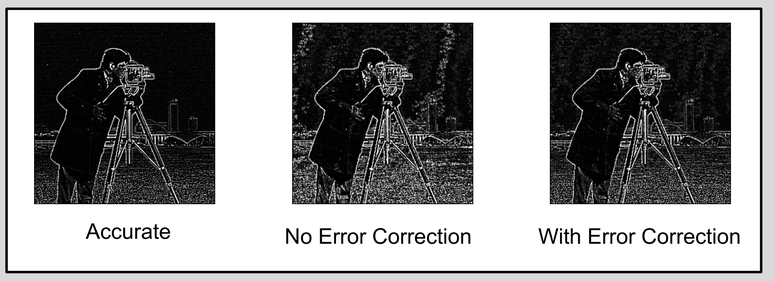
Approximate designs for different MED targets.

Less energy required, with more error tolerance, but meeting accuracy constraint.

MED	PDP [μW·ns]	PDP (Norm.)	PSNR [dB]	SSIM
		Sobel		
0	6420.57	1	∞	1
5	4461.26	0.69	29.86	0.84
11	3985.95	0.62	22.44	0.65
16	3912.11	0.61	19.52	0.58
23	3679.43	0.57	18.50	0.54
		Sharpen		
0	13202.22	1	∞	1
5	9212.01	0.70	36.00	0.98
15	8526.78	0.65	24.50	0.91
20	8120.10	0.62	21.61	0.84
30	7471.01	0.57	17.99	0.76

Selective Error Correction

For approximate accelerators, an accuracy limit must be defined and satisfied [3].

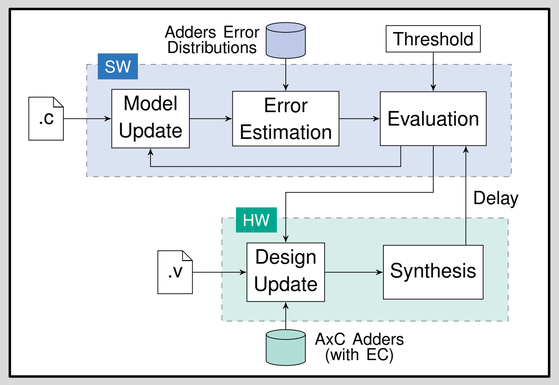


Accurate | No Error Correction | With Error Correction

Performance decreases from 2.1x to 1.7x for this Laplace filer example, as accelerator results with errors with ED > 90 are re-computed.

Goal: Improve application performance while introducing selective error correction at approximate adder and reducing the required re-computations [5].

ECAx: Error Correction for Approximate Accelerators



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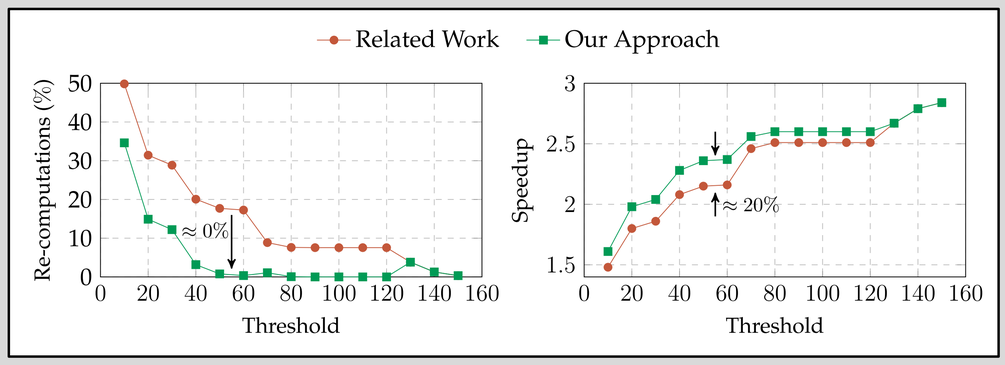

[1] D. Hernández-Araya, J. Castro-Godínez, M. Shafique, and J. Henkel. “AUGER: A Tool for Generating Approximate Arithmetic Circuits,” in *LASCAS*, 2020.
[2] J. Castro-Godínez, H. Barrantes-García, M. Shafique, and J. Henkel. “AxLS: An Open-Source Framework for Netlist Transformation Approximate Logic Synthesis,” in *WOSET*, 2020.
[3] J. Castro-Godínez, S. Esser, M. Shafique, S. Pagani, and J. Henkel. “Compiler-driven error analysis for designing approximate accelerators,” in *DATE*, 2018.
[4] J. Castro-Godínez, J. Mateus-Vargas, M. Shafique, and J. Henkel. “AxHLS: Design Space Exploration and High-Level Synthesis of Approximate Accelerators using Approximate Functional Units and Analytical Models,” in *ICCAD*, 2020.
[5] J. Castro-Godínez, M. Shafique, J. Henkel. “ECAx: Balancing Error Correction Costs in Approximate Accelerators,” in *ACM TECS, ESWeek Special Issue*, 2019.

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