Statistical Modeling with the Virtual Source MOSFET Model

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Abstract—A statistical extension of the ultra-compact Virtual Source (VS) MOSFET model is developed here for the first time. The characterization uses a statistical extraction technique based on the backward propagation of variance (BPV) with variability parameters derived directly from the nominal VS model. The resulting statistical VS model is extensively validated using Monte Carlo simulations, and the statistical distributions of several figures of merit for logic and memory cells are compared with those of a BSIM model from a 40-nm CMOS industrial design kit. The comparisons show almost identical distributions with distinct run time advantages for the statistical VS model. Additional simulations show that the statistical VS model accurately captures non-Gaussian features that are important for low-power designs.

I. INTRODUCTION

Continued scaling of CMOS technology has introduced increased variations of process and design parameters, which profoundly affect all aspects of circuit performance [1]. While statistical modeling addresses the need for high product yield and performance, it inevitably increases the cost of computation. This problem is further exacerbated as future digital design becomes larger and more complex. Therefore, the simplicity of device models is a key factor in effective statistical design flows. Current compact transistor models consist of a large number of parameters and complex equations which do capture many (if not all) of the physical short-channel effects, but significantly slow down the simulation speed [2]. A distinct benefit of the ultra compact, charge-based statistical virtual source (VS) MOSFET model is that it directly addresses both the complexity and simulation problems of statistical circuit analysis for nanoscale CMOS devices [3] [4]. Indeed, it provides a simple, physics-based description of carrier transport in modern short-channel MOSFETs along with the capability of mapping the variability characterization in device behavior onto a limited number of underlying model parameters, which in turn enables the efficient prediction of variations in circuit performance.

The core of the ultra compact VS model is a simple physical description of channel minority carrier charges at the virtual source. It essentially substitutes the quasi-ballistic carrier transport concept for the concept of drift-diffusion with velocity-saturation. In doing so, it achieves excellent accuracy for the I-V and C-V characteristics of the device throughout the various domains of circuit operation. The number of parameters needed is considerably fewer (11 for DC and 24 in total) than in conventional models.

In this paper, we present the first derivation and validation of the statistical VS model. The development of the model is centered on a statistical extraction technique called the Backward Propagation of Variance (BPV) [5]. Although this is performed for the nominal $V_{dd}$, the resulting statistical model is valid over a whole range of $V_{dd}$’s, thus enabling the efficient analysis of power-delay tradeoffs in the presence of parameter variations.

The method we describe in this paper is applied to characterize the within-die (e.g., geometry-dependent) variability component due to manufacturing variations. It is well known that for the deeply-scaled technologies (65-nm CMOS and beyond), where the VS model is most appropriate, within-die variations can dominate inter-die (i.e., global) variations. However, the general idea of BPV could be applied to inter-die variation as well.

II. VIRTUAL SOURCE CHARGE-BASED COMPACT MODEL

A. Review of the VS Model Equations

The core concept of the Virtual Source (VS) compact model is that as the MOSFET operation in saturation approaches the ballistic limit, the virtual source velocity $v_{xo}$ becomes independent of $V_{ds}$ except for the drain-induced barrier lowering (DIBL) effects. This behavior is to be contrasted with the drift-diffusion transport model where the velocity is directly proportional to the electrical field $E$ and becomes saturated as the electrical field $E$ passes beyond a critical value.

In saturation, the drain current $I_D$ is calculated as the product of the charge areal density $Q_{ixo}$ and the channel-injected carrier velocity $v_{xo}$ at the virtual source

$$I_D = F_s \cdot Q_{ixo} \cdot v_{xo} \tag{1}$$

The function $F_s$ is to account for non-saturation and provides continuity across all regions of operation

$$F_s = \frac{V_{ds}}{V_{dsat}} \left(1 + \left(\frac{V_{ds}}{V_{dsat}}\right)^\beta\right)^{1/\beta} \tag{2}$$

$\beta$ is a fitting parameter with a typical value of 1.8 [3].

B. Parameter Variations in VS Model

To support statistical circuit simulation, the measured IV and CV statistics need to be converted into variations of a complete set of independent VS model parameters. For modern MOSFETs, the primary sources of within-die variations include random dopant fluctuation (RDF), line-edge roughness (LER) and oxide thickness fluctuation (OTF) as well as local fluctuations of mechanical stress. To maintain the simplicity of the statistical VS model, we relate most of its parameters directly to standard device measurements rather than to manufacturing process parameters. The VS model parameters used for statistical modeling are listed in Table I. In the VS model, the threshold voltage is modeled as

$$V_T = V_{T0} - \delta(L_{eff})V_{DS} \tag{3}$$

where $\delta(L_{eff})$ is the $L_{eff}$-dependent DIBL coefficient [3]. The threshold voltage variation in Table I is determined by the variations in implantation energy and dose as well as fluctuations in substrate doping. These effects are modeled through variation in $V_{T0}$ while length-dependent threshold

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where the subscript $p$ represents a parameter process such as effective channel length and width. For local mismatch, we have $\sigma_L = \sigma_{L_{eff}}$ and $\sigma_W = \sigma_{W_{eff}}$ and a complete equation considering the geometric dependence of each parameter is

$$\begin{bmatrix}
\sigma_{V_{th}} \\
\sigma_L \\
\sigma_W \\
\sigma_{\mu} \\
\sigma_{C_{inv}}
\end{bmatrix} = \begin{bmatrix}
\alpha_1 \quad \alpha_2 \quad \alpha_3 \quad \alpha_4 \quad \alpha_5
\end{bmatrix} \begin{bmatrix}
\sqrt{\frac{\sigma_{V_{th}}}{LW}} \\
\sqrt{\frac{\sigma_L}{LW}} \\
\sqrt{\frac{\sigma_W}{LW}} \\
\sqrt{\frac{\sigma_{\mu}}{LW}} \\
\sqrt{\frac{\sigma_{C_{inv}}}{LW}}
\end{bmatrix}$$

The ultimate goal of this statistical modeling is to extract a group of $\alpha_{1-5}$ that is appropriate for all transistor geometries and that match the statistical circuit performance. The mismatch variances of $p_j$ cannot be characterized directly from measurement or device simulations. Instead, variations $\sigma_{V_{th}} (i = 1, 2, ..., m)$ of electrical performance parameters (e.g., $I_{dsat}$, $I_{off}$, etc.) are measured under different geometry and bias conditions and the $\sigma_{p_j}$ are calculated from BPV [5] according to the formula

$$\sigma_{V_{th}}^2 = \sum_{j=1}^{n} \left( \frac{\partial V_{th}}{\partial p_j} \right)^2 \sigma_{p_j}^2 \tag{8}$$

Here $p_j$ and $p_k$ for any $j \neq k$ is assumed to be independent since we successfully decoupled variation sources into independent variation parameters in the VS model in Section II(B). Equation (8) assumes Gaussian distributions for both groups of $\{\epsilon_i\}$ and $\{p_j\}$. This assumption requires a careful selection of both $\{\epsilon_i\}$ and $\{p_j\}. In our work and unlike the statistical modeling approach of [5], $\epsilon_i$ is not applicable for all bias conditions. Other bias conditions such as $I_{th}$ at the transition region between linear and saturation, or $L_{eff}$ are not appropriate $\{\epsilon_i\}$ because they do not strictly follow a Gaussian distribution.

The accuracy of Equation (8) hinges on the validity of approximating the electrical performance parameters as linear functions of the process parameters. We have found that such linear approximation is sufficiently accurate to extract $\sigma_{p_j}$.

A system of linear equations is set up after stacking a group of equations with different transistor sizes, as is shown in (9). The sensitivity matrix in (9) is calculated from SPICE simulation using the VS model. Virtual source velocity is not considered as a separate variation parameter in Equation (9) since its effect has been captured in the variation of $L_{eff}$ and $\mu$. Also, silicon dioxide films are created with a thermal oxidation process which historically has been extremely tightly controlled [9] with the $\sigma$ variation of $C_{inv}$ being less than 0.5% in our case. Because the BPV process tends to overestimate variation in tightly controlled process parameters, we directly measure $C_{inv}$ through the oxide thickness, as suggested in [10].

Since the primary intrinsic mismatch corresponding to gate length and width variation is due to line edge roughness (LER), which is caused by etching and sub-wavelength lithographic process, it is reasonable to assume the same roughness for both length and width. Therefore an empirical relationship $\alpha_2 = \alpha_3 (\sigma_L/\sigma_W = L/W)$ is assumed to further reduce the unknown parameters in (9). A good match to data is achieved ($\alpha_2/\alpha_3 = 0.95 - 0.99$ under different geometries) in a 40-nm CMOS technology.

IV. VERIFICATION

To validate the accuracy of the VS statistical model as well as the statistical extraction method, we implement it using Verilog-A under the Cadence Virtuoso Design Environment. The method described in Section III was applied to characterize the SPICE-level benchmark circuit statistics of a 40-nm bulk CMOS technology. Although the BPV method is applicable to measurement data, here we have employed a BSIM based industrial design kit to validate the proposed VS statistical model. Various Monte Carlo simulations were performed, including several geometries of MOSFETs and different electrical tests (IV and CV). The sample sizes are more than 1000 to characterize the statistical variation and correlation for $\epsilon_i$. The extracted parameter statistics $\alpha_{1-5}$ are listed in Table II.

A. Validation of Device Variability

The percentage differences of $\sigma/\mu$ for $I_{dsat}$ mismatch and the underlying process parameter contributions are shown in Fig. 1(a). Compared with previous results in a similar technology [11], we observe a similar extracted $\sigma_{V_{th}}/\mu_{V_{th}}$ and $\sigma_{\mu_{L_{eff}}}/\mu_{L_{eff}}$ but smaller $\sigma_{\mu}/\mu_{\mu}$ in the VS model. The latter result is due to the fact that in the context of the VS model,
mobility and virtual source velocity have meanings that differ with those of [11]. $I_{dsat}$ and $\log\alpha I_{eff}$ bivariate scatter plots for BSIM model and 1σ, 2σ and 3σ confidence ellipses for both the VS and BSIM models are shown in Fig. 1(b). Note that in the statistical VS model, the generated variation parameters $I_{eff}$, $V_{T0}$, and $\mu$ are non-correlated. This behavior confirms that the $I_{dsat}$ and $\log\alpha I_{eff}$ variations are fully decoupled during the statistical extraction procedure.

### B. Statistical Validation Using Benchmark Circuits

We have performed statistical experiments on both the BSIM model and the VS model using a set of benchmark circuits, including standard library logic cells (INV, NAND2, DFF, etc.) and an SRAM cell. Our first standard cell is a fanout-of-3 static INV gate having different geometries, as shown in Fig. 2. The $V_{dd}$ in all cases is 0.9V which is the standard supply voltage for this particular technology. Excellent matching is achieved across a wide range of transistor sizes, which confirms that the geometric dependencies of the VS variation are well characterized. It is important to note that our statistical extraction procedure remains valid regardless of the specific functional dependence of the variations on device geometry.

Our second standard cell is a fanout-of-3 static NAND2 gate operating under a $V_{dd}$ of 0.9V, 0.7V and 0.55V. Although power consumption decreases with supply voltage, local variations increase significantly, and as a result parametric yield is decreased. Even worse, the probability density of the delay becomes highly non-Gaussian at low supply voltage, and as a result, the application of statistical static timing analysis (SSTA) becomes more difficult [12]. Although all variation parameters in the VS model are assumed to be independent Gaussian variables, the non-Gaussian property of the delay distribution becomes correctly captured, as is shown in Fig. 3. The quantile-quantile plot for delay variation starts to deviate from a linear relationship when $V_{dd} = 0.7V$, and the non-linearity becomes pronounced at $V_{dd} = 0.55V$. In both cases, the VS prediction shows a good match with the BSIM model at the 3σ scale. Unlike the PSP model [13] where variances of extra electrical performance parameters have to be added to match the variance at different $V_{gss}$, no extra statistical fitting is needed in the VS model to adjust timing distributions in cases dynamic voltage scaling is used.

After verifying the approach on combinational logic cells, we now extend it to perform setup and hold time analysis on a D flip-flop. The schematic of the benchmark master-slave register is shown in Fig. 4(a). Fig. 4(b) shows a typical timing path for setup/hold analysis. The PDF’s for setup/hold time for the registers simulated from VS model and BSIM models are shown in Fig. 4(c). One important note is that the characterization of the setup/hold time requires about 20 times more SPICE simulations than those of a combinational cell having the same number of transistors. This is because the setup/hold time can only be measured indirectly by varying clock to input signal delay. The ultra compact VS model plays a more important role in this case where tens of thousands of SPICE simulations are required.
The last circuit in our validation is a 6T SRAM cell, which is known to be highly sensitive to within-die variations, as shown in Fig. 5. Both the VS and BSIM models are employed to simulate the variability in SRAM READ and HOLD Static Noise Margin (SNM). The characteristic butterfly patterns generated with the statistical VS model are shown in Fig. 5 (a) and (d), for READ and HOLD, respectively. The SNM comparisons between the two models for READ and HOLD are shown in Fig. 5 (b) and (e). Even with this highly sensitive analog circuit, the ultra-compact statistical VS model provides an excellent match to the “golden” BSIM model. In Fig. 5 (f), the quantile-quantile plot for SRAM HOLD SNR using both models shows a slight non-Gaussian distribution.

Finally, the runtime speedup of the VS model (Verilog-A) with respect to BSIM4 (C code) is shown in Table III. We notice a 4.2× speedup and 8.7× reduction in memory usage. These favorable results can be further improved using an optimized C code implementation of the VS model in line with the optimized C code used for BSIM4.

V. CONCLUSION

In this paper, we have described the first statistical extension of the ultra-compact Virtual Source (VS) MOSFET model. The derivation of the statistical model is based on the backward propagation of variance (BPV), and nanometer-regime variation sources are mapped onto independent VS model parameters. The statistical VS model is validated in reference to a “golden” 40nm BSIM model using extensive Monte Carlo runs.

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REFERENCES