A 14 bit, 280 kS/s Cyclic ADC with 100 dB SFDR

Thomas Froehlich, Vivek Sharma, Markus Bingesser
Austriamicrosystems Switzerland AG
Rapperswil Switzerland

Abstract— **This paper presents the design of a 14 bit, 280 kS/s cyclic ADC which consumes 1.6 mW power and achieves 100 dB SFDR. The design is optimized with a half-scale residue transfer characteristic (RTC) which lowers swing and slew requirements on the opamp. Further advantages of this RTC are exploited to reduce the number and magnitude of dominant error sources, and the residual error is randomized with dithering. Capacitor scaling and optimized allocation of conversion time to each step add to power savings. The ADC fabricated in a 0.35 µm CMOS process occupies 1.04 mm^2 silicon area.**

Cyclic analog-to-digital converter (ADC); half-scale residue transfer characteristic (RTC); residue amplifier (RA); dithering; integral nonlinearity (INL); differential nonlinearity (DNL)

I. INTRODUCTION

Medium resolution (12-16 bits) ADCs sampling at less than 1 MS/s find widespread use, particularly in sensor frontends. Portability is important and power consumption must be kept under a few milliwatts. ΔΣ ADCs offer reduced sensitivity to element mismatch, but are unable to provide one-one correlation between input and output, which is an important requirement in sensor systems operating in closed loop configuration. Nyquist-rate converters score better on this point but require great care to minimize effects of element mismatch beyond 10 bit resolution. Successive approximation register (SAR) based ADCs offer good power efficiency but require a large DAC beyond 10 bits for matching reasons, and also accumulate maximum error at midscale, limiting small-signal linearity and SFDR. Cyclic ADCs consume a bit more power but offer a compact solution with more degrees of freedom.

In this work, the design of a 14 bit, 280 kS/s cyclic ADC is described. The principle of operation is shown in Fig. 1. At each step of the conversion, a small flash ADC with some redundancy digitizes the input IN to a digital code D, and a residue amplifier (RA) scales up the difference between IN and an analog representation of D, which is the input to the next step [1]. The digital outputs from various steps are combined to get the final code. The primary sources of error are: (1) Finite gain and settling errors in the opamp (2) Element mismatch in the RA causing INL/DNL and (3) Thermal noise in the switches and opamp. The choice of the RA transfer characteristic (RTC) and RA gain are crucial to optimizing power consumption, speed, area, linearity and design effort [2].

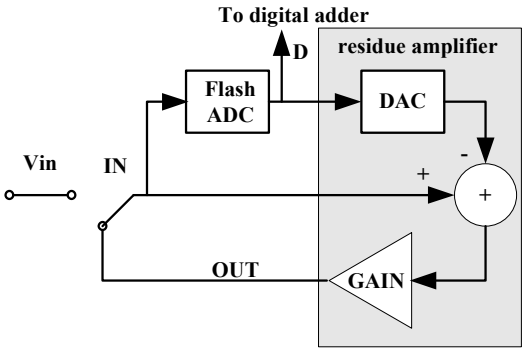

Figure 1. Simplified diagram of the cyclic ADC. All elements are sampled systems, the sample-and-holds not shown explicitly. The residue amplifier (RA) is realized with a switched-capacitor (SC) network and an opamp.

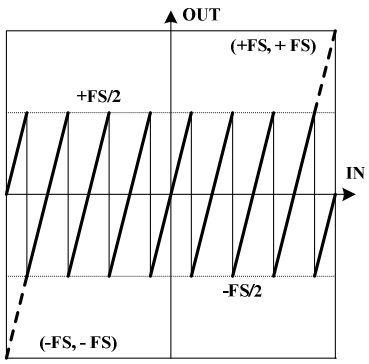

Figure 2. Half-scale residue transfer curve (RTC) of the cyclic ADC stage used in this work. Conventional full-scale RTC (mostly overlapping) is shown dashed.

II. ADC DESIGN DETAILS

A. Architecture optimization for noise, power, linearity

Capacitor size must be increased to reduce thermal noise and mismatch-related INL/DNL. Opamp gain, slew rate and settling speed must be increased to suppress systematic INL/DNL. Power consumption is minimized with smaller capacitance and a reduced slew and speed requirement on the opamp. Higher RA gain reduces contribution of errors from later steps but reduces the feedback factor (speed) of the RA. An RA gain of 4 was found to be optimal for this work.

The RA structure was chosen to minimize the number of dominant error terms. The half-scale RTC of Fig. 2 was

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chosen. The output swing of the RA is ± FS/2, compared to ± FS for a conventional RA, FS denoting full-scale level. This reduces slew and swing requirements on the opamp in the RA, and causes less gain compression as described in [3]. Another advantage not described in [3] lies in the fact that no input signal causes large errors in all conversion steps simultaneously. To see this, consider input signals approaching ± FS, where the RA output is always > ± FS/2. These give similar and correlated gain compression errors, which worsen INL rapidly unless the RA is overdesigned to cope with this. The RTC used in this work guarantees that any conversion step resulting in the peak output (around ± FS/2) is immediately followed by steps with almost zero output where there is no nonlinearity, and thus there is only one dominant step with nonlinear error. The gain of 4 per step means that only the first conversion step contributes appreciable nonlinear error, and noise. It also ensures that input signals < -20 dBFS fall in one single segment of the RTC, eliminating the effect of element mismatch in the first conversion step. This combined with a split residue amplifier structure [4] with an inherently linear 2-level DAC boosts small-signal linearity of the ADC significantly.

B. Circuit design issues

The cyclic ADC operation and the RTC of Fig. 2 are realized with a switched-capacitor (SC) amplifier with 8 unit element poly-poly capacitors (Fig. 3). With a gain of 4, 7 conversion steps are needed for 14 bit resolution. Ideally, two capacitor banks are enough, one each for the even and odd cycles of operation. We use three banks: the first bank with a 250 fF unit capacitor to reduce mismatch and noise for the first conversion step, and two banks with a unit capacitor of 125 fF for the remaining steps to save area and power. To suppress the residual DNL, a dithering scheme is used where all the comparator thresholds are shifted left/right randomly as shown in Fig. 4, controlled by an on-chip PRBS generator. In case of oversampled signals this spreads the DNL, reducing the peak value, without increasing overall noise [5].

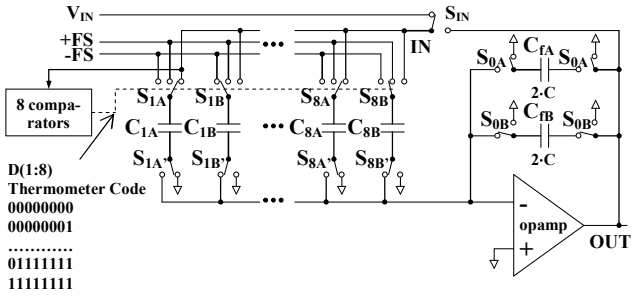

Figure 3. Simplified schematic of the cyclic ADC shown single-ended with only 2 capacitor banks A & B, which alternate between sampling the output of the RA, and connecting across the opamp to realize the RTC.

The RA uses a differential, folded cascode opamp with SC common-mode feedback. The gain is boosted to > 120 dB [6]. The opamp noise is optimized by minimizing transconductance in all active loads as much as allowed by signal swing constraints. Impact ionization in the cascode transistors is avoided with non-minimum channel length and output common mode selection [7]. The same opamp is used for all steps, but more time is allowed for the first step where the capacitors are 2 x larger and accuracy is more important [8]. The settling accuracy of the RA is > 107 dB for removing its effect from overall INL/DNL and for reduced temperature sensitivity. CMOS transmission gates are used as switches with bottom-plate sampling to reduce effects of charge injection [9]. The capacitors were laid out for good matching. Extensive shielding eliminates cross-coupling capacitances, but significantly increases the overall parasitic capacitance, causing a sizeable increase in overall current consumption, a price for precise matching.

Comparator offset is not critical. However, it shifts the RTC from its ideal level increasing the output swing of the RA. To minimize the impact of this, the opamp was designed for 20 % more output swing, and comparator offset suppressed with output offset cancellation [10]. A fully differential, capacitively-coupled comparator with 2 preamplifier stages was used, which also allows easy dithering. Attention was paid not to discharge any signal charge into the references or threshold voltages. Finally, chopping was used to up-convert low-frequency 1/f noise for enhanced DC accuracy [9].

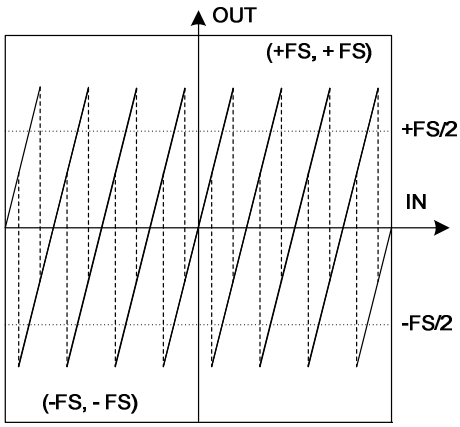

Figure 4. Dithering principle. All comparator thresholds are randomly shifted right or left together based on a PRBS output.

III. SIMULATION METHODS AND RESULTS

This section covers the simulation strategy used to achieve first time right silicon performance.

A. Simulation Strategy

The aim was to verify performance parameters directly relevant to the ADC performance such as noise and INL/DNL with high-level models as much as possible. Therefore a top-down modeling strategy was used. This included an optimization loop using hand estimations and top-level simulations to find the best solution concerning quantization noise, thermal noise of the SC network and opamp, and nonlinearities related to element mismatch. In the next step, the architectural design was implemented in a block structure with a behavioral model for each cell. Step by step each behavioral model was then replaced with its basic design to run transistor simulations on it. Post-layout simulations ensured the

identification and reduction of layout parasitics or asymmetries. Worst-case and statistical simulations were done to assure high yield and proper operation across all conditions.

B. *Linearity Simulations*

Systematic INL and DNL due to RA gain and settling errors are simulated directly for the RA at transistor level at all corners by observing the output around each transition of the RTC, followed by statistical simulations at the worst corner for mismatch-induced INL/DNL. These give an estimation of the overall ADC INL/DNL and information about the worst corner.

The INL/DNL of the overall ADC (Fig. 5) were also estimated around each transition points and the zero crossings. For this, the comparators of the DAC in the RA were forced to the desired state at the first conversion step. The INL is calculated by the difference of the digital representation of the residue voltage of the last conversion step minus the ideal expected ADC output value. 20 statistical runs are simulated at the worst corner (Fig. 5). An uncorrelated run with 2.5 x capacitor mismatch coefficients were used to improve coverage (Fig. 6).

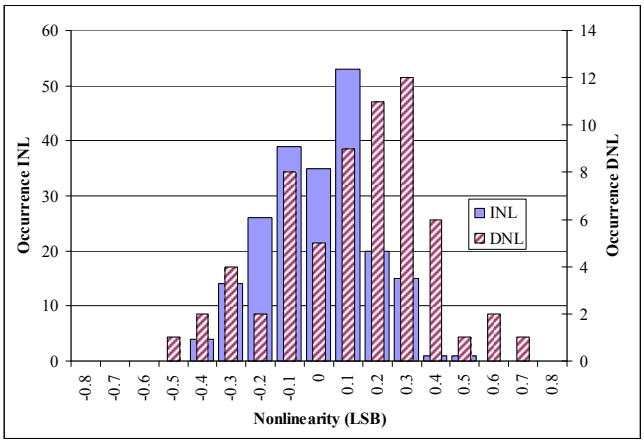

Figure 5. Simulated INL/DNL distribution over 20 statistical runs.

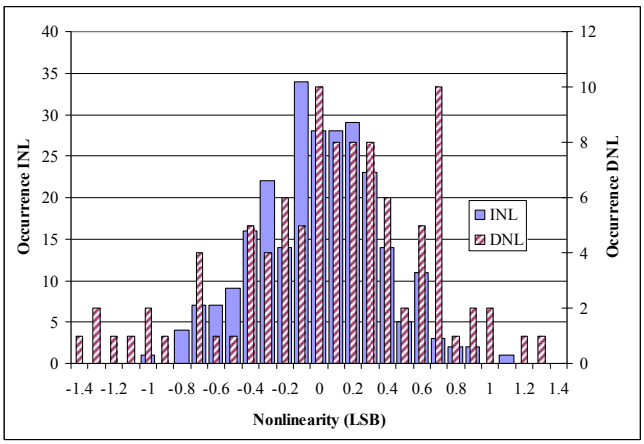

Figure 6. Simulated INL/DNL distribution over 20 statistical runs with 2.5 x worse capacitor matching.

C. *Simulation Summary*

Table I summarizes the relevant simulation results.

TABLE I. SIMULATION SUMMARY

Parameter	Specification	Simulation	Notes
INL	±4 LSB ±1.5 LSB	±1.2 LSB ±0.7 LSB	±FS range ±FS/10 range
DNL	±2 LSB ±1 LSB	±1.4 LSB ±0.8 LSB	±FS range ±FS/10 range
RA settling accuracy	103 dB	> 107 dB	
Total Noise	98 µVrms	70 µVrms	

IV. LAYOUT

In the die photo on Fig. 7 the 3 pairs of capacitor banks are well visible with the RA in the center. The capacitor banks are arranged in such a way, that the main unit capacitor elements as well as the connecting switches and the sensitive interconnect are matched perfectly with each other. The RA is placed in the center of the capacitor arrays to reduce routing length. Nevertheless a significant part of the total ADC area is consumed by the interconnect of the capacitor arrays to the RA and the digital control signals. The reason is, that many critical nets had to be shielded against each other and the shields had to be placed moderately apart from the signal net in order to prevent excessive capacitive loading of the sensitive nets.

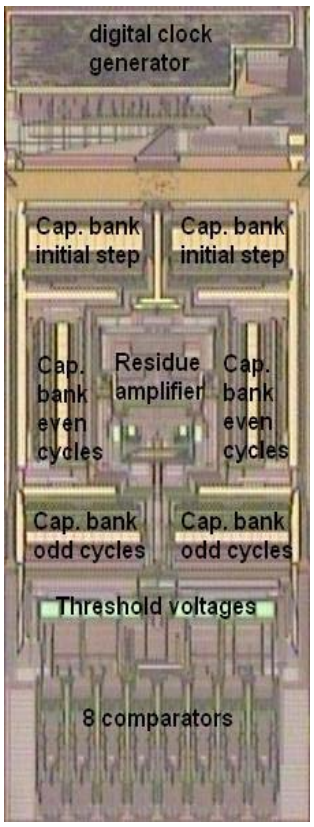

Figure 7. Die photo of the ADC

IV. MEASUREMENT RESULTS

The ADC fabricated in a 0.35 µm double-poly three metal CMOS process occupies 1.04 mm^2 area and consumes 1.6 mW power at 3.3 V with a conversion time of 3.56 µs. INL < 2.11 LSBs and DNL < 0.55 LSBs are achieved (Fig. 8). These are measured by histogram testing with a triangular wave input at 200 Hz.

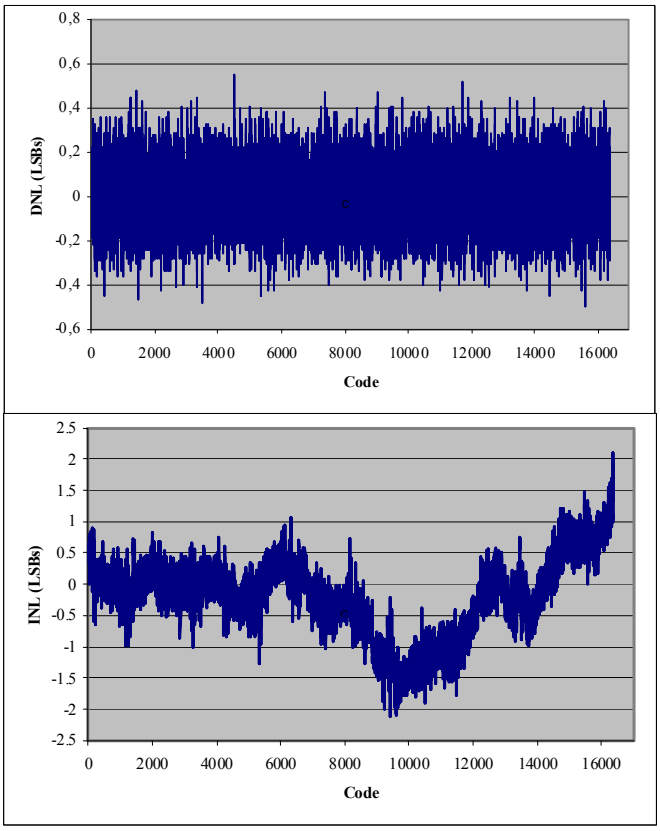

Figure 8. Measured INL/DNL.

SNR and SFDR were measured with a 240Hz input sine wave. Dynamic performance is shown in Fig. 9

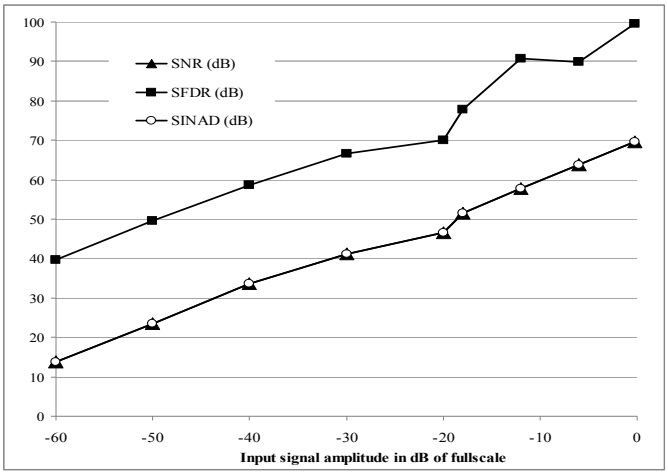

Figure 9. Measured performance vs. input. Setup noise limits SINAD.

The overall ADC performance is summarized in table II. The measured SNR is poorer than expected, limiting SINAD. Part of the excess noise appears to come from the input drivers external to the chip. This is confirmed by an idle channel noise test where the ADC inputs are tied to an internal common mode reference, causing a drop of 5.17 dB in the measured noise. An additional noise contributor was found to be a parasitic coupling capacitor between the digital output lines of the flash ADC and the input of the RA. After removing the coupling in a redesign, the idle channel noise went further down by another 4.6 dB.

TABLE II

PERFORMANCE SUMMARY	
Resolution	14 bit
Conversion rate (Fs)	280 kS/s
Supply voltage	3.3 V (analog) 1.8V (digital)
Active area	1.04 mm^2
Total power consumption	1.6 mW
SINAD / SFDR	69.6 dB / 99.6 dB
INL / DNL	2.11 LSB / 0.55 LSB
RMS Noise with ADC inputs shorted (1 Hz … 60 kHz)	-79.4 dBFS

TABLE III

FIGURE OF MERIT [11] COMPARISON	
[12] 16 b 1 MS/s	4.5 pJ/step
[8] 12 b 5 MS/s	9.3 pJ/step
[13] 12 b 42 kS/s	0.9 pJ/step
[14] 12 b 3.3 MS/s	1.2 pJ/step
[This work] 14 b 280 kS/s (corrected for setup noise after redesign)	0.75 pJ/step

A comparison to some recent publications on comparable cyclic ADCs shows that the present work attains a respectable figure of merit (FOM = Power/(2^{ENOB}·Fs)) at 2.29 pJ/step. If we use the idle channel noise for SNR calculation, this figure would drop to 0.75 pJ/step. Note that this commonly used definition [11] gives a poorer FOM for higher resolution noise limited ADCs since doubling the SNR requires 4x power increase and not just 2x.

The power efficiency of this ADC could be improved another factor 2-3 by using telescopic cascode opamps and MIM capacitors. Also based on the achieved SFDR it would be possible to extend the resolution to 15 or 16 bits by adding an additional conversion step.

V. CONCLUSION

The above work demonstrates advantages of a half-scale residue transfer characteristic beyond those described in the literature. Its successful application to the design of a 14 bit, 280 kS/s ADC achieving 0.75 pJ/step power efficiency is also presented. Techniques like optimal RA gain selection, capacitor scaling, optimal allocation of cycle time to each conversion step and dithering were used to realize the high level of power efficiency.

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