The Road to Energy-Efficient Systems: From Hardware-Driven to Software-Defined

Cool Electronic Systems Special Day Panel Session

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Abstract—Innovations in micro and nano technology form the basis of modern ICT. However, the steady growth in the ICT sector has meanwhile a significant ecological footprint: 2% of global CO2 emissions are due to ICT systems already today - one fourth of the emissions caused by cars. The energy costs for running ICT infrastructure have turned into a significant economical factor. The most urgent challenge in the area of micro and nanotechnology is therefore to massively increase energy efficiency, in particular for ICT as a key sector for economic growth. Significant improvements in this area can only be achieved through disruptive innovations and new system approaches, which rely on a combination of excellent research & development and world leading know-how of semiconductor production.

But will hardware be the driver to fulfill these requirements and software has to adapt to whatever hardware concepts are developed? Or should the ability to program systems energy-efficiently define the design of the hardware architecture? This session will present the different perspectives on the problem and try to bring both sides together.

PANELISTS

Heinrich Meyr, RWTH Aachen, DE

To increase energy efficiency we must first of all concentrate on those parts of electronic systems which offer the greatest potential for improvement. For mobile applications and multimedia these parts are truly innovative, massively parallel and heterogeneous HW-architectures. And we must be acutely aware that energy efficiency and ease of programming are conflicting goals. We must not repeat the mistake of the early days of digital signal processors: to design architectures for which it is impossible to write good compilers. We must follow a joint architecture-tools design approach.

Jan Rabaey, UC Berkeley, US

Many techniques for low-power design developed over the past decades are quickly running out of steam. Getting one or more orders of magnitude improvements in energy efficiency will be very hard, unless novel device structures with a sharper on-off transition are adopted. There is however a low-hanging fruit still to be harvested: doing “nothing” well. The vast majority of electronic systems rarely operate at maximum performance - operational loads typically are way below 50%. However, the energy-efficiency of most systems (work delivered over energy consumed) drops substantially at lower workloads. By making our electronic systems doing nothing (or little) well, major energy savings can be contained. This however requires a multi-layer system level solution.

Gerd Teepe, Globalfoundries, DE

Technology progress leads to higher integrations densities and thus there is a natural dividend from Moore’s Law. However, whether this dividend is used for higher performance systems or for lower power devices is decided by the system. Today, we have not exhausted all measures for lower power designs, as we are struggling with the additional complexities associated to low-power IC-designs. Staring at the power consumption of semiconductor devices, however, will make us miss the point: There is much more to be gained from the application of microelectronics to our “old economy power consumers” than from the consumption of electronics itself.

Kees Vissers, Xilinx, US

Many programmers have no idea of the power consumption of their program. Historically the focus has been on execution time and lately with multi-cores on speedup. The importance of flexibility and programming can not be underestimated. In this panel I will show that the power consumption of FPGAs programmed exclusively in C or C++ is very attractive compared to a processor core and multi-core architectures for the next generation communication standards. This will offer the system designer another option in achieving fully programmable, high-throughput real-time systems at the lowest total cost of ownership for software defined real-time systems.

Wolfgang Fichtner, ETH Zurich, CH