

Periodic Steady-State Analysis Augmented with Design Equality Constraints

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Abstract—A design-oriented periodic steady-state analysis is presented in this paper. The new analysis finds the values of circuit parameters that result in a desired circuit performance specified by a set of equality constraints. This is done by including the design equality constraints and the circuit parameters directly in the steady-state analysis as additional equations and unknowns. A time-domain finite difference method and the numerical implementation for the proposed analysis are described. Several examples demonstrate that the new analysis accurately and efficiently tunes circuit parameters that conform to a wide range of design specifications.

I. INTRODUCTION

Design specifications define various aspects of a circuit operation, including the nominal large-signal performance, sensitivity to process variations, and noise performance. A designer is interested in finding a circuit topology and parameters that result in the desired circuit performance. However, basic circuit analyses (transient, periodic steady state, small-signal ac, etc.) available in circuit simulators solve the reverse problem. Given a circuit topology and parameters, these analyses find the circuit response that provides information about a particular aspect of circuit operation. The conventional analyses determine only the performance of a circuit without any consideration for the design specifications. The designer uses these analyses in an iterative manner to improve a design and obtain the desired specifications.

The focus of this paper is on a new design-oriented analysis that also tunes the values of circuit parameters such that a circuit meets some desired objectives. Specifically, we consider the largesignal periodic steady-state (PSS) analysis [1]. The new analysis presented in this paper handles performance specifications given by design equality constraints (DECs). The design goal is achieved by performing a single PSS analysis with the constraint equations being included in the analysis. We call it PSS analysis with design equality constraints (PSS-DEC).

In prior work [2], [3], a single oscillator parameter is tuned to obtain a desired oscillation frequency. The application of PSS-SF analysis [3] is limited to analyzing oscillators with a single constraint, i.e., a specification for the oscillation frequency. The new generalized PSS-DEC formulation is capable of working with various design specifications. Furthermore, the new analysis can simultaneously tune several circuit parameters to satisfy several design specifications. The PSS-DEC analysis is an elegant and efficient approach for solving problems with equality constraints, suitable for achieving intermediate design goals. It is not an optimization technique and can not handle design specifications with inequality constraints.

The theoretical formulation of the PSS-DEC analysis is presented in Section II. In Section III, a discrete-time circuit representation suitable for computer simulation is presented. Based on this representation, the time-domain finite difference method for PSS-DEC analysis is presented. In Section IV, simulation results for a two-stage operational amplifier are given. Finally, the paper is concluded in Section V.

II. THEORETICAL FORMULATION

In this section, a conventional PSS analysis is reviewed, and the design problem with DECs is defined. The PSS and DEC formulations are then combined to obtain a continuous-time mathematical representation of the PSS-DEC analysis.

A. Periodic Steady-State (PSS)

Any nonlinear circuit can be modeled as a set of \( m \) differential-algebraic equations (DAEs) given by

\[
\frac{d}{dt} q(x(t), \Gamma_E) + f(x(t), \Gamma_E) + b(t, \Gamma_E) = 0
\]  (1)

where

\[
t \in \mathbb{R} : \text{time, independent variable},
\]

\[
x : \mathbb{R} \rightarrow \mathbb{R}^n : \text{circuit state variables},
\]

\[
\Gamma_E \in \mathbb{R}^E : \text{vector of circuit parameters},
\]

\[
q : \mathbb{R}^m \times \mathbb{R}^E \rightarrow \mathbb{R}^m : \text{contribution of resistive components},
\]

\[
f : \mathbb{R}^m \times \mathbb{R}^E \rightarrow \mathbb{R}^m : \text{contribution of reactive components},
\]

\[
b : \mathbb{R} \times \mathbb{R}^E \rightarrow \mathbb{R}^m : \text{excitations and independent sources}.
\]

The circuit parameters (components of \( \Gamma_E \)) \( \gamma_1, \ldots, \gamma_E \in \mathbb{R} \) may be design parameters, such as MOSFET geometry parameters \( W_M, L_M \), values of passive components \( R, L, C \), process parameters, or environmental parameters, such as temperature, power supply voltage, excitation parameters, load capacitance, etc.

Given a \( T_{in} \)-periodic excitation, the solution \( x(t) \) of DAEs in (1) is called the PSS solution if it satisfies \( x(t) = x(t + T_{in}) \). This periodicity constraint can be expressed as

\[
x(0) = x(T_{in})
\]  (2)

The PSS \( x(t) \) is uniquely defined by (1) and (2), resulting in the continuous-time equations for a forced circuit in the steady-state

\[
\begin{align*}
\frac{d}{dt} q(x(t), \Gamma_E) + f(x(t), \Gamma_E) + b(t, \Gamma_E) &= 0 \\
x(0) &= x(T_{in})
\end{align*}
\]  (3)

This is a periodic boundary value problem (BVP), a special case of a two-point BVP [4].

Given a vector of parameters \( \Gamma_E \), a conventional PSS analysis finds the steady-state solution \( x(t) \)

\[
\Gamma_E \rightarrow \text{PSS} \rightarrow x(t)
\]  (4)

Once the PSS solution \( x(t) \) is found, it is postprocessed to obtain large-signal circuit performance measurements, such as the output amplitude, features of the time-domain response, frequency content of circuit signals, etc.
**B. Design Equality Constraints (DECs)**

Consider a design problem for which the values of $E$ circuit parameters $\Gamma_E$ have to be determined, such that a set of $E$ design equality constraints are satisfied. The DECs are given by

$$G_E(x(t), \Gamma_E) = 0, \quad t \in (0, T_{in}]$$

where $G_E$ is a vector-valued function in terms of the steady-state solution $x(t)$ along one period and the vector of parameters $\Gamma_E$. The individual design equality constraints are represented by scalar functions $g_1, \ldots, g_E$, such that

$$G_E = \begin{bmatrix} g_1 \\ \vdots \\ g_E \end{bmatrix}, \quad g_e = g_e(x(t), \Gamma_E), \quad e = 1, \ldots, E$$

An example of a DEC is a specification for the total harmonic distortion (THD). For a DEC that requires a THD of $1\%$

$$g_1(x(t), \Gamma_E) = \text{THD}(x(t)) - 1\%$$

Note that the THD is evaluated based on the harmonic content of the output signal in $x(t)$. Analytical expressions for $G_E$ in terms of the circuit parameters $\Gamma_E$ are not required.

In a conventional design approach, the solution to the design problem in (5) is obtained by searching for a suitable set of parameters $\Gamma_E$. This is done iteratively with the use of the conventional PSS analysis.

$$\Gamma_E \rightarrow \text{PSS} \rightarrow x(t) \uparrow \text{if } G_E \neq 0 \rightarrow \text{update } \Gamma_E$$

The values of circuit parameters $\Gamma_E$ can be updated manually by a designer, or automatically. The solution is a vector of parameters $\Gamma_E$ that produces a PSS response $x(t)$, such that $G_E(x(t), \Gamma_E) = 0$. The DECs are satisfied, and a new circuit has the desired performance.

In this work, we focus on a well-posed design problem in (5), with equal number of parameters and constraints, and propose an elegant and efficient solution, the PSS-DEC analysis.

**C. PSS Analysis with Design Equality Constraints (PSS-DEC)**

The PSS-DEC analysis is formulated by combining the PSS equations in (3) and DECs in (5) together, while having $x(t)$, and $\Gamma_E$ as the unknowns of the new system of equations

$$\begin{cases} \frac{\text{d}q}{\text{d}t}(x(t), \Gamma_E) + f(x(t), \Gamma_E) + b(t, \Gamma_E) = 0 \\ x(0) - x(T_{in}) = 0 \\ \Gamma_E = 0 \end{cases}$$

The continuous-time description of the PSS-DEC analysis in (9) is a system of nonlinear DAEs that represent a periodic BVP. The solution of (9) simultaneously satisfies the original PSS equations in (3), and the design problem in (5).

Once the design goals are specified as equality constraints $G_E = 0$, and a suitable set of circuit parameters $\Gamma_E$ is defined, a single PSS-DEC analysis adjusts the values of the parameters, such that the design goals are met, while simultaneously finding the corresponding steady-state solution $x(t)$
used to eliminate $x_0$ from the list of unknowns. The remaining $nm + E$ equations represent a finite difference formulation of the proposed PSS-DEC analysis. Denoting the left hand side of (12) by $F_{fd}(x_1,\ldots,x_n,\Gamma_E)$, $F_{fd}: \mathbb{R}^m \times \ldots \times \mathbb{R}^m \times \mathbb{R}^E \rightarrow \mathbb{R}^{nm+E}$ we rewrite the equations as
\[
F_{fd}(x_1,\ldots,x_n,\Gamma_E) = 0
\]
The system of nonlinear equations in (14) can be solved using the Newton-Raphson iteration
\[
J_{fd}(X_{fd}^{(k)}) [X_{fd}^{(k+1)} - X_{fd}^{(k)}] = -F_{fd}(X_{fd}^{(k)})
\]
where $k$ is the iteration index, $X_{fd} = \begin{bmatrix} x_1^T & \ldots & x_n^T & \Gamma_E \end{bmatrix}^T$ is the vector of the finite difference unknowns,
\[
J_{fd}(x_1,\ldots,x_n,\Gamma_E) = \partial F_{fd}/\partial X_{fd}
\]
is the augmented finite difference Jacobian matrix, given by (13), $J_{fd}: \mathbb{R}^m \times \ldots \times \mathbb{R}^m \times \mathbb{R}^E \rightarrow \mathbb{R}^{(nm+E)\times(nm+E)}$. The Jacobian matrix is defined in terms of $C_i$ and $G_i$, the capacitance and conductance matrices
\[
C_i = \frac{\partial q_i}{\partial x_i}, \quad C_i: \mathbb{R}^m \times \mathbb{R}^E \rightarrow \mathbb{R}^{m \times m} \tag{17}
\]
\[
G_i = \frac{\partial f_i}{\partial x_i}, \quad G_i: \mathbb{R}^m \times \mathbb{R}^E \rightarrow \mathbb{R}^{m \times m} \tag{18}
\]
The top-left Jacobian block in (13) is the same as the Jacobian of the finite difference difference method for the conventional PSS analysis. The last columns of the Jacobian matrix $J_{fd}$ in (13) require derivatives of device contributions $\partial q/\partial \Gamma_E$, $\partial f/\partial \Gamma_E$, and $\partial b/\partial \Gamma_E$. These derivatives with respect to the tuning parameters can be obtained analytically or numerically from device models. The last rows of $J_{fd}$ require derivatives of DECs, $\partial G_i/\partial x_i$, $i = 1,\ldots,n$, and $\partial G_i/\partial \Gamma_E$. These derivatives can be obtained by differentiating the expressions for DECs with respect to individual waveform samples and tuning parameters.

The Newton-Raphson method has local convergence, and therefore, the initial guess must be close enough to the solution. The values of the tuning parameters, and the PSS solution of the original circuit is a reasonable initial guess for the PSS-DEC analysis.

There may be no solution to the design problem with DECs in (5), which means that the design specifications can not be satisfied by tuning the values of the selected parameters. Selection of a suitable set of parameters requires a good understanding of the design, and is delegated to a designer.

IV. EXAMPLES AND RESULTS

We have implemented the PSS-DEC analysis in our Matlab-based circuit simulator. In this section, a two-stage operational amplifier [6] in Figure 1 and a feedback circuit in Figure 2 are used to demonstrate the application of the PSS-DEC analysis.

![Two-stage operational amplifier](image1)

Fig. 1. Two-stage operational amplifier.

![Operational amplifier in a unity gain negative feedback](image2)

Fig. 2. Operational amplifier in a unity gain negative feedback.

Power consumption, slew rate, settling time, harmonic distortion, unity gain bandwidth, and phase margin are commonly used time-domain and frequency-domain opamp specifications. Next it will be shown how the design-oriented PSS-DEC analysis can handle these design specifications.

A. Harmonic Distortion

Amplifiers cause unwanted distortion of an input signal due to inherent nonlinearities. For example, given a sinusoidal input $x_{input}(t) = A_{in}\sin(2\pi f_\text{in}t)$, the output voltage contains harmonics $X_{out_2}, X_{out_3}, \ldots$ that have a real and an imaginary component. Harmonic distortion is a measure of the signal distortion, and depends on both the input amplitude $A_{in}$, and the frequency $f_\text{in}$.
harmonic distortion $HD_N$ is defined as the ratio of the magnitude of the $N^{th}$ harmonic to the magnitude of the $1^{st}$ harmonic (the fundamental) at the output $HD_N = |X_{out_N}| / |X_{out_1}|$.

Given an input frequency and amplitude, harmonic distortion can be found by a conventional PSS analysis that provides the output waveform $x_{out}(t)$ or its frequency spectrum. An example is shown below for the op amp in Figure 2.

$$f_{in} = 1.00 \text{ MHz} \quad A_{in} = 4.00 \text{ V} \quad \rightarrow \quad \text{PSS} \rightarrow \quad x(t) \quad \text{HD}_2 = 7.39\%$$

Alternatively, given a frequency $f_{in}$, a designer is often interested in finding the input amplitude $A_{in}$ for which the harmonic distortion reaches a certain specified level, e.g., $HD_2 = 1\%$. A single PSS-DEC analysis with one DEC and one parameter, $A_{in}$, can solve this problem efficiently. An appropriate amplitude $A_{in}$ is found directly as depicted below.

$$f_{in} = 1.00 \text{ MHz} \quad \rightarrow \quad \text{PSS} \longrightarrow \quad g_1 = 0 \quad \gamma_1: A_{in} = 3.28 \text{ V}$$

$$g_1(x) = |X_{out_2}| / |X_{out_1}| - 1\%$$

The PSS-DEC solution $x(t)$ satisfies the DEC equation,

$$|X_{out_2}| / |X_{out_1}| = 1\%,$$

which ensures that $HD_2$ is exactly 1%. As expected, at a given frequency, a smaller input signal exhibits less distortion.

The DEC $g_1$ is written in terms of the output voltage $x_{out}(t)$. The derivatives $\partial g_1 / \partial x_i$ must appear in the last row of the Jacobian matrix $J_{sol}$ in (13). The derivatives of the excitation $\partial h_i / \partial \gamma_j$ must appear in the last column of $J_{sol}$.

The PSS-DEC analysis with constraints on harmonic distortion has applications in analog filter design. The signal-to-noise ratio (SNR) of analog filters is normally defined for the input level that results in a specified harmonic distortion. This input level can be found efficiently by the PSS-DEC analysis as illustrated in the above example.

### B. Settling Time and Slew Rate

A voltage step $x_{in}(t)$ in Figure 3(a) produces a response $x_{out}$ in Figure 3(b) that is a distorted version of the inverted input signal. As seen from Figure 3(b), during a transition from high to low, the output voltage changes at a constant rate, called the slew rate (SR). The slew rate is determined by the speed with which the drain current of $M_3$ charges the compensation capacitor $C_c$ (Figure 1). The output transition from low to high is shaped by the time constant at the output node. As shown in Figure 3(b), the time that it takes for the output to reach the ideal level of 3 V within an error band of, e.g., ±5%, is called the settling time $T_s$. In this example, the output voltage does not overshoot the 3.15 V level, and therefore, the settling time is defined by the time of the 2.85 V level crossing

$$T_s = t_s - 450 \text{ ns}, \quad t_s : \quad x_{out}(t_s) = 2.85 \text{ V} \quad (19)$$

The values of the slew rate and settling time of the step response in Figure 3(b) can be found from a conventional PSS analysis

$$C_I = 5.00 \text{ pF} \quad \rightarrow \quad \text{PSS} \rightarrow \quad \gamma_1: C_c = 2.89 \text{ pF}$$

$$I_1 = 156.47 \mu\text{A} \quad \rightarrow \quad \gamma_2: I_1 = 191.55 \mu\text{A}$$

Let the design goal be to drive a 5 pF load while having a 150 ns settling time with an increased slew rate of $-80 \text{ V/\mu s}$. This can be achieved by tuning the current $I_1$ and the compensation capacitor $C_c$. The values of $I_1$ and $C_c$ are found from the PSS-DEC analysis with two DECs and two parameters.

$$C_I = 5.00 \text{ pF} \quad \rightarrow \quad \text{PSS} \rightarrow \quad \gamma_1: C_c = 2.89 \text{ pF}$$

$$I_1 = 156.47 \mu\text{A} \quad \rightarrow \quad \gamma_2: I_1 = 191.55 \mu\text{A}$$

The goal is achieved by requiring the output of 2.85 V at 600 ns, that is 150 ns after the transition from low to high starts, and requiring the output voltage slope of $-80 \text{ V/\mu s}$ during the transition from high to low, at 100 ns.

The step response with the circuit parameters obtained from the PSS-DEC analysis is shown in Figure 4. It can be seen that the design goal is met.

![Fig. 4. Step response of the original design and the design obtained from the PSS-DEC analysis.](image-url)
A small-signal frequency-domain description of an op amp is the gain $A(f) = X_{out}(f)/X_{in}(f)$. One important small-signal characteristic of an op amp is the frequency band $f \in [0, f_u]$ where the gain magnitude is at least one. This band is limited by the unity gain characteristic of an op amp is the frequency band that cannot be handled by a traditional small-signal AC analysis. However, small-signal characteristics can be verified by a conventional large-signal PSS analysis as well, given a sufficiently small input amplitude, such that the output harmonics are negligible. This allows us to set up the PSS-DEC analysis with DECs for the phase compensation capacitor $C_c$ between the input and output signals $X_{in}(f)$ and $X_{out}(f)$. The lower limit for $f_u$ can be verified by a conventional large-signal AC analysis. In practice, due to parameter variations, the value of the on-chip compensation capacitor $C_c$ is not exactly the same as the nominal value of $2.84 \, \text{pF}$. Consequently, the phase margin and the unity gain frequency deviate from the ideal values. Let the design specifications allow the PM and $f_u$ to vary from their ideal values by at most $\pm 5^\circ$ and $\pm 10 \, \text{MHz}$, respectively. It is useful to know the bounds for acceptable capacitor variations, and what design specification is violated first as $C_c$ variation increases.

This problem can be solved by several PSS-DEC analyses. The $C_c$ value that results in $f_u = 30 \, \text{MHz}$ is found from a PSS-DEC analysis with one DEC and one parameter. 

The design equality constraint used in this example, $|X_{out}| = |X_{in}|$, ensures that the output and input magnitudes are equal, and therefore, the gain is unity. The value of $3.99 \, \text{pF}$ obtained from the PSS-DEC analysis corresponds to the upper limit of the compensation capacitor, for the unity gain frequency to stay in the specified bounds. The PSS-DEC analysis finds the lower limit $C_c = 2.12 \, \text{pF}$ that corresponds to $f_u = 50 \, \text{MHz}$ in a similar fashion. It can be seen from the above results, as well as from Figure 5, that the phase margin specification is violated first as $C_c$ variation increases.

A tighter region of capacitor variations that simultaneously results in acceptable $f_u$ and PM is found based on two PSS-DEC analyses, one for PM = 55$^\circ$ and one for PM = 65$^\circ$. The upper limit for $C_c$ is found from a PSS-DEC analysis with two DECs and two parameters.

### TABLE I

<table>
<thead>
<tr>
<th>Units</th>
<th>PSS</th>
<th>PSS-DEC</th>
<th>PSS-DEC</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_a$ [\text{ns}]</td>
<td>229.57</td>
<td>150.00</td>
<td>150.00</td>
</tr>
<tr>
<td>SR [\text{V/\mu s}]</td>
<td>-68.33</td>
<td>-68.19</td>
<td>-80.00</td>
</tr>
<tr>
<td>$C_1$ [\text{pF}]</td>
<td>5.00</td>
<td>2.02 ($\gamma_1$)</td>
<td>5.00</td>
</tr>
<tr>
<td>$C_c$ [\text{pF}]</td>
<td>2.84</td>
<td>2.84</td>
<td>2.89 ($\gamma_1$)</td>
</tr>
<tr>
<td>$I_1$ [\text{\mu A}]</td>
<td>156.47</td>
<td>157.47</td>
<td>191.55 ($\gamma_2$)</td>
</tr>
</tbody>
</table>

### C. Unity Gain Frequency and Phase Margin

The frequency response $A(f)$ is traditionally computed by a fast small-signal AC sweep, rather than by a large-signal PSS analysis. However, small-signal characteristics can be verified by a conventional large-signal PSS analysis as well, given a sufficiently small input amplitude, such that the output harmonics are negligible. This allows us to set up the PSS-DEC analysis with DECs for the phase margin and the unity gain frequency, and solve certain problems that can not be handled by a traditional small-signal AC analysis.

The op amp in Figure 1 is designed with the use of a compensation capacitor $C_c$ for a typical PM of 60$^\circ$, and a unity gain frequency of 40 MHz. The PM and $f_u$ can be verified by a conventional large-signal PSS analysis. $f_{in} = 40.00 \, \text{MHz}$ $A_{in} = 1.00 \, \text{mV}$ $C_c = 2.84 \, \text{pF}$ 

$|A(f_{in})| = 1.00 \rightarrow f_u = 40.00 \, \text{MHz}$ 

The frequency response $A(f)$ is traditionally computed by a fast small-signal AC sweep, rather than by a large-signal PSS analysis. However, small-signal characteristics can be verified by a conventional large-signal PSS analysis as well, given a sufficiently small input amplitude, such that the output harmonics are negligible. This allows us to set up the PSS-DEC analysis with DECs for the phase margin and the unity gain frequency, and solve certain problems that can not be handled by a traditional small-signal AC analysis.

The lower limit for $C_c$ is found in a similar manner. Figure 5 shows that if $C_c \in [2.30 \, \text{pF}, 3.56 \, \text{pF}]$, then PM $\in [55^\circ, 65^\circ]$, and the unity gain frequency is within the acceptable range as well. 

Note that in the previous PSS-DEC setup, the second parameter $\gamma_2$ is the input frequency $f_{in}$, and the steady-state period is not known beforehand. This example shows the flexibility of the PSS-DEC analysis, and its ability to simulate forced circuits in a similar manner to oscillators where the period of oscillation is one of the PSS unknowns.

### D. Power Consumption and Other Design Constraints

Next, consider an op amp at an intermediate stage of a design process. A response for values of circuit parameters at this design stage is computed by a conventional PSS analysis.

$\gamma_1$: $C_c = 3.56 \, \text{pF}$ $\gamma_2$: $f_{in} = 33.08 \, \text{MHz}$ $g_1(x) = X_{out} - X_{in}$ $g_2(x) = \Delta X_{in} - \Delta X_{out} - 115^\circ$ 

The lower limit for $C_c$ is found in a similar manner. Figure 5 shows that if $C_c \in [2.30 \, \text{pF}, 3.56 \, \text{pF}]$, then PM $\in [55^\circ, 65^\circ]$, and the unity gain frequency is within the acceptable range as well.
In this example, the power consumption $P_c$ is computed as
\[ P_c = -\left[ V_d \cdot DC(x_{V_d}) + V_s \cdot DC(x_{V_s}) \right] \] (21)
where $DC(\cdot)$ denotes the DC or average value, $V_d, V_s$ are the values of the power supply voltage sources, and $x_{V_d}, x_{V_s}$ are the currents through these voltage sources.

Let the design goal be to achieve a $60^\circ$ phase margin at 40 MHz unity gain frequency, as well as to reduce the power consumption by 20% to 8 mW by tuning the design parameters. Other design considerations must be taken into account, such as keeping the input pair devices same $W_1 = W_2$, preserving the width ratio $W_6 = kW_3 = kW_4$, $k = 17/5$, as well as adjusting the zero cancellation resistor according to $R_s = 1/g_m$ if the size of $M_6$ changes.

This problem can be solved by a PSS-DEC analysis with four DECs and four parameters.

\[ f_i = 40.00 \text{ MHz} \]
\[ A_i = 1.00 \text{ mV} \]
\[ g_1 = 0 \]
\[ g_2 = 0 \]
\[ g_3 = 0 \]
\[ g_4 = 0 \]

\[ f_u = 40.00 \text{ MHz} \]
\[ P_c = 8.00 \text{ mW} \]
\[ \gamma_1: \ R_s = 361.02 \Omega \]
\[ \gamma_2: \ W_1 = 74.73 \mu m = W_2 \]
\[ \gamma_3: \ W_6 = 56.77 \mu m = kW_3,4 \]
\[ \gamma_4: \ I_1 = 156.48 \mu A \]

The circuit parameters and performance measurements of the original design, and the design obtained by the PSS-DEC analysis are shown in Table II. The gain magnitude and phase responses for the two designs are shown in Figure 6.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>PSS</th>
<th>PSS-DEC</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_u$ [MHz]</td>
<td>38.90</td>
<td>40.00</td>
</tr>
<tr>
<td>PM [deg]</td>
<td>52.07</td>
<td>60.00</td>
</tr>
<tr>
<td>$P_c$ [mW]</td>
<td>10.11</td>
<td>8.00</td>
</tr>
<tr>
<td>$R_s$ [\Omega]</td>
<td>591.22</td>
<td>361.02 (\gamma_1)</td>
</tr>
<tr>
<td>$W_1 = W_2$ [\mu m]</td>
<td>75.00</td>
<td>74.73 (\gamma_2)</td>
</tr>
<tr>
<td>$W_6 = kW_3 = kW_4$ [\mu m]</td>
<td>17.00</td>
<td>57.66 (\gamma_3)</td>
</tr>
<tr>
<td>$I_1$ [\mu A]</td>
<td>200.00</td>
<td>156.48 (\gamma_4)</td>
</tr>
</tbody>
</table>

Describing $W_6$, $W_3$, and $W_4$ by only one parameter $\gamma_3$ results in a more compact PSS-DEC problem, without including the relationships $W_6 = kW_3$ and $W_6 = kW_4$ as DECs. Note that the entries of the corresponding column of the Jacobian matrix $J_{f,d}$ in (13) must be computed as, e.g.,
\[ \frac{\partial q}{\partial \gamma_3} = \frac{\partial q}{\partial W_6} + k \frac{\partial q}{\partial W_3} + k \frac{\partial q}{\partial W_4} \] (22)

The relation for the input pair devices $W_1 = W_2$ is treated in a similar fashion.

![Figure 6](image-url)

(a) Magnitude, and (b) phase of the small-signal gain of the original design and the design obtained from the PSS-DEC analysis.

Note that the DEC $g_4(x, \gamma_1, \gamma_3)$ is written not only in terms of $x(t)$ but also in terms of $\gamma_1$ and $\gamma_3$. Partial derivatives $\partial g_4/\partial \gamma_1$, and $\partial g_4/\partial \gamma_3$ must appear in the bottom-right block of $J_{f,d}$.

**V. Conclusion**

We have presented a theoretical formulation and numerical methods for a design-oriented periodic steady-state analysis that includes design equality constraints (PSS-DEC analysis). This analysis efficiently finds the values of circuit parameters that result in a desired circuit performance, defined by equality constraints. In contrast to a conventional design approach, there is no need for performing a sequence of conventional PSS analyses. Examples demonstrate usage scenarios for the PSS-DEC analysis in op amp design but the technique is applicable to a wide range of circuits.

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