Efficient Unknown Blocking Using LFSR Reseeding

Seongmoon Wang  Kedarnath J. Balakrishnan  Srimat T. Chakradhar
NEC Laboratories America, 4 Independence Way, Princeton, NJ 08540, USA
Email: {swang,bala,chak}@nec-labs.com

Abstract

This paper presents an efficient method to block unknown values from entering temporal compactors. The control signals for the blocking logic are generated by an LFSR. The proposed technique minimizes the size of the LFSR by propagating only one fault effect for each fault and balancing the number of specified bits in each control pattern. The linear solver to find seeds of the LFSR intelligently chooses a solution such that the impact on test quality is minimal. Experimental results show that sizes of control data for the proposed method are smaller than prior work and run time of the proposed method is several orders of magnitude smaller than that of prior work. Hardware overhead is very low.

1 Introduction

Reducing test data volume of complex designs has become an important part of current test methodologies. Higher test data volume leads to higher test costs as well as longer test application time. Several techniques including commercial tools [4, 2] to compress both input test patterns and output responses have been developed. Techniques to reduce output response can be classified into two basic categories: spatial and temporal compaction. Spatial compaction reduces response data volume by reducing the number of outputs that are observed by the automatic test equipment (ATE).

The presence of unknown values (unknowns for short) in output responses of scan test patterns creates a lot of complications for test data compression. In spatial compaction, if a fault effect appears at the output of a scan chain along with an unknown (X) at a given scan shift cycle, the fault effect is masked and cannot be observed at the output of the compactor during that cycle. Temporal compaction compresses output responses over a period of time into a signature, which is significantly smaller than the size of even a single output response. A multiple input signature register (MISR) is the simplest and the most popular example of a temporal compactor. Since entrance of any unknown into a temporal compactor corrupts the signature for output responses over the entire period of testing time, unknowns at outputs are catastrophic in temporal compaction.

The solution to this problem is to either design compactors that can tolerate unknowns or devise techniques to mask or block unknowns from entering the compactor. Blocking unknowns requires control data that also contribute to overall test data volume. Previously proposed schemes for blocking unknowns include the selective compactor [4], channel masking [1] and XML [6] for Logic BIST. The first two techniques suffer from limited observability since either only one scan chain output can be observed at a time (as in [4]) or all scan chains are together either blocked or observed at any scan shift cycle (as in [1]). Enhancements of both these techniques have been proposed to improve observability but at the expense of higher area overhead and/or larger control data [5]. In [6], a combinational logic block called X-Masking Logic (XML) to generate the blocking signals is designed for specific BIST patterns. To minimize hardware overhead of the XML, the algorithm uses fault isolation tables which requires huge memory space and makes this impractical for large industrial designs.

In this paper, we present a very efficient method that can be used to minimize control data volume required to block unknowns in temporal compaction. It is based on LFSR reseeding, a technique that has been used extensively for test stimuli compression.

2. LFSR Reseeding Based Unknown Blocking

Figure 1 illustrates the basic LFSR reseeding based unknown blocking scheme. Unknowns and fault effects are blocked or propagated by control signals that are driven by the LFSR. In order to propagate an error (fault effect) to the MISR input, the control input of the corresponding blocking logic gate should be set to a 0, assuming that the blocking logic gate is an OR gate (see the fault effect $D$ at the output of the scan chain 2 in Figure 1). On the other hand, if an unknown appears at the output of a scan chain, then the unknown should be blocked by setting the control input of the corresponding blocking logic gate to a 1 (see the two unknowns that are scanned out at the outputs of scan chain 1 and scan chain 4). All the other control inputs need not be specified. Control signals for the blocking logic gates are generated by the LFSR by loading appropriate seeds from the ATE memory into the LFSR.

Naruse et al. [3] proposed an unknown blocking scheme for Logic BIST based on the above. However, in order to reduce the number of seeds that are stored in an on-chip memory, a best feedback polynomial of LFSR is searched from a set of different degrees of polynomials. The critical drawback of this method is prohibitive run time. The logic circuit for mapping the content of fragment counter to a memory address and the test pattern count decoder that is required
to block some responses from entering the MISR should be customized to a specific set of test responses. Hence, if test patterns and responses are regenerated due to last minute design change, the whole blocking hardware should also be redesigned.

In LFSR reseeding, the number of specified bits in the most specified test pattern, which is often denoted by $S_{\text{max}}$, determines the size of seeds or the number of stages of LFSR. Hence it is important to minimize the number of specified bits in the control pattern that has the most specified bits to reduce overall control data volume. Every unknown that is scanned out of any scan chain output should be blocked to prevent corrupting the signature. However, typically, the number of unknowns observed is much less than the number of fault effects captured by the scan chains. Hence, the number of control bits to be specified will be determined by the number of fault effects (errors) that are selected to propagate to the MISR.

In the proposed scheme, a two fold method is applied to minimize $S_{\text{max}}$. First, we reduce the number of specified bits by propagating only one fault effect per fault. Computed control patterns are processed by a linear solver to compute LFSR seeds that expand to desired control patterns. The proposed linear solver minimizes possible degradation on quality of testing due to single fault effect propagation by intelligently assigning free variables in equations to compute seeds for control patterns. Second, the number of specified bits in each control pattern is balanced by a technique based on reverse order fault simulation. The proposed method can achieve the same fault coverage that can be achieved by direct scan chain observation (without using any output compaction) without modification of existing test patterns or addition of new test patterns to compensate faults that are not detected due to use of output compaction.

3. Experimental Results

Table 1 shows a comparison of proposed scheme with previous work [3] for test responses with 0.2% unknowns. Fault coverage is reported in columns $FC\%$. Storage bits (column $\text{stor. (bits)}$) for control patterns of the proposed scheme are smaller than [3] for most circuits except s15850. Especially, storage for s13207 of the proposed scheme is only about 1/3rd of that of [3]. Run time of the proposed method is several orders of magnitude shorter than that of [3] for all circuits. Hardware overhead is shown in gate equivalents in columns $GE$. Since the proposed method needs only an LFSR to control the blocking logic, hardware overhead for the proposed method is significantly lower. Another advantage of the proposed method is that the hardware is pattern and design independent. The proposed blocking circuitry can be designed once the scan architecture of design is fixed without detailed knowledge on the design. Some design changes may necessitate adding a few flip-flops to the LFSR. However, adding a few flip-flops is trivial compared to redesigning a large decoder such as XML [6] or address mapping logic [3].

4. Conclusions

This paper presents an efficient method to block unknowns for temporal compactors. In the proposed method, blocking logic gates, which selectively block unknowns and propagate fault effects to the temporal compactor, are controlled by an LFSR. Control patterns for the blocking logic that are generated by the LFSR are compressed by LFSR reseeding. The proposed method can achieve the same fault coverage that can be achieved by direct scan chain observation (without using any output compaction) without modification of existing test patterns or addition of new test patterns to compensate faults that are not detected due to use of output compaction.

References