Opportunities for Cross-Layer Design in High-Performance Computing Systems with Integrated Silicon Photonic Networks

Asif Mirza, Shadi Manafi Avari, Ebadollah Taheri, Sudeep Pasricha, and Mahdi Nikdast
Department of Electrical and Computing Engineering
Colorado State University, Fort Collins, Colorado, USA
E-mail: {asifmirza, shadim, taheri, sudeep, mnikdast}@colostate.edu

***Abstract*—With the ever growing complexity of high-performance computing (HPC) systems to satisfy emerging application requirements (*e.g.*, high memory bandwidth requirement for machine learning applications), the performance bottleneck in such systems has moved from being computation-centric to be more communication-centric. Silicon photonic interconnection networks have been proposed to address the aggressive communication requirements in HPC systems, to realize higher bandwidth, lower latency, and better energy efficiency. There have been many successful efforts on developing silicon photonic devices, integrated circuits, and architectures for HPC systems. Moreover, many efforts have been made to address and mitigate the impact of different challenges (*e.g.*, fabrication process and thermal variations) in silicon photonic interconnects. However, most of these efforts have focused only on a single design layer in the system design space (*e.g.*, device, circuit or architecture level). Therefore, there is often a gap between what a design technique can improve in one layer, and what it might impair in another one. In this paper, we discuss the promise of cross-layer design methodologies for HPC systems integrating silicon photonic interconnects. In particular, we discuss how such cross-layer design solutions based on cooperatively designing and exchanging design objectives among different system design layers can help achieve the best possible performance when integrating silicon photonics into HPC systems.**

***Index Terms*—High-performance computing, silicon photonics, cross-layer design.**

I. Introduction

The emergence of novel applications (*e.g.*, machine learning) with high computation and communication requirements and the continuous advances in CMOS integration density have driven the trend for integrating many processing nodes in today's high-performance computing (HPC) systems. State-of-the-art HPC systems have multiple manycore general-purpose processor chips with tens of cores (*e.g.*, AMD EPYC processor family with up to 64 cores [1] and Intel's Xeon Platinum processor family with up to 56 cores [2]), connected by a network-on-chip (NoC) architecture and with up to 8 sockets of these chips interconnected together. Emerging graphics processing units (GPUs) and neuromorphic accelerator chips with hundreds to thousands of cores are now further pushing the boundaries of on-chip and off-chip communication architecture design. For instance, NVIDIA's GPU chips with the Turing architecture have more than 4000 CUDA cores [3] and AMD's Navi/RDNA GPU architecture supports more than 2500 cores [4]. As another example, Cerebras recently unveiled an artificial intelligence (AI) accelerator processor chip with 1.2 trillion transistors and 400,000 (lightweight) cores [5]. While such a chip may not be representative of commercially-viable mainstream processors, it points to a future where hundreds to thousands of CPU, GPU, and AI cores will need to be connected together with high bandwidth and low power interconnect solutions.

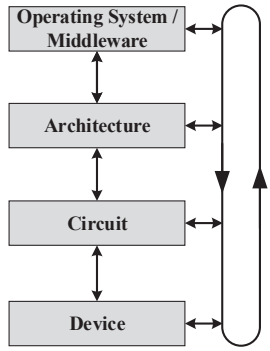

Fig. 1. An abstract overview of different design layers and a cross-layer design approach concept in HPC systems integrating silicon photonic interconnects.

The fundamental communication infrastructure in today's HPC systems relies on electrical interconnect technology for intra-chip and inter-chip communication. However, such conventional interconnects will fail to deliver the performance requirements of future complex HPC systems: electrical interconnects cannot provide bandwidth, latency, and energy requirements for emerging applications, especially as HPC systems scale [6]. Indeed, the overall system performance in HPC systems is determined not only by the computation power of each individual node, but most importantly by how

This research was supported by the National Science Foundation (NSF) under grant number CCF-1813370.

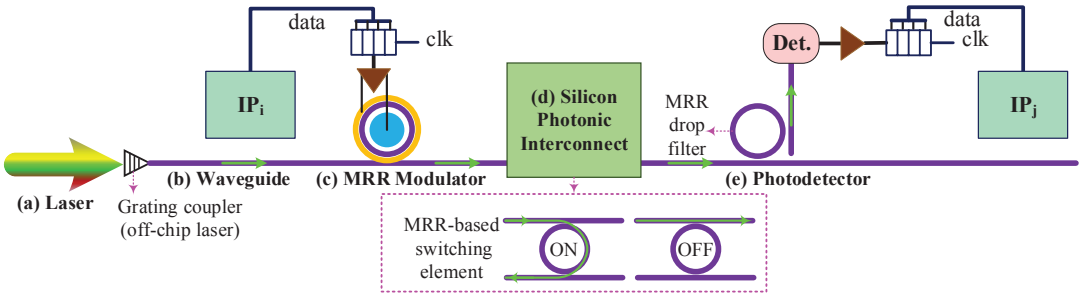

Fig. 2. An abstract overview of a silicon photonic interconnect between two intellectual property (IP) cores (IP_i and IP_j) in a HPC system. As an example, we consider using microring resonators (MRRs) for modulation, switching, and filtering.

efficiently such nodes can communicate with one another. Silicon photonic interconnects have been proposed to address such high-performance communication requirements in future complex HPC systems and to overcome the metallic interconnect bottleneck [7].

Several intra-chip and inter-chip communication networks have been proposed for HPC systems based on silicon photonics [6]. In general, such architectures include a laser source (often off-chip), modulators, optical waveguides, photonic switching elements, optical multiplexers and demultiplexers, optical filters, and photodetectors. There have been many successful demonstrations of these fundamental devices to pave the way for their integration into HPC systems. All of such devices, however, are susceptible to inevitable variations in fabrication process and runtime temperature fluctuations. In particular, any variation in the critical dimensions (*e.g.*, waveguide thickness or width) of a silicon photonic waveguide can considerably impact the device performance [8], [9], often in terms of imposing higher losses and crosstalk noise, both of which impact the energy efficiency of silicon photonic devices. Such device inefficiencies can accumulate in a system, considerably degrading the system performance. For example, it was shown that fabrication process variations can decrease the optical signal-to-noise ratio (OSNR) in silicon photonic interconnects by up to 20 dB [8]. Similar to the impact of fabrication process variations, temperature variations can significantly degrade the performance of silicon photonic interconnects because of the high thermo-optic effect in silicon. For example, [10] indicated a considerable increase in system power loss in silicon photonic interconnects due to runtime temperature variations.

There have been many efforts to mitigate the impact of inevitable fabrication and thermal variations in silicon photonic interconnects. While the silicon photonic interconnect design space is multi-layer (*i.e.*, device, circuit, architecture, and operating system, see Fig. 1), such efforts very often focus only on a single design layer in silicon photonic interconnects. Consequently, there is a gap between what a design solution can improve in one design layer, and what it might impair in another one. On the other hand, cross-layer design solutions involve enhancements at one or more of the device, circuit, architecture, and system (operating system and/or middleware) layers in a cooperative manner. Such techniques have the potential to be significantly more effective than single-layer techniques in achieving holistic design goals such as energy efficiency and higher reliability under different variations.

In this paper, we review some of the recent efforts in implementing cross-layer design solutions in HPC systems integrating silicon photonic interconnects to mitigate the impact of fabrication and thermal variations in the system. In particular, we discuss the main requirements to enable such cross-layer design solutions, and provide examples from our prior work on cross-layer optimization techniques to minimize crosstalk and improve system performance and reliability under runtime thermal variations.

The rest of the paper is organized as follows. Section II reviews some of the fundamental challenges in silicon photonic devices that impact the system performance in HPC systems integrating silicon photonic interconnects as well as some single-layer design solutions to address such challenges. We present some of our recent efforts on enabling cross-layer optimization techniques in HPC systems integrating silicon photonics in Section III. Finally, we discuss our conclusions in Section IV.

II. Silicon Photonic Challenges and Single-Layer Design Solutions

We start by an overview of a silicon photonic interconnect in a HPC system. Fig. 2 shows an abstract overview of a silicon photonic interconnect between two intellectual property (IP) cores (IP_i and IP_j) in a HPC system. As can be seen, an optical signal, which is often generated by an off-chip laser, couples to the waveguide through a grating coupler (see Figs. 2a and 2b). The optical signal is then modulated based on electronic data from the source IP core (IP_i) and through silicon photonic modulators (*e.g.*, microring resonator modulator (MRR) in Fig. 2c). The modulated signal travels through a silicon photonic interconnect network that often includes many switching elements to route signals between different source and destination IPs (*e.g.*, MRR-based switching element in

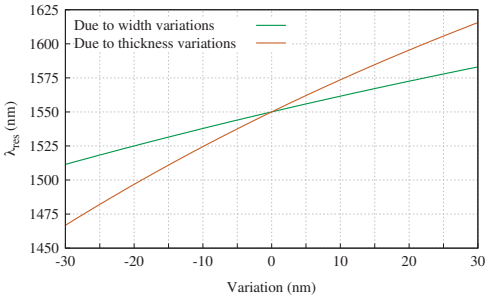

Fig. 3. Resonant wavelength (λ_{res}) shift in a microring resonator as a result of variations in the waveguide width and thickness (x-axis). As can be seen, the resonant wavelength shifts with any variations in the critical dimensions (width and thickness) of the microring resonator.

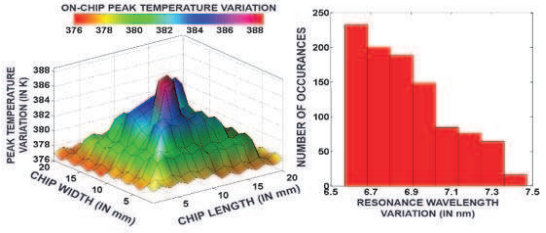

Fig. 4. (a) Spatial variation in peak temperatures; and, (b) Histogram of peak thermal variation-induced resonant wavelength variation across a chip of size 400 mm^2 using 3D ICE tool while executing 64 threaded PARSEC and SPLASH2 benchmark applications on a 64-core system [15].

Fig. 2d). At the receiver, the desired optical signal is dropped into a photodetector and eventually converted to electronic data, which is received by the destination IP core (IP$_j$, see Fig. 2e). In silicon photonics, we can transfer multiple optical wavelengths simultaneously through a single waveguide. The number of wavelengths used per waveguide is often referred to as the degree of wavelength division multiplexing (WDM), with each wavelength enabling the transfer of a stream of bits (in parallel with other wavelengths) to support high bandwidth transfers.

There is attenuation and performance degradation throughout all the steps discussed in Fig. 2. This section reviews some of the fundamental challenges at the silicon photonic device level in terms of vulnerability to fabrication and thermal variations and aging effects, all of which impact performance and energy efficiency of HPC systems integrating silicon photonic interconnects. Moreover, we review some of the common single-layer design solutions (*e.g.*, device-layer) to mitigate the impact of such effects in HPC systems integrating silicon photonic interconnects. Note that there are other challenges and single-layer (*e.g.*, those at the circuit-layer) design solutions in HPC systems integrating silicon photonics. We focus on a few examples at the device-layer in this paper.

A. Silicon Photonic Device Challenges

To realize reliable silicon photonic interconnects, it is critical to align the central optical wavelengths of different components in such networks, particularly when employing many optical wavelengths (*i.e.*, optical channels) for dense wavelength division multiplexing (DWDM). However, the fundamental building blocks in silicon photonic interconnects are considerably sensitive to fabrication process variations. Fabrication process variations mostly originate in the fabrication process (*e.g.*, lithography effects, chemical polishing), contributing to different variations in the waveguide thickness, linewidth, dopant, *etc*. [11]. Such variations deviate central wavelengths among different components in silicon photonic interconnects, leading to performance degradation, or in the worst-case, system failure. For instance, a single nanometer change (due to fabrication variations) in the critical dimensions of a microring resonator, a fundamental building block in silicon photonic interconnects [12], can shift the central optical wavelength (*i.e.*, MRR resonant wavelength) of the device by ≈2 nm [8] (see Fig. 3). Such deviations in DWDM networks, with a typical channel spacing of 0.2 to 1 nm, are absolutely unacceptable, imposing high OSNR degradation and increasing the bit-error-rate (BER) in the network [13].

In addition to fabrication process variations, silicon photonic devices are sensitive to runtime temperature fluctuations. Such thermal instability is due to the high thermo-optic effect of silicon. In particular, this is of concern when such devices are integrated and packaged with electronic devices in HPC systems, where chip-scale temperature variations can reach up to 30 degrees [13]. Silicon refractive index is temperature dependent (due to the thermo-optic effect) and follows

$$n = n_0 + \frac{dn}{dt}\Delta T, \tag{1}$$

where n_0 is the silicon refractive index at room temperature, $\frac{dn}{dt}$ is the thermo-optic coefficient of silicon that is in the range of 1.8×10^{-4} K^{-1} [14], and ΔT is the chip temperature variation. As a result, similar to the impact of fabrication process variations, temperature variations can considerably degrade the performance of silicon photonic interconnects because of the high thermo-optic effect in silicon. For example, in addition to fabrication process variations, the resonant wavelength of an MRR is also sensitive to thermal variations with up to a 7.4 nm shift in the resonance on a state-of-the-art 64-core processor chip (see Fig. 3) [15]. Such a resonance shift causes wavelength coupling failures, prompting the need for dynamic MRR tuning.

Devices such as MRRs often use current injection tuning to switch between resonance modes and also to compensate for resonance drifts. Current injection tuning involves applying a positive or negative voltage bias to an MRR's PN-junction (between the core and cladding) to inject or remove free carriers into or from the MRR core. For high frequency operation and lower power consumption, an MRR's PN-junction is typically operated under a negative voltage bias or

reverse bias [16] (otherwise known as carrier depletion mode of an MRR). The application of this voltage bias generates an electric field across the MRR's core and cladding boundary. Similar to MOSFETs, this electric field generates voltage bias temperature induced (VBTI) traps at the core/cladding (silicon/silicon dioxide) boundary of the MRR over time (*i.e.*, VBTI aging). In [17], we demonstrated for the first time how these VBTI aging induced traps alter carrier concentration in the silicon core of MRRs, which incur resonance wavelength drifts and increase optical scattering loss in MRRs to degrade their quality (Q) factors.

B. Single-Layer Design Solutions

Due to the fabrication and thermal variations discussed in the previous section, devices such as MRRs are susceptible to resonance wavelength shifts (see Figs. 3 and 4), which prevent accurate modulation, switching, and filtering for detection. Such deviations impose performance degradations in silicon photonic interconnects especially when using multiple wavelengths in such interconnects. The proposed single-layer solutions to address variation-induced shifts fall into two main categories: permanent post-fabrication trimming and runtime tuning mainly through the thermo-optic effect (*i.e.*, thermal tuning) or electro-optic effect (*i.e.*, bias or current injection tuning).

The main post-fabrication trimming solutions are based on either changing the level of compaction or stress of the cladding or core material (*e.g.*, using high-energy electron or laser beams), or changing the refractive index of the cladding material by applying high-energy UV light. Thermal tuning is achieved by varying current through a heater near the MRR, introducing an increase in the refractive index of the silicon and the resonant wavelength to achieve a red shift. The current injection tuning method injects (or depletes) free carriers into (or from) the silicon core of an MRR using an electrical tuning circuit, which reduces (or increases) the MRR's refractive index owing to the electro-optic effect, to compensate for the variation-induced red (or blue) shift in the MRR's resonance wavelength.

Current injection tuning can provide a tuning range of only 1.5 nm at most [18], but it incurs relatively low latency and power overheads (an addition of up to 130 μW/nm shift per MRR to the total link power [19]). In contrast, thermal tuning incurs high latency and power overheads: an addition of 550 mW/nm shift per MRR to the total link power [20], and in speed, with devices displaying very high $\approx$100 μm thermal time constants [21]. However, it can provide a larger tuning range of about 6.6 nm [15] and induces lower power loss than current injection tuning. It is possible to only rely on one of these methods in a design, but intelligently utilizing both can enable better energy efficiency. As for the aging effects, it was shown in [22] that the use of pulse-amplitude modulation (PAM)-4 signaling can reduce the impact of aging while also improving energy-efficiency by 5.5% compared to using conventional on-off keying (OOK) signaling, in the presence of aging-induced long term variations.

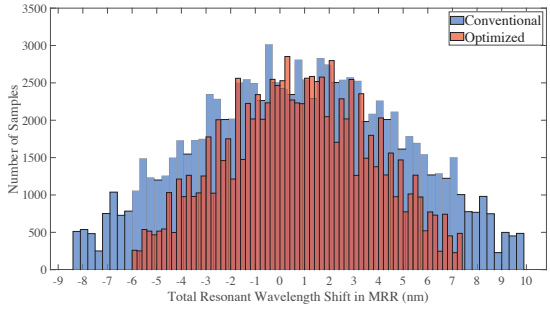

Fig. 5. Total resonant wavelength shift in a microring resonator (MRR) as a result of random variations in the waveguide width and thickness as well as those in the MRR's radius. Compared to the conventional MRR design, the optimized MRR design has a higher tolerance to different fabrication process variations (*i.e.*, the total resonant wavelength shift is smaller) [24].

There have been some efforts at the device layer to improve thermal stability of silicon photonic devices and their tolerance to fabrication process variations. To improve thermal stability, several methods have been proposed based on passive temperature stabilization using athermal solutions (*e.g.*, based on polymers and titanium dioxide) for silicon photonic devices [23]. For example, by using organically modified sol-gel claddings, [23] demonstrated a thermal shift down to -6.8 pm/$^\circ$C for transverse electric (TE) polarization in MRRs with waveguide widths of 325 nm. To improve MRR tolerance to different fabrication process variations, we presented a comprehensive design space exploration of the physical parameters of MRRs under fabrication process variations [24]. In particular, we developed analytical models required to study the resonant wavelength shift, cross-over coupling, and quality factor in MRRs under fabrication process variations. Leveraging these comprehensive models, a design optimization solution was developed to find optimal physical design parameters in MRRs, enhancing their tolerance to fabrication process variations while improving insertion loss (through coupling) and Q-factor in such devices. Fig. 5 compares the total resonant wavelength shift in an MRR because of random variations in the waveguide width, waveguide thickness, and MRR's radius. As can be seen, our design optimization can effectively reduce the total resonant wavelength shift in an MRR under different random variations.

III. Cross-Layer Design Solutions

As discussed in Section II, single-layer design solutions are effective, but often can only impact the single design layer they are targeting in HPC systems integrating silicon photonic interconnects. In addition, some of these solutions may improve the performance of a particular design layer, but impose performance degradation on other design layers. For example, thermal tuning can improve the device-layer performance through correcting devices whose central optical frequencies have been shifted, but at a cost of high power consumption at the circuit-layer and also high latencies at

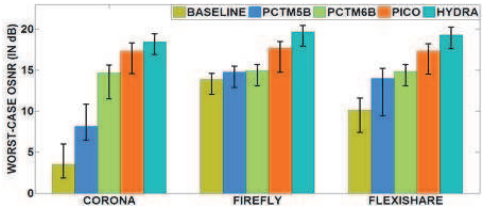

Fig. 6. The worst-case OSNR comparison of cross-layer HYDRA framework with single-layer solutions PCTM5B [30], PCTM6B [30], and PICO [31] for Corona, Firefly, and Flexishare photonic NoCs (PNoCs). Bars show mean values of the worst-case OSNR across 100 fabrication process variation maps; confidence intervals show variation in the worst-case OSNR.

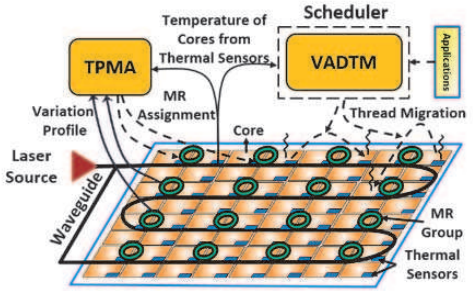

Fig. 7. Overview of LIBRA framework that integrates a device-level thermal and process variation aware microring assignment mechanism (TPMA) and a system (operating system) level variation-aware anti wavelength-shift dynamic thermal management (VADTM) technique.

the architecture-layer (*e.g.*, for optical switching applications). In contrast, cross-layer approaches involve enhancements at one or more of the device, circuit, architecture, and system (operating system and/or middleware) layers in a cooperative manner. Such techniques can be significantly more effective than single-layer techniques in achieving holistic design goals such as energy efficiency. In this section, we summarize our recent efforts in enabling cross-layer design solutions in silicon photonic interconnects to improve such network performance under crosstalk and runtime thermal variations. We believe that a fundamental requirement to enable efficient cross-layer design solutions is to develop computationally efficient and accurate compact models to enable exchanging design objectives and impacts across different design layers.

In [25], we proposed the HYDRA cross-layer framework to minimize crosstalk in silicon photonic interconnects, while improving energy-efficiency of data transfers. HYDRA combined multiple device-layer and circuit-layer techniques into a cross-layer framework. A device-layer approach was utilized for intermodulation (IM) crosstalk [26] mitigation by placing additional MRRs at modulating and receiving nodes to reduce IM noise. Another device-layer approach was utilized for heterodyne crosstalk mitigation that used double MRRs to improve worst-case OSNR in detectors by tailoring the MRRs' pass-bands to have steeper roll-off. Lastly, a circuit-layer technique was proposed for heterodyne crosstalk mitigation that improved the worst-case OSNR in detectors by encoding data to avoid undesirable data value occurrences. The synergistic combined effect of using the two device-layer techniques and one circuit-layer enhancement in HYDRA was shown to improve the worst-case OSNR by up to 5.3× for the Corona [27], Firefly [28], and Flexishare [29] photonic NoC (PNoC) architectures in the presence of fabrication process variations. Fig. 6 summarizes the OSNR improvement across PNoCs with the cross-layer HYDRA framework, when compared to the baseline PNoC architecture and several single-layer crosstalk mitigation solutions. HYDRA also had additional benefits of lower latency by up to 3.2% and lower energy consumption by up to 5.9% compared to these single-layer solutions.

Runtime variations due to runtime temperature fluctuations on a chip also create a significant challenge for silicon photonics designers. As discussed earlier, the resonant wavelength of an MRR is sensitive to thermal variations with up to a 7.4 nm shift in the resonance on a state-of-the-art 64-core processor chip [15]. Such a resonance shift causes serious wavelength coupling failures, prompting the need for dynamic MRR tuning. However, device-level tuning incurs costs in power and latency, as also discussed earlier. In [15], we proposed the LIBRA cross-layer framework to reduce the overhead of single-layer (*i.e.*, device-layer) optimization for overcoming the effect of thermal variations. Fig. 7 indicates a high-level overview of this cross-layer framework. A thermal and process variation aware MRR assignment (TPMA) mechanism was proposed at the device level that dynamically assigns each MRR to the nearest available carrier wavelength, to enable reliable modulation and reception of data while maintaining the maximum possible bandwidth. This device-level mechanism also adaptively selects the least power-consuming method from thermal tuning and current injection tuning as the preferred method for process- and thermal-variation remedy, and thus, reduces the total power for variation mitigation in the PNoC. However, limiting the peak temperature swings below threshold levels is essential to further reduce the total power for a holistic variation mitigation solution. To achieve this, LIBRA utilizes a variation-aware anti-wavelength-shift dynamic thermal management (VADTM) scheme that uses a support vector regression (SVR) machine learning based temperature prediction and dynamic thread migration between cores, to avoid on-chip thermal threshold violations, minimize on-chip thermal hotspots, and reduce tuning power for MRRs. The LIBRA cross-layer framework was shown to reduce the total power dissipation by up to 61.3% (thermal and current injection tuning power by up to 76.2%), and the total energy by up to 57.3% on the Corona and Flexishare PNoC architectures, compared to single-layer variation mitigation approaches at the device and circuit levels.

IV. Conclusion

Silicon photonic interconnect has emerged to boost the communication performance in today's increasingly complex

high-performance computing systems. However, the fundamental building blocks in such interconnects suffer from a number of issues both at design-time (*e.g.*, fabrication process variations) and at runtime (*e.g.*, thermal variations and aging effects). Although the design space of HPC systems integrating silicon photonics is a multi-layer one, most of the current solutions proposed to address such challenges rely only on a single design layer. Consequently, they can at most improve the performance of that particular design layer while often imposing performance degradation on the other design layers. In this paper, we discussed the promise of cross-layer design solutions that can provide improvements at one or more of the device, circuit, architecture, and system layers in a cooperative manner. We presented a few examples of such cross-layer design solutions to improve silicon photonic interconnect performance in terms of crosstalk as well as reliability and performance under thermal variations. We believe that such cross-layer solutions can be significantly more effective than single-layer techniques in achieving holistic design goals such as energy efficiency and variation resilience.

REFERENCES

[1] AMD EPYC Processor Family. [Online]. Available: https://www.amd.com/en/products/epyc

[2] Intel Xeon Platinum Processor Family. [Online]. Available: https://www.intel.com/content/www/us/en/products/processors/xeon/

[3] NVIDIA Turing Architecture. [Online]. Available: https://www.nvidia.com/en-us/geforce/turing/

[4] AMD RDNA GPU Architecture. [Online]. Available: https://www.amd.com/en/technologies/rdna

[5] Cerebras Wafer-Scale Engine. [Online]. Available: https://www.cerebras.net/

[6] M. Nikdast, G. Nicolescu, S. L. Beux, and J. Xu, *Photonic Interconnects for Computing Systems: Understanding and Pushing Design Challenges*. Wharton, TX, USA: River Publishers, 2017.

[7] Y. Shen, X. Meng, Q. Cheng, S. Rumley, N. Abrams, A. Gazman, E. Manzhosov, M. S. Glick, and K. Bergman, "Silicon photonics for extreme scale systems," *Journal of Lightwave Technology*, vol. 37, no. 2, pp. 245–259, January 2019.

[8] M. Nikdast, G. Nicolescu, J. Trajkovic, and O. Liboiron-Ladouceur, "Chip-scale silicon photonic interconnects: A formal study on fabrication non-uniformity," *Journal of Lightwave Technology*, vol. 34, no. 16, pp. 3682–3695, August 2016.

[9] M. Nikdast, G. Nicolescu, J. Trajkovic, and O. Liboiron-Ladouceur, "Modeling fabrication non-uniformity in chip-scale silicon photonic interconnects," in *Design, Automation, and Test in Europe (DATE) Conference Exhibition*, March 2016, pp. 115–120.

[10] Y. Ye, Z. Wang, P. Yang, J. Xu, X. Wu, X. Wang, M. Nikdast, Z. Wang, and L. H. K. Duong, "System-level modeling and analysis of thermal effects in wdm-based optical networks-on-chip," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 33, no. 11, pp. 1718–1731, November 2014.

[11] Z. Lu, J. Jhoja, J. Klein, X. Wang, A. Liu, J. Flueckiger, J. Pond, and L. Chrostowski, "Performance prediction for silicon photonics integrated circuits with layout-dependent correlated manufacturing variability," *Optics Express*, vol. 25, no. 9, pp. 9712–9733, May 2017.

[12] M. Bahadori, M. Nikdast, S. Rumley, L. Y. Dai, N. Janosik, T. Van Vaerenbergh, A. Gazman, Q. Cheng, R. Polster, and K. Bergman, "Design space exploration of microring resonators in silicon photonic interconnects: Impact of the ring curvature," *Journal of Lightwave Technology*, vol. 36, no. 13, pp. 2767–2782, July 2018.

[13] K. Skadron, M. R. Stan, K. Sankaranarayanan, W. Huang, S. Velusamy, and D. Tarjan, "Temperature-aware microarchitecture: Modeling and implementation," *ACM Transactions on Architecture Code Optimization*, vol. 1, no. 1, pp. 94–125, 2004.

[14] F. G. Della Corte, M. Esposito Montefusco, L. Moretti, I. Rendina, and G. Cocorullo, "Temperature dependence analysis of the thermo-optic effect in silicon by single and double oscillator models," *Journal of Applied Physics*, vol. 88, no. 12, pp. 7115–7119, 2000.

[15] S. V. R. Chittamuru, I. G. Thakkar, and S. Pasricha, "LIBRA: Thermal and process variation aware reliability management in photonic networks-on-chip," *IEEE Transactions on Multi-Scale Computing Systems*, vol. 4, no. 4, pp. 758–772, October 2018.

[16] P. Dong, S. Liao, D. Feng, H. Liang, D. Zheng, R. Shafiiha, C.-C. Kung, W. Qian, G. Li, X. Zheng, A. V. Krishnamoorthy, and M. Asghari, "Low vpp, ultralow-energy, compact, high-speed silicon electro-optic modulator," *Optics Express*, vol. 17, no. 25, pp. 22 484–22 490, December 2009.

[17] S. V. R. Chittamuru, I. Thakkar, and S. Pasricha, "Analyzing voltage bias and temperature induced aging effects photonic interconnects for manycore computing," in *ACM System Level Interconnect Prediction Workshop (SLIP)*, June 2017.

[18] M. Mohamed, Z. Li, X. Chen, L. Shang, and A. R. Mickelson, "Reliability-aware design flow for silicon photonics on-chip interconnect," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, no. 8, pp. 1763–1776, August 2014.

[19] J. Ahn, M. Fiorentino, R. G. Beausoleil, N. Binkert, A. Davis, D. Fattal, N. P. Jouppi, M. McLaren, C. M. Santori, R. S. Schreiber, S. M. Spillane, D. Vantrease, and Q. Xu, "Devices and architectures for photonic chip-scale integration," *Applied Physics A*, vol. 95, no. 4, pp. 989–997, June 2009.

[20] M. Bahadori, A. Gazman, N. Janosik, S. Rumley, Z. Zhu, R. Polster, Q. Cheng, and K. Bergman, "Thermal rectification of integrated microheaters for microring resonators in silicon photonics platform," *Journal of Lightwave Technology*, vol. 36, no. 3, pp. 773–788, February 2018.

[21] P. Dong, W. Qian, H. Liang, R. Shafiiha, D. Feng, G. Li, J. E. Cunningham, A. V. Krishnamoorthy, and M. Asghari, "Thermally tunable silicon racetrack resonators with ultralow tuning power," *Optics Express*, vol. 18, no. 19, pp. 20 298–20 304, September 2010.

[22] I. G. Thakkar and S. Pasricha, "Mitigating the energy impacts of VBTI aging in photonic networks-on-chip architectures with multilevel signaling," in *International Green and Sustainable Computing Conference (IGSC)*, October 2018, pp. 1–7.

[23] S. Namnabat, K.-J. Kim, A. Jones, R. Himmelhuber, C. T. DeRose, D. C. Trotter, A. L. Starbuck, A. Pomerene, A. L. Lentine, and R. A. Norwood, "Athermal silicon optical add-drop multiplexers based on thermo-optic coefficient tuning of sol-gel material," *Optics Express*, vol. 25, no. 18, pp. 21 471–21 482, September 2017.

[24] A. Mirza, F. Sunny, S. Pasricha, and M. Nikdast, "Silicon photonic microring resonators: Design optimization under fabrication non-uniformity," in *Design, Automation, and Test in Europe (DATE) Conference and Exhibition*, March 2020.

[25] S. V. R. Chittamuru, I. G. Thakkar, and S. Pasricha, "HYDRA: Heterodyne crosstalk mitigation with double microring resonators and data encoding for photonic nocs," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 1, pp. 168–181, January 2018.

[26] K. Padmaraju, X. Zhu, L. Chen, M. Lipson, and K. Bergman, "Intermodulation crosstalk characteristics of wdm silicon microring modulators," *IEEE Photonics Technology Letters*, vol. 26, no. 14, pp. 1478–1481, July 2014.

[27] D. Vantrease, R. Schreiber, M. Monchiero, M. McLaren, N. P. Jouppi, M. Fiorentino, A. Davis, N. Binkert, R. G. Beausoleil, and J. H. Ahn, "Corona: System implications of emerging nanophotonic technology," in *International Symposium on Computer Architecture*, June 2008, pp. 153–164.

[28] Y. Pan, P. Kumar, J. Kim, G. Memik, Y. Zhang, and A. Choudhary, "Firefly: Illuminating future network-on-chip with nanophotonics," *Special Interest Group on Computer Architecture News*, vol. 37, no. 3, pp. 429–440, 2009.

[29] Y. Pan, J. Kim, and G. Memik, "Flexishare: Channel sharing for an energy-efficient nanophotonic crossbar," in *High-Performance Computer Architecture*, January 2010, pp. 1–12.

[30] S. V. R. Chittamuru and S. Pasricha, "Crosstalk mitigation for high-radix and low-diameter photonic noc architectures," *IEEE Design Test*, vol. 32, no. 3, pp. 29–39, June 2015.

[31] S. V. R. Chittamuru, I. G. Thakkar, and S. Pasricha, "PICO: Mitigating heterodyne crosstalk due to process variations and intermodulation effects in photonic nocs," in *ACM/EDAC/IEEE Design Automation Conference (DAC)*, June 2016, pp. 1–6.