Design of a Reliable Power Delivery Network for Monolithic 3D ICs*

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***Abstract*—As Moore's law hits physical limits, monolithic 3D (M3D) integration based on fine-grained monolithic inter-tier vias is emerging as a promising technique to continue performance, power, and area improvements. However, the design of a reliable power delivery network (PDN) for M3D integrated circuits (ICs) is a formidable challenge due to higher power and current densities. In addition, compared to traditional designs, interconnects in M3D designs are more susceptible to electromigration and stress migration. Yield loss resulting from the power-supply noise (PSN) in functional and testing mode is also a major concern for M3D ICs. In this paper, we describe recent research efforts that provide solutions to mitigate these reliability concerns in M3D ICs.**

I. Introduction

Three-dimensional (3D) integration is a promising way to achieve high functionality and reduce chip footprint. The improvements in performance, power, and area (PPA) can be attributed to the decrease in wirelength in 3D designs. Die/wafer bonding with through-silicon vias (TSVs) is widely used in modern 3D integration technologies because it does not have a major impact on the typical fabrication flow. However, TSV fabrication causes tensile stress around copper TSVs due to the mismatch in the coefficients of thermal expansion between silicon and copper. Keep-out-zones (KOZs) offer a conservative solution to protect cells and wires from TSV-induced stress, but its large size impacts placement and routing, which can negate the benefits of 3D integration.

Monolithic 3D (M3D) is a more recent 3D integration technology that leverages fine-grained monolithic inter-tier vias (MIVs) to achieve extremely thin device layers and high alignment precision [1]. Compared with TSVs, MIVs are one to two orders of magnitude smaller in the size and the induced capacitance is negligible [2], as shown in Figure 1. These advantages enable MIVs to be used in massive quantities within designs, which allows high integration density and significant reduction in wirelength. As a result, M3D results in increased performance with lower power consumption. Depending on the way tier partitioning is carried out, there are three categories of M3D IC designs: (i) transistor-level, (ii) gate-level, and (iii) block-level integration. Transistor-level M3D ICs divide P-channel and N-channel transistors into different tiers. In gate-level and block-level M3D, standard cells and functional blocks are split over multiple tiers, respectively. The interconnects between tiers in all three designs are made up of signal MIVs.

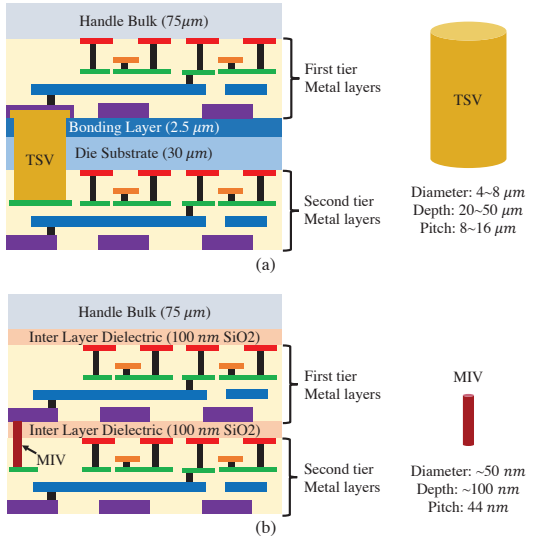

Fig. 1. Examples of 3D integration methods: (a) TSV-based 3D IC; (b) M3D IC. The figure is adapted from [3] and redrawn.

The benefits of M3D integration are accompanied by several challenges and barriers to commercial exploitation. The design of a reliable power delivery network (PDN) is a major concern for M3D ICs because of high power and current densities. Compared to traditional designs, the PDN for an M3D IC serves more devices in all the tiers with fewer C4 bumps, leading to higher voltage droop [4]. Electromigration (EM) is also a major concern for PDN reliability [5]. EM-induced opens and shorts may produce errors in circuit operation and reduce the lifetime of the device. Allocating more resources (e.g., routing tracks and back-end-of-the-line metals) for the PDN is an effective approach to address the above issues, but M3D ICs are extremely crowded with vertical interconnections. Therefore, the routing-congestion problem increases the complexity of PDN designs. The circuit performance and

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reliability needs to be jointly optimized in an effective PDN design flow.

Power-supply noise (PSN) is another concern in M3D ICs. In both functional mode and testing mode, high PSN may lead to erroneous results during circuit operation. With high switching activity during scan shift and capture, the testing mode suffers more from the excessive PSN, and this problem may result in the failure of fault-free chips on the tester, i.e., yield loss. A number of methods for power-aware testing have been presented in the literature [6]–[8]. A test-generation flow featuring guaranteed launch safety for at-speed scan testing is presented in [9]. However, prior work has largely ignored PSN challenges that arise from M3D integration. To improve the circuit performance and minimize undesirable yield loss, careful analysis of PSN for M3D ICs needs to be carried out.

In this paper, we review major challenges associated with a reliable PDN design in M3D ICs, and describe recent research efforts to address these challenges. For 3D integration technologies, we perform a survey of existing PDN models for both TSV-based and M3D ICs. Comparison between different models is presented; this comparison can help us to identify unexplored problems and set clear directions for future research. Fundamental concepts related to the analysis of PSN are also presented.

The rest of the paper is organized as follows. Section II describes the challenges related to PDN design. Section III presents PDN models and optimization methods for both TSV-based and M3D ICs. An analysis of the power-supply noise is presented in Section IV. Finally, Section V concludes the paper.

II. PDN Design Challenges

A. Voltage droop

In advanced technology nodes, high power density, low supply voltage, and high clock frequency increase the complexity of designing a PDN. A non-ideal PDN may cause functional failures and performance degradation due to parasitics-induced voltage droop. Voltage droop is composed of two components: (i) IR-drop resulting from instantaneous currents through resistances, and (ii) Ldi/dt drop resulting from rapid changes in currents. Considerable research efforts have been devoted to voltage droop issues. Node-based and row-based algorithms are described in [10] to quickly analyze a large power grid. Dynamic IR-drop analysis is performed in [11]. A methodology is presented in [12] to precisely verify the worst-case voltage droop conditions. Decoupling capacitors (decaps) are utilized as charge storage to mitigate voltage droop; these include the intrinsic decoupling capacitance and intentionally inserted decoupling capacitors [13] [14]. However, adding decaps on a chip may produce resonance oscillations in the PDN [15], leading to significant Ldi/dt drop if the resonance frequency overlaps the operating frequency range of the system. In M3D integration, both static and dynamic voltage droop are more severe than in conventional 2D ICs. Table I shows a comparison for the discrete cosine transform (DCT) benchmark [14].

TABLE I
Static and dynamic voltage droop for the DCT benchmark [14]

	2D	M3D	Increase (Δ)
Static voltage droop (mV)	27.6	68.1	146.7%
Dynamic voltage droop (mV)	323.4	346.9	7.3%

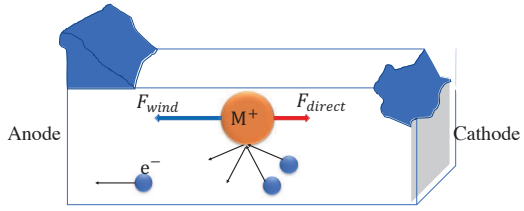

Fig. 2. EM-induced void and hillock, where F_{direct} is the electrostatic interaction with the field, and F_{wind} is the momentum transfer from electrons.

B. Electromigration

EM is a mass transport process attributed to momentum transfer between conducting electrons and diffusing metal atoms in a conductor. With a sufficiently long period of time, EM may nucleate a void near the cathode side and a hillock near the anode side, leading to an open or a short in electronic devices, as shown in Figure 2. Reliability threats caused by EM become more significant with technology scaling due to the increased current density. Large unidirectional currents make PDN more susceptible to EM. Black's Equation [16] has been widely used to approximate the mean-time-to-failure (MTTF) caused by EM:

$$MTTF = Aj^{-n}e^{\frac{E_a}{k_B T}} \tag{1}$$

where A is a constant, j is the current density, n is the current density exponent, k_B is the Boltzmann's constant, T is the absolute temperature, and E_a is the EM activation energy. The current exponent, n, was determined as 2 in Black's derivation, but experiments nowadays show that it depends on test structures and conditions [17]. For wires with diffusion boundaries, the Blech limit [18] can be employed:

$$(j \times L) \leq \frac{\Omega \sigma_{crit}}{eZ\rho} \tag{2}$$

where L is the metal wire length, σ_{crit} is the critical stress for failure caused by void or hillock nucleation, eZ is the effective charge of migrating metal atoms, and ρ is the metal resistivity. Wires within the Blech limit do not fail due to EM. Recent research shows that Black's Equation may not be valid under all conditions. [5] proposes a physics-based EM modeling method and derives the saturated void volume effect in void growth. [19] provides a model that considers the influence of material parameter variations. A transient analysis method considering EM effects in multi-segment wires is developed in [20]. The PDN in M3D ICs suffers from higher susceptibility to EM due to higher current density compared to traditional 2D designs.

C. Routing Congestion

The trade-off between PDN robustness and routing resources needs to be carefully addressed. The PDN creates blockages in signal routing, which result in an increase in the total wirelength for cell-to-cell interconnections. In the design of 3D ICs, routing congestion issues are more severe due to the limited amount of resources available for 3D connections. TSV-based 3D ICs can directly deliver power from top tiers to bottom tiers but they require the KOZs for power TSVs. In M3D IC designs, the topmost metal layers of the bottom tier and the bottom-most metal layers of the top tier are dedicated for the PDN, leading to a reduction in resources available for signal routing [2]. Blockages caused by MIVs exacerbate the routing congestion problem. A non-ideal PDN may considerably increase the total wirelength for signal routing and diminish the benefits of 3D integration. Therefore, routing resources should be carefully allocated for the M3D PDN in order to reduce the impact of congestion.

III. PDN for 3D ICs

A. PDN models for TSV-based Designs

In the realm of 3D integration, TSV-based ICs are relatively more mature than M3D, hence there has been more research on PDN optimization for TSV-based designs. Therefore, we first survey existing TSV-based PDN models.

In [21], a comprehensive analysis of the PDN for different TSV sizes is performed. Contrary to what we might expect, the IR-drop in 3D PDNs saturates with increasing TSV size. Therefore, an appropriate trade-off between the TSV size and performance degradation must be carried out. With optimum TSV sizing, different strategies have been proposed to mitigate the problems of IR-drop and Ldi/dt drop. Experimental results on realistic benchmarks show that increasing C4 bump granularity greatly mitigates the voltage droop, which means that targeting off-chip components is an effective way to optimize PDN designs. The use of coaxial TSVs is another solution for optimizing the performance of a TSV-based PDN. Without any area and performance penalty, coaxial TSVs can reduce routing blockages as well as add more decaps. The flexibility of overlaying signal and power routing enables TSV-based 3D ICs to route additional signals under the same footprint.

EM issues in TSVs and surrounding wires are studied in [22]. TSVs and wires are modeled to quantify the EM-induced stress under different situations. TSV models present the hotspot of atomic concentration distribution resulting from EM in a TSV. With increasing TSV radius and landing pad size, large stress gradients are more likely to be created. Wire models concentrate on the TSV-induced stress in surrounding wires for various locations relative to the TSV center. Since the center suffers significantly from EM, keeping wires away from TSV centers and preventing wires in lower metal layers from crossing TSVs can improve the robustness of IC design. Stress and reliability libraries that can be used to estimate the impact of TSVs on wires are presented in [23].

PDN impedance and switching noise are discussed in [24]. Below high-frequency regions, the PDN impedance of a TSV-based 3D IC is similar to that of a conventional 2D device because the off-chip PDN dominates. For frequency regions above 100 MHz, PDN impedance starts to be significantly affected by the 3D integrated chip. Besides PDN impedance, the switching activity is another contributor to the noise. [24] carries out current simulation, and calculates both the time-domain waveform as well as frequency-domain spectrum with amplitude and phase. The simultaneous switching noise amplitude spectrum in TSV-based 3D ICs is obtained by multiplying the frequency-domain average PDN impedance with the switching current amplitude. Next, the noise waveform is calculated by mapping the result to the time domain. In higher frequency regions, the coupling through TSVs creates resonance modes. A large amount of noise may be generated when the resonance modes overlap with the operating frequency; therefore, it is necessary to simulate switching noise for a robust TSV-based 3D PDN design.

B. PDN Models for M3D Integration

Due to the difference in technology, fabrication methods, and dimensions, TSV-based models cannot be directly mapped to M3D ICs. Therefore, a fresh look is needed for the analysis of the PDN for M3D. Recent work has presented three PDN models to target different challenges related to performance and reliability [2] [14] [25]. A comparison among those models is shown in Table II.

In [2], a full chip impact study, with and without PDN designs, is conducted; this study includes wirelength, MIV count, power consumption, and IR-drop. Thermal impact has been pointed out as another key concern for an M3D PDN. From the analysis results, it can be seen that although PDNs help improve the temperature profile by enhancing lateral conductivity, the maximum temperature obtained is still worse than that in designs without a PDN. To optimize an M3D PDN, clustered power and ground rails are advocated instead of equally spaced rails. This approach prevents long detours by saving more continuous space for signal routing and MIV planning. The reduction in the number of top metal layers and the utilization of intermediate metal layers for the PDN help us to achieve lower power consumption without exceeding the IR-drop limits. These methodologies provide useful guidelines for a desirable PDN design.

One of the major difference in fabrication flow between TSV-based ICs and M3D ICs is that transistors in different tiers are processed on the same wafer in M3D, enabled by a low-temperature vertical integration process that prevents damage to interconnects and cells in the bottom tier. Therefore, specific design flows are necessary to generate optimized physical designs for M3D ICs. Extended version of the Shrunk-2D [26] has been utilized in M3D PDN optimization [14] [25], as shown in Figure 3. Within the design flow, methods published in the literature aim at different targets in the M3D PDN optimization step.

A simplified RLC model of a system-level PDN structure, including the PCB, package, C4 bump, and 3D integrated chip, is presented in [14] to evaluate statistical and vector-based power consumption. Comprehensive studies demonstrate that Ldi/dt drop has less impact than static IR-drop due to

TABLE II
COMPARISON BETWEEN DIFFERENT M3D PDN MODELS AND DESIGN METHODS [2] [14] [25].

	[2]	[14]	[25]
Level of granuarity	Gate-level	Gate-level	Gate-level
Target	Full-chip impact	System-level analysis	Reliability
Analysis	Full-chip PDN impact Thermal impact	Static rail Dynamic rail Frequency- and time-domain	Current density Mean-time-to-failure Power-supply noise
Optimization methodology	Power and ground rails design Metal layers usage Full PDN analysis results	Top-tier cell repositioning Asymmetric top- and bottom-tier PDN	GP-based design space exploration

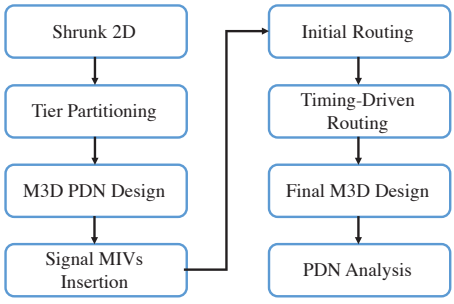

Fig. 3. Design flow for an M3D PDN.

implicit and explicit decaps in the 3D PDN design. Also, an important observation is made in the frequency- and time-domain analysis: the high resistance of M3D PDNs actually improves resiliency against AC noise. Therefore, it is crucial to reduce IR-drop in a robust PDN design. The work in [14] introduces two methodologies to optimize M3D PDNs: (i) top-tier cell repositioning, and (ii) asymmetric top- and bottom-tier PDN. Both these methods are shown to be effective in alleviating IR-drop.

A chip-level PDN optimization flow addressing reliability issues is presented in [25]. EM-induced MTTF is modeled in terms of the void nucleation time [5] for the bottom tier and Black's equation for the top tier. With a design space defined by power and ground MIV counts, distributions of MIVs, and restricted routing resources, the MTTF and the worst-case IR-drop for each design are obtained. Taking the design space and estimated values of MTTF/IR-drop in account, [25] leverages genetic programming (GP)-based design space exploration to find the best PDN design features. PSN analysis under these design features is conducted to evaluate the expected yield loss. Simulation results show that the PDN design thus obtained can mitigate reliability problems, and result in decreased current densities in wires and lower yield loss during testing.

IV. Power Supply Noise

A. Functional Mode

PSN refers to the voltage differences between the local references of drivers and receivers. In traditional two-cycle testing, it is difficult to accurately simulate normal functional operation due to the mismatch of PSN between functional and testing mode. In [27], Pseudo-functional K-Longest Path Per Gate (PKLPG) test is proposed to generate delay tests to better mimic functional mode. A simulation-based method is applied to maximize effective weighted switching activity to control PSN for PKLPG test, which can test the longest paths with a similar PSN as seen during normal functional operation.

A considerable amount of prior work on 3D integration has focused on modeling power delivery and analyzing voltage droop to tackle PSN problems. [28] presents a simplified 3D stacked circuit model. By analytically solving a system of partial differential equations composed of Helmholtz and Poisson equations with boundary conditions, the frequency- and time-domain transient power noise can be obtained. SPICE simulations show that solutions obtained using this model are less than 4% sub-optimal under the worst-case scenario. When only one die in a 3D integrated chip is switching, the worst-case peak noise is lower than that for a single die case because non-switching dies can behave as decaps to reduce the noise. However, when all the dies are switching simultaneously, there is a greater likelihood that the induced noise will be well beyond the acceptable limit, even in the bottom-most die. To suppress the noise level, additional dies occupied entirely by decaps can be helpful, but this method has the drawback of a longer cooling path. Increasing the number of power and ground I/O pins to provide higher density and better mechanical properties is another solution to the power integrity problem.

The work in [29] specifically focuses on modeling and characterization of decaps. Along with T models, which consist of two series subcircuits (R and L) and one shunt subcircuit (C and G) in the vertical direction, a dedicated equivalent circuit model for PSN analysis is obtained by electromagnetically extracting all RLGC and converting them into the SPICE format. On-chip decaps, interposer decaps, and package decaps are considered in the analysis. On-chip decaps include polysilicon-insulator capacitors, MOS capacitors, metal-insulator-metal capacitors, and lateral flux capacitors. Large on-chip decaps are desired, whereas interposer and package decaps are not very effective for reducing the worst-case voltage droop. To determine the number of required on-chip decaps, it is needed to analyze feed-in voltages and identify hot spots. Location is another important factor in decap optimization. Placing decaps near active circuits such as drivers and high-power units can lead to more effective noise relief than a random arrangement of decaps.

Temperature is another major contributor to PSN. The resistivity of supply rails is a function of temperature. The Joule heating created by high currents flowing through a node for a long time may increase local temperature, leading to significant voltage droop and EM. [30] uses electrical and thermal co-simulation to improve PSN simulation accuracy for M3D IC designs. In an iterative process, a thermal map is first obtained through a stand-alone thermal analysis, followed by a dynamic voltage-droop analysis. Next, the generated power distribution serves as an input for thermal analysis. This procedure terminates when the changes in voltage droop and temperature between iterations are less than 5%. Experimental results show that the undesirable peak chip temperature and worst-case voltage droop can be considerably reduced by appropriately choosing the number of power and ground MIVs, as well as the MIV density. However, the MIV count needs to be carefully determined.

B. Testing Mode

PSN in scan-testing mode is relatively larger than in functional mode because a large number of transitions occur in a short time. A model to detect the PSN level and impact on delay testing is presented in [31]. In the model, the effective region for a switching device is computed, which refers to the area whose RC time constant does not exceed the clock cycle time. Capacitors within the effective region provide current to the device, while others are considered irrelevant to the noise analysis. With effective regions, the proposed method can achieve a fast analysis during delay testing. The correlation between simulations and measurements shows that the extra delay on the tester can be well explained by PSN impacts. [31] also applies don't care bit filling techniques, random fill of don't care bits in test patterns, to the analysis. Experimental results show that a higher rate of filling don't care bits to 1 may generate more switching activity and induce PSN variation, which creates a great variation in delay. Therefore, PSN needs to be carefully addressed for pattern generation and timing analysis during delay testing.

Automatic test pattern generation (ATPG) is an integral part of the IC design flow today. PSN-aware ATPG has been studied extensively [32] [33]. An average power model to analyze static as well as dynamic IR-drops is presented in [33]. This approach leads to a new framework to generate PSN-aware test patterns using existing commercial ATPG tools. The proposed switching cycle average power (SCAP) metric refers to the average power consumption of each test pattern during the time frame corresponding to the switching activity. With SCAP, patterns with lower switching activity but with a very short time frame can be taken into consideration, which is ignored in the previous power model [34]. By using Synopsys VCS simulator to calculate SCAP, PSN-aware test patterns can be generated by setting an upper limit on SCAP value of each pattern. Comparison between different don't care bit filling techniques shows that assigning don't care bits to 0 can achieve the best results with all SCAPs below the threshold. The test patterns obtained in this way are tolerant to IR-drop during at-speed delay test and there is only a 4% increase in the number of test patterns.

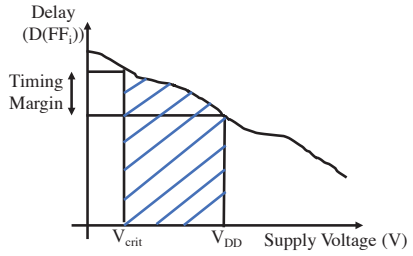

Fig. 4. Illustration of the delay distribution for the shift/capture path [25].

Test generation for M3D-specific IC designs has yet to be investigated. Nevertheless, PSN during testing for M3D designs has recently received attention. In [25], dynamic simulation of transition delay patterns is carried out to analyze the impact of PSN on the proposed PDN model after optimization. The optimized models of realistic workloads can reduce the worst-case power-supply droop compared to the baseline. Moreover, the analysis shows that the lower the power budget for scan shift and capture, the lower the maximum voltage droop. However, the impact of PSN is more severe during scan shift since the shift operation leads to high switching activity.

C. Yield Loss

To quantify the impact of PSN for the proposed M3D PDN design, [25] provides a metric to indicate the likelihood of eliminating a good chip on the tester. The delay distribution for the shift/capture path ending at a scan cell (SC) can be illustrated as shown in Figure 4, with the approximation that delay varies linearly with the supply voltage [35]. Consequently, the probability of capturing a correct value at SC_i during scan shift can be expressed as:

$$P_S(SC_i) = \int_{V_{cirt}}^{V_{DD}} D_S(v)d(v) \tag{3}$$

The probability of capturing a correct value during capture can be expressed as:

$$P_C(SC_i) = \int_{V_{cirt}}^{V_{DD}} D_C(v)d(v), \tag{4}$$

where V_{crit} is the supply voltage at which the timing margin on the shift path or scan path becomes zero, and $D_S(v)$ ($D_C(v)$) is the delay distribution with the smallest slack for SC_i of the shift path (capture path). The probability that SC_i captures a wrong value during testing is denoted as $P'(SC_i)$, and it can be expressed as:

$$P'(SC_i) = 1 - P_S(SC_i) \times P_C(SC_i) \tag{5}$$

Supposed there are N SCs in the circuit under test. The yield loss can be calculated as: $\sum_{i=1}^{N} P'(SC_i)$. The analysis in [25] shows that the proposed M3D design leads to considerably lower yield loss compared with the baseline.

V. Conclusion

We have described major challenges encountered in the design of PDN for 3D ICs. We have reviewed PDN models that have been proposed for TSV-based and M3D ICs and highlighted the key differences between them. We have also described recent research that has attempted to tackle the problem of PSN in both functional mode and test mode, and we also described a method to quantify the yield loss due to PSN. As M3D integration receives more attention, PDN reliability and optimization become even more important. There is a need for concerted research effort for PDN reliability analysis and performance/reliability optimization.

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