# M3D-ADTCO: Monolithic 3D Architecture, Design and Technology Co-Optimization for High Energy Efficient 3D IC

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***Abstract*— Monolithic 3D (M3D) stands now as the ultimate technology to side step Moore's Law stagnation. Due to its nano-scale Monolithic Inter-tier Via (MIV), M3D enables an ultra-high density interconnect between Logic and Memory that is required in the field of highly energy efficient 3D integrated circuits (3D-ICs) designed for new abundant data computing systems. At design level, M3D still suffers from a lack of commercial tools, especially for Place and Route, precluding the capability to provide signoff M3D GDS. In this paper, we introduce M3D-ADTCO, an architecture, design and technology co-optimization platform aimed at providing signoff M3D GDS. It relies on a M3D Process Design Kit and the use of a commercial Place and Route tool. We demonstrate an area reduction of 23.61% at iso performance and power compared to a 2D RISC-V micro-controller based System on Chip (SoC) while creating space to increase (2x) the RISC-V instruction memory.**

***Keywords*— *Monolithic 3D (M3D), Signoff Design Flow & Methodologies, CAD Tools, Process Design Kit.***

## I. INTRODUCTION

M3D is a three-dimensional integration technology in which a second layer of active FET devices is fabricated monolithically on top of the first one, meaning that no post die or wafer fabrication stacking is required. Consequently, it provides a very high alignment precision and a significantly reduced inter-tier Via (MIV) size (50 nm diameter for 28 nm technology – same size than the others Vias). M3D technology requires a low temperature fabrication process of the top tier (under 500°C) well mastered in the CoolCube™ process [1]. Figure 1 presents the full range of 3D IC technologies and the diameter and pitch of the state of the art 3D interconnects. The capability to integrate active FET devices in the third dimension makes Gate-Level integration [2] down to Transistor-Level integration [3] possible. Recent works [4, 5] rely on Gate-Level M3D to dramatically increase the power efficiency of new computing architectures by providing ultra-thin interconnect between processing logic and memory. M3D is emerging as a technology to sidestep the stagnation in Moore's law by fabricating multiple tiers of tightly coupled processing logic with local memory. On the other hand, at the Computer Aided Design (CAD) level, M3D still suffers from a lack of commercial Place and Route (PnR) tool to provide a high quality M3D Graphic Database System (GDS). Since a MIV has the same dimensions as existing Vias, with a density up to 100 million of MIVs per mm², there is interest in automatically managing MIVs using a PnR tool and running a single PnR step. Unfortunately, no commercial PnR tool is capable of doing this, thus, all advanced M3D designs use a solution based on workarounds on top of commercial CAD tool, but none has yet proposed a solution capable of providing a M3D signoff GDS and using a commercial tool as is.

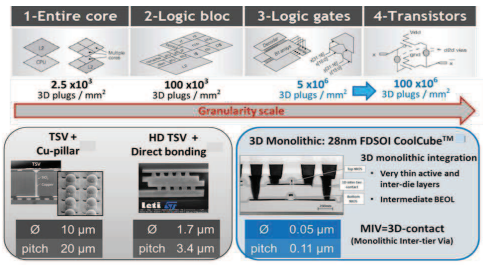



Figure 1 : 3D Technologies range and respective interconnect dimensions

In [7], the authors introduce a M3D design methodology that produces Performance, Power and Area (PPA) improvements compared to a 2D baseline circuit. We can see that many custom steps are introduced between placement and routing (e.g. pathfinding, bin based tier partitioning based on 2D reference circuit) in order to emulate 3D placement while the routing is still done tier-by-tier precluding post-placement optimizations. In [8], the authors propose a methodology capable of 3D placement and routing on a single step while wrapping MIV into cells and dummy wire but an initial 2D PnR is required to perform M3D PnR, which significantly increases the time to design a M3D-IC.

Instead, by providing a M3D PDKit aimed at manipulating MIVs as any other Vias and modifying library files for Standard Cells (SC) and SRAM Memories, makes possible the use of a commercial PnR tool without any custom steps. Consequently, all 2D PnR steps such as Floorplanning, Power Mesh, Design for Testability, Clock Tree and Routing are reusable and extendable for M3D. M3D-ADTCO that combines both M3D PDKit and commercial PnR tool is for the best of the authors' knowledge the first platform available for designing high quality M3D-IC GDS while analyzing the impact of M3D technology parameters that come into play at design level (e.g. number of metal layers needed for intermediate Back end of Line, MIV parasitics…). At architecture level, M3D-ADTCO allows fast silicon Performance, Power and Area (PPA) prototyping on any technology (28 nm FDSOI in this work).

The contributions of this paper are:

- M3D 28 nm FDSOI technology files (PDKit) required to perform M3D Signoff Place and Route including additional metal layers as well as MIV parasitics – **M3D PDKit**,
- M3D Signoff PnR methodology, including DFT and compatible with 2D commercial tools– **M3D PnR**,
- M3D signoff PnR experimentation with comparison to 2D baseline circuit – **M3D-ADTCO Experiment**.

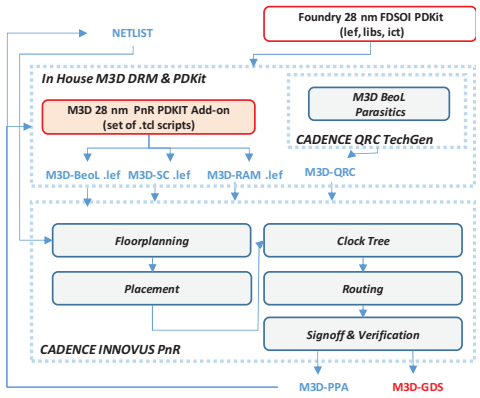



Figure 2 : M3D-ADTCO platform

## II. M3D-ADTCO Platform

In this section, we present our M3D-ADTCO platform composed of the M3D PDKit and the M3D Signoff PnR. First, we detail the M3D-PDKit content, in line with the M3D/CoolCube™ technology constraints and parameters; then, we demonstrate how a 2D commercial PnR tool is used to provide a single M3D signoff GDS.

Figure 2 presents our M3D-ADTCO platform content. It takes as inputs:

- the netlist of a circuit and its physical implementation constraints (.v & .sdc files),
- any foundry PDKit (e.g. 28 nm FDSOI in our case) that specifically contains technology (.lef) files for Back end of Line as well as for SC and SRAM memory blocks, timing and power library (.lib) files of the SC and the SRAM memory blocks and the Back end of Line (BeoL) parasitics (.ict) files.

It provides:

- a single M3D signoff GDS,
- a post PnR netlist for simulations and verifications.

In this work, we use twice the same technology, 28 nm FDSOI for top and bottom tiers, to build the M3D 28 nm FDSOI technology in which the MIVs are treated as any others Vias. A MIV connects the top tier lowest metal (M1) and the bottom tier highest metal (M6_bot) as illustrated in Figure 6. Indeed, to match the guidelines of the M3D cost model presented in [6], we have selected only six metal layers for the bottom tier BeoL over the ten available. Figure 3 presents the M3D 28 nm FDSOI technology and the MIV connectivity. The full BeoL stack is kept for the top tier with the last two metal layers (M9-M10) used for M3D Power Delivery Network (PDN). The SC are placed on the top tier above the pre-placed SRAM memory blocks on the bottom tier as mentioned in introduction, to enable a tight logic-memory integration. A SRAM memory block layout needs four metal layers in the 28 nm FDSOI technology. Thus, we dispose of two free layers (M5_bot and M6_bot) to extend the PDN from the top to bottom tier and use M5_bot stripes to supply the SRAM memories; but also to ease the 3D routing by jogging between top and bottom BeoL using both M5_bot and/or M6_bot. Moreover, we have a Ground Plane

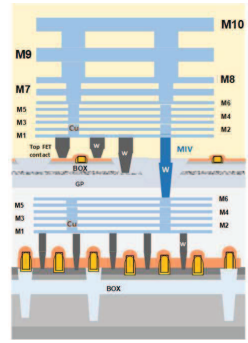



Figure 3 : M3D 28 nm FDSOI technology

(GP) that is used as the common reference for all the FDSOI flavored MOS devices in the top tier.

M3D-ADTCO has been set up using CADENCE QRCTechGen and CADENCE Innovus PnR tools, but it can be used with any others Electronic Design Automation (EDA) commercial tools.

### A. M3D PDKit

In this section, we detail M3D PDKit content and the methodology to generate M3D technology files required to perform signoff PnR and thus to generate the M3D GDS:

- the Technology Library Exchange Format (.lef) file in which each metal layer and Vias are physically described including direction, pitch, offset, spacing and width,
- the SC and Memory Library Exchange Format (.lef) files in which the SC and the SRAM Memory macros are physically described : X and Y dimensions, I/Os and Power pins layers and locations of SC and SRAM,
- the Parasitics (.ict) file which reflects the metal layers resistivity and dielectric capacitance of the technology. This file is compiled with QRCTechGen tool to provide an equivalent binary parasitics file (.qrc) used by the PnR tool to estimate the timings across the nets.

This subset of technology files is passed through a M3D PDKit generator to provide the resulting M3D 28 nm FDSOI PDKit [9]. The M3 PDKit generator is a subset of tcl scripts that automatically generates the M3D PDKit add-on files, and more particularly those necessary for PnR as described above.

M3D PDKit relies on our internal Design Rule Manual (DRM) that describes all the rules to match for the fabrication of the MIVs as well as the front end devices in the CoolCube™ cold process (top tier MOS devices). Figure 4 shows a MIV described as a Via (cut lef layer) in M3D.lef file. We can see that 50 nm width and 50 nm spacing with same net are used as introduced earlier. Additional design rules are added for the enclosure of metallization required above and beneath a MIV cut in line with the DRM. We use 25 nm for both M1 and M6_bot enclosure. M3D PDKit provides also set a MIVs matrix directly usable by the PNR tool, especially during the M3D Power Delivery Network (PDN) definition.

As a result, M3D PDKit is an add-on to any planar technology PDKit.

```
LAYER MIV
TYPE CUT ;

WIDTH    0.050 ;
SPACING 0.050  SAMENET ;
SPACING 0.110 ;

ENCLOSURE BELOW 0.025 0.025 ; # M6_BOT
ENCLOSURE ABOVE 0.025 0.025 ; #M1_TOP
```

Figure 4 : MIV described as a Via in M3D-BEOL LEF file

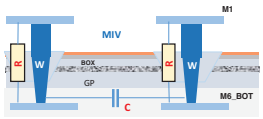



Figure 6 : MIV resistivity and dieletric capacitance

As introduced earlier, no commercial tools dispose of a legal 3D placement engine. Shrunk2D based flow [7], its evolution Cascade2D [8] and all related works in the state of the art specifically address this point. Indeed, the authors manage the 3D placement by shrinking the SC and the metal layers of the respective technology node used, before generating the bin based partitioned netlists for top and bottom tiers. Then, 2D routing is done on each tier with half de-shrunk SC. The advantage of the M3D-ADTCO platform is that the M3D physical views of the SC and the SRAM memory blocks are generated to be directly compliant with any 2D commercial tool. Actually, by just changing the attribute BLOCK by COVER, in the SRAM memory block .lef file, enables the SC or others SRAM memory block to be legally placed above. Consequently, 2D placement engine can optimize the placement of each SC just above the corresponding SRAM memory block and accordingly with the location of its IO pins.

Figure 5 presents the M3D SC legally placed above its memory as expected in [4, 5]. Note that the same methodology can be applied to the SC themselves enabling Logic-on-Logic M3D PnR. Moreover, the top SC.lef file is also modified. Indeed, we add an obstruction relative to the MIV-cut layer in each SC footprint to avoid the routing engine to fill a SC with a MIV. The PnR tool is guided during the routing step by the BeoL parasitics contribution (resistivity and dielectric capacitance) to take into account delay across the nets. As for the technology .lef file, we extend the .ict file for M3D. Figure 6 shows the resistivity and the dielectric capacitance involved by the MIV in CoolCube™ process. We take 100 Ohm for the Resistivity (10x higher than the others Vias) and 5 pF max for the dielectric Capacitance between M6_bot and M1 (half the same order of magnitude than other Vias) from internal data and simulation. As a result, we dispose now of the M3D.ict file that is compiled with CADENCE Techgen in order to generate the M3D-QrcTechFile, the binary file used by Innovus PnR tool to manage timing contribution of the nets.

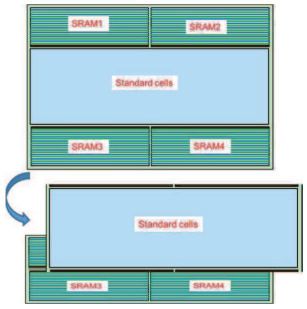



Figure 5 : M3D Logic-on-Memory partitioning concept

### B. M3D PnR

#### 1) M3D Floorplan and PDN-Mesh

Usually, a 2D PDN-Mesh is defined during the floorplan, using the last metal layers that are 2x to 4x thicker than first thin layers. A Ring in the periphery and a Mesh of these 2 layers are drawn targeting a density of 50% in order to avoid a major IR Drop drawback. Then, a myriad of Power Vias connect the PDN-Mesh layers to the power pins of the SC. Even if the SRAM macros have been modified to support legal overlap, the signal and power pins are still available for routing. As a result, we just need to extend this 2D PDN-Mesh thanks to Power MIVs beneath the Ring in the periphery of the circuit and to use stripes of M5_bot added to this effect to connect the M3D power ring to the SRAM power pins as illustrated in Figure 7. Additional MIVs can be instantiated in the core of the design to connect top and bottom mesh if needed (depending on the power budget of the bottom tier).

#### 2) M3D Placement, Clock Tree and Routing

As introduced in section II.B, 3D Placement is now possible. Figure 9 (a) shows the SC legally placed above the SRAM memory blocks. We benefit from the use of commercial tool to enable post placement optimization leading to find the optimal position of each SC and thus clock buffers during Clock Tree. MIVs are used to connect the clock pins of the SRAM memory blocks to the main tree. Finally, accurate timing driven routing and post route optimization are done taking into account the parasitics of the MIVs. Figure 9 (b) illustrates how the MIVs are automatically inserted to connect the clock pin of the SRAM memory macro to the main tree. We see that the routing engine places double MIVs, that is in line with Design for Manufacturing (DFM) guidelines.

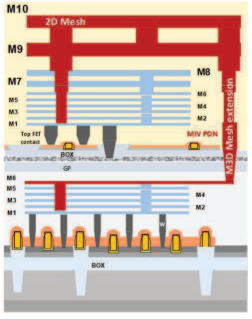



Figure 7 : 2D PDN extended beneath the ring with MIVs and stripes

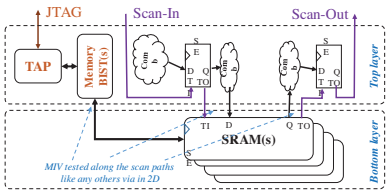


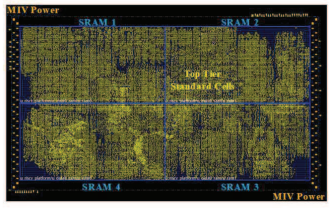

Figure 8 : M3D DFT scheme reused from 2D

*3) M3D DFT*

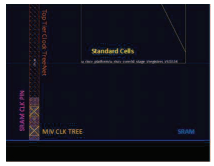
Unlike 3D stacking, in which the Known-Good-Dies (KGD) only are assembled, it is not forecasted to use the KGD strategy because of the monolithic fabrication process that does not really permit to test each tier independently. This strategy would lead to more complex test equipments and an increased fabrication time. Moreover, the huge amount of MIVs to diagnose makes impossible the utilization of Boundary Scan Registers as in [10]. However, the MIVs are now treated as the others Vias. Thus, we just need to include the MIVs in Design for Test (DFT) Scan and Built-In-Self-Test (BIST) paths and to provide a top tier DFT access including the pads and a Test Access Port (TAP) controller. Thus, we propose a rather simple 3D-DFT architecture inherited from 2D DFT and adapted to M3D:

- Memory BIST engines, using a TAP controller in the IEEE1687 standard,
- Full Scan logic, including the SRAM - Logic connectivity,
- a Join Test Action Group (JTAG) access using dedicated pads in the top tier.

This M3D-DFT architecture is presented in more details in Figure 8. The overall M3D-DFT architecture can be implemented using any DFT tool, such as Mentor Tessent tool. Finally, in terms of implementation, the overall M3D-DFT logic (BIST and Scan) is placed in the logic layer, and the routing of all DFT signals is then performed automatically by providing exactly the same Scan Chain Paths file (.scandef) than in 2D PnR.




(a) SC overlapping SRAM




(b) Clock Tree double MIVs

Figure 9 : (a) legal SC overlapping SRAM and (b) clock tree MIVs

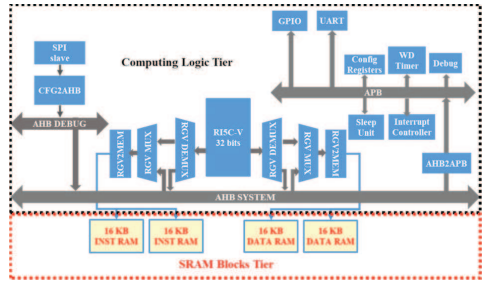



Figure 10 : RISC-V SoC architecture

## III. M3D-ADTCO RISC-V PnR Experiment

In this section, we present the full Performance, Power, Area (PPA) results of a 32 bits RISC-V micro-controller based System on Chip (SoC) implemented in 2D and in M3D using M3D-ADTCO platform.

### *A. PnR Experiment Setup*

The RI5C-V SoC relies on the RI5CY core from [11], which is optimized for Cyber Physical System (CPS) applications, and a set of peripherals. The RI5CY core is an in-order 4-stage Single Core 32 bits RISC-V micro-controller interconnected through the Advanced High performance Bus (AHB) and the Advanced Peripheral Bus (APB) with peripherals as: Serial Parallel Interface (SPI), configuration registers, , Interrupt controller, Universal Asynchronous Receiver Transmitter (UART), Timer, Watchdog, Debug unit and General Purpose Input/Output (GPIO). The RI5CY core memory is composed of 32 Kbytes each Instruction and Data organized in 2x 16Kbytes memory block. The TAP controller is not integrated in this experiment.

The corners for the physical implementation (synthesis and place and route) are the following: the setup timings are fixed in the worst case corner (0.8V - 125°C); the hold timings are fixed in the best case corner (1.0V - minus 40°C) and the typical corner (0.9V - 25°C) is used for the analyze of the power consumption results. These corners are used for both functional implementation (no DFT paths activated) mode and for and M3D-DFT mode (M3D-DFT Paths activated).

We take 5% of On Chip Variation (OCV) margin for both 2D and M3D trials and we use the same target clock frequency for both functional and test modes. Post synthesis complexity of the RI5CY platform is 36K cells equivalent to an area of 0.06 mm² and 0.2 mm² for the four SRAM memory blocks.

We define a signoff GDS as: a GDS in which the hold are fixed in best case corner with positive slack only; and that contains no DRC errors, meaning neither shorts nor layout rules violated remain at the end of the M3D PnR; and a Layout Versus Schematic (LVS) check clear. We use Mentor Graphics Calibre tool for these signoff verifications.

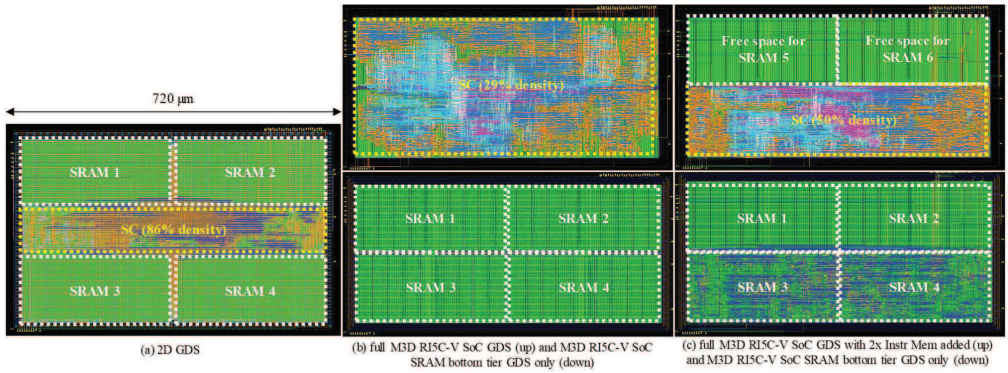



Figure 11 : 2D GDS, M3D GDS and M3D 2x instruction memory GDS

## IV. 2D AND M3D-ATDCO PPA RESULTS.

Figure 11 shows three different GDS:

(a) the 2D RI5C-V SoC GDS,

(b) *up*: the M3D RI5C-V SoC GDS,
*down*: the bottom tier layers only of the M3D RI5C-V SoC GDS emphasizing the SRAM memory blocks and their power stripes (M5_bot),

(c) *up*: the M3D RI5C-V SoC GDS with the SC fenced in the half of the area leading to spare the other half of the area for doubling the instruction memory (M3D-2),
*down*: the bottom tier layers only of the M3D-2 GDS emphasizing the SRAM memory blocks, their power stripes (M5_bot) and the bottom layers used for 3D routing.

In (a), the SRAM memory blocks are pre placed in the corners and the SC are sandwiched in between with a density up to 86%, that is the minimum footprint configuration possible (720 $\mu$m x 440 $\mu$m). In M3D, we reduce the footprint to the exact sum of SRAM memory block footprints leading to an overall area reduction of 23.61%. As a result, the SC density in the top tier decreases of 29%. From here, we can we can choose to increase the RI5C-V SoC Performance (b) by adding more inverters/buffers or to double for instance, the instruction memory capacity of the RI5C-V SoC (c).

Table 2 presents all the PPA results for 2D, M3D and M3D-2 cases in the range of 550 MHz and 625 MHz target clock frequency. For the 550 MHz target clock frequency point, that is the highest performance of the 2D RI5C-V SoC, the hold are met for the three cases. In the M3D case, we observe an increase of SC instantiated and more precisely the amount of inverters used (+15.97%), that is direct consequence of the reduction of the logic density. Thus, the Total Wire Length (TWL) increases as well (+18.75%). As a result, a slightly increase in Power consumption occurs (+4.77%) and especially regarding net switching power (+7.34%). In this case, 86000MIVs are used, essentially for the PDN-MESH and few for signal routing since there is no routing congestion at this very low SC density. Indeed, the routing engine prefers to use top BeoL layers which make sense regarding the MIV parasitics cost.

On the other hand, by fencing the logic in the half of the footprint, in order to double the instruction memory, leads to increase again the overall logic density in M3D-2 case from 29% to 50%. As a result, less inverters are needed while TWL and thus power consumption (especially the net switching power) decrease again compared to M3D and 4.6x much more MIVs (400000) used. Finally, at iso Performance and Power, M3D allows a 2x increase of instruction memory capacity compared to 2D.

However, M3D technology allows to reach a highest performance point as presented in Table 2. Indeed, a performance increase of 7.39% is feasible, with a maximum clock speed of 591 MHz. The critical path is a memory to flop path in the Arithmetic Logic Unit (ALU) of the RI5CY micro-controller; so by decreasing drastically the density, it releases free space to add extra buffers or inverters and thus the capacity to speed up this path. To sum up, M3D allows area reduction of 23.61% and a Performance increase of 7.39% compared to 2D.

Nevertheless, there is a trade off point that consists in fencing the logic in half the area to double for instance the instruction memory capacity. By doing this, as in 550 MHz target point, the density of logic increases again, limiting the buffers/inverters effect and thus a reduced speed gain compared to 2D but we observe a reduction in TWL (-16.09%) and in Power consumption (-7.66%) compared to pure M3D. Finally, this M3D-2 maximum performance point produces a 2x instruction memory capacity increase and +3.06% increased Performance compared to 2D.

In Figure 12, we plot the spreading of each routing layers for both 2D, M3D and M3D-2 for the 555 MHz point. We can see that, in the M3D case where the logic density is very low and thus there is no routing congestion, the routing engine does not use the intermediate BeoL (Mx_bot). Indeed, it reduces the amount of MIVs to its minimum, in order to focus on top tier BeoL for routing as expected knowing the extra cost of the parasitics of the MIVs. On the other hand, in M3D-2, the logic density increases again and thus routing congestions start to arise. In this case, the routing engine uses the bottom layers in order to free top tier routing tracks and thus leading to reduce the overall TWL utilization that produces a more power efficient point compared to M3D. In this case, the routing engine uses up to 415000 MIVs, which represents a density of 17291 MIV/mm$^2$.

TABLE 1 : 2D AND M3D PPA RESULTS @ 555 MHZ

| PPA Results - 555 MHz | 2D | M3D | M3D vs 2D | M3D-2 | M3D-2 vs 2D | M3D-2 vs M3D |
|---|---|---|---|---|---|---|
| Footprint (µm²) | 322560 | 246394 | -23.61% | 246394 | -23.61% | 0.00% |
| WC Perf (MHz) | 550.36 | 551.88 | 0.28% | 553.10 | 0.50% | 0.22% |
| #Buffer | 6251 | 6096 | -2.48% | 5997 | -4.06% | -1.62% |
| #Inverter | 4540 | 5265 | 15.97% | 4705 | 3.63% | -10.64% |
| #Comb. | 25814 | 28434 | 10.15% | 27916 | 8.14% | -1.82% |
| #Flops | 7855 | 7855 | - | 7855 | - | 0.00% |
| #SRAM | 4 | 4 | - | 4 | - | 0.00% |
| Total Cells | 44464 | 47654 | 7.17% | 46477 | 4.53% | -2.47% |
| Density (%) | 86% | 29% | - | 50% | -41.60% | 75.07% |
| TWL (µm) | 852015 | 1011771 | 18.75% | 796846 | -6.48% | -21.24% |
| #MIVs | 0 | 86000 | - | 400000 | - | 365.12% |
| Dynamic Power (mW) | 14.94 | 15.29 | 2.34% | 15.05 | 0.74% | -1.57% |
| Switching Power (mW) | 14.31 | 15.36 | 7.34% | 14.09 | -1.54% | -8.27% |
| Leakage (mW) | 0.31 | 0.32 | 3.23% | 0.36 | 16.13% | 12.50% |
| Total Power (mW) | 29.56 | 30.97 | 4.77% | 29.5 | -0.20% | -4.75% |

TABLE 2 : M3D AND M3D-2 PPA RESULTS @ 625 MHZ

| PPA Results - 625 MHz | M3D | M3D vs 2D | M3D-2 | M3D-2 vs 2D | M3D-2 vs M3D |
|---|---|---|---|---|---|
| Footprint (µm²) | 246394 | -23.61% | 246394 | -23.61% | 0.00% |
| WC Perf (MHz) | 591.02 | 7.39% | 567.21 | 3.06% | -4.03% |
| #Buffer | 7218 | 15.47% | 6597 | 5.54% | -8.60% |
| #Inverter | 5723 | 26.06% | 4905 | 8.04% | -14.29% |
| #Comb. | 29210 | 13.16% | 28193 | 9.22% | -3.48% |
| #Flops | 7855 | - | 7855 | - | 0.00% |
| #SRAM | 4 | - | 4 | - | 0.00% |
| Total Cells | 50010 | 12.47% | 47554 | 6.95% | -4.91% |
| Density (%) | 29% | - | 50% | -41.60% | 75.07% |
| TWL (µm) | 1036509 | 21.65% | 869779 | 2.08% | -16.09% |
| #MIVs | 86000 | - | 415000 | - | 382.56% |
| Dynamic Power (mW) | 19.74 | - | 18.58 | - | -5.88% |
| Switching Power (mW) | 19.38 | - | 17.56 | - | -9.39% |
| Leakage (mW) | 0.56 | - | 0.5 | - | -10.71% |
| Total Power (mW) | 39.68 | - | 36.64 | - | -7.66% |

## V. DISCUSSION

In this work, we have focused on a logic over memory partitioning that is in line with advanced computing requirements [4, 5]. However, some could be interested in logic on logic partitioning. M3D-ADTCO offers the capability to do logic on logic, applying exactly the method presented in this paper to the SC. In this case, a smart and automatic thermal aware partitioning has to be introduced during the PnR to forbidden the superposition of two hot spots, even if M3D thermal behavior is better than coarser grain 3D stacking technologies [12]. M3D-ADTCO is also capable of doing logic on analog/mixed signal heterogeneous application (e.g. smart sensors) since .lef and .lib files are available and stands as the the first step toward full M3D Design Platform for pure digital application.

Moreover, the PPA presented in this paper depend on the architecture and the complexity of the testcase as well as the technology node used. Indeed, we use a quite small and simple SoC testcase of 0.32 mm² and a mature node (28 nm FDSOI). Additional works could consist in exhibiting M3D-ADTCO PPA on a much more complex circuit as well as for a more advanced technology node in which BeoL parasitics become dominant and drastically affect the performance of the circuit [13].

Lastly, we have decided to look at creating space for increasing the memory capacity in the M3D-2 case, but it could have been interesting to benchmark the PPA results when adding computing logic as for instance a Floating Point Unit (FPU).

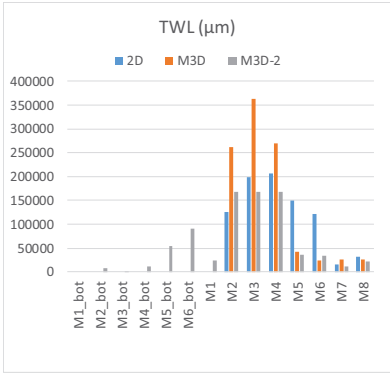



Figure 12 : 2D, M3D and M3D-2 total wire length spreading

## VI. CONCLUSION

In this paper, we have introduced M3D-ADTCO platform relaying on M3D PDKit which makes possible the utilization of any commercial 2D PnR tool to do a single M3D PnR. The combination of M3D PDKIT and M3D PnR leads to provide a signoff M3D GDS with a reduction of area of 23.61% while spreading space for doubling the instruction memory capacity compared to 2D baseline RI5C-V based SoC. Eventually, it is the first platform allowing a full architecture, design and technology co-optimization dedicated to Monolithic 3D.

## VII. ACKNOWLEDGMENT

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## REFERENCES

[1] L. Brunet, et. al., "Breakthroughs in 3D Sequential technology," in IEEE International Electron Devices Meeting (IEDM), 2018.

[2] G.Yeric,"community.arm.com/arm-research/b/articles/posts/three-dimensions-in-3dic---part-ii "

[3] G.Yeric,"community.arm.com/arm-research/b/articles/posts/three-dimensions-in-3dic---part-iii "

[4] T.F. Wu, et. al., "Hyperdimensional Computing Exploiting Carbon Nanotube FETs, Resistive RAM, and Their Monolithic 3D Integration,' in IEEE Journal of Solid State Circuits (JSSCC), 2018.

[5] Y. Yu. And N. K. Jha, "A Monolithic 3D Hybrid Architecture for Energy-Efficient Computation," in IEEE Transactions on Multi-Scale Computing Systems (TMSCS), 2018.

[6] D. Gitlin, M. Vinet , and F. Clermidy, "Cost Model for Monolithic 3D Integrated Circuits," in IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S) , 2016

[7] S. Kumar Samal, et . al., "Tier Partitioning Strategy to Mitigate BEOL Degradation and Cost Issues in Monolithic 3D ICs," in in IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2016.

[8] K. Chang, et. al., "Cascade2D: A Design-Aware Partitioning Approach to Monolithic 3D IC with 2D Commercial Tools," in IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2016.

[9] O. Billoint, et. al., "Merging PDKs to build a design environment for 3D circuits: methodology, challenges and limitations" in IEEE/ 3D Integrated Circuit Conference (3DIC), 2019.

[10] I. Jani, et. al., "Test Solutions for High Density 3D-IC Interconnects–Focus on SRAM-on-Logic Partitioning", in IEEE European Test Symposium (ETS), 2019

[11] https://www.pulp-platform.org/docs/ri5cy_user_manual.pdf.

[12] C. Lopes dos Santos et. al., "Thermal Performance of CoolCube™ Monolithic and TSV-based 3D Integration Processes" in IEEE/ 3D IC conference (3D IC), 2016.

[13] F. Clermidy et. al., "Technology scaling: the CoolCube™ paradigm" in IEEE/SOI-3D-Subthreshold Conference (S3S), 2015.