ESA Athena WFI Onboard Electronics - Distributed Control and Data Processing

Markus Plattner, Sabine Ott, Sebastian Albrecht, Jintin Tran, Christopher Mandla
Max Planck Institute for extraterrestrial Physics
Garching, Germany

Jan-Christoph Tenzer, Thomas Schanz, Samuel Pliego
Institute for Astronomy and Astrophysics - University of Tübingen
Tübingen, Germany

Denis Tcherniak
Astrophysics and Atmospheric Physics - Technical University of Denmack
Kgs. Lyngby, Denmark

Manfred Steller, Harald Jeszensky
Space Research Intitute - Austrian Academy of Sciences
Graz, Austria

Roland Ottensamer
Department of Astrophysics - University of Vienna
Vienna, Austria

Konrad Skup
Space Research Centre - Polish Academy of Science
Warsaw, Poland

Chris Thomas, Julian Thornhill
Physics and Astronomy – University of Leicester
Leicester, United Kingdom

***Abstract*— Within this paper, we describe architecture and functionality of the Wide Field Imager (WFI) control and data processing electronics. WFI is one of two scientific instruments of the next European X-ray observatory ATHENA whose development started five years ago. A conceptual design, development models and a number of technology development activities have been performed and results will be shown.**

Keywords—Athena, WFI, FPGA, Onboard Processing, Instrument Control Unit

I. ESA ATHENA AND THE WIDE FIELD IMAGER

Cosmic Vision is the program for the European Space Agency's long-term planning of science missions [1]. In 2014, ATHENA (Advanced Telescope for High ENergy Astrophysics) was selected as the second large-class mission scheduled for launch in 2031. Since then, ESA, space industry and science institutes have been developing the ATHENA spacecraft and its scientific payloads. The ATHENA spacecraft will be operated in the second Lagrangian point L2, 1.5 million kilometers from Earth in opposite direction from Sun.

The Wide Field Imager (WFI) is one of the two X-ray instruments onboard ATHENA. WFI is a camera system with a detector assembly consisting of five active pixel sensor matrices providing imaging in the energy range from 0.2 up to 15 keV. Additionally, the incoming photons are spectrally resolved with a resolution below 170 eV and their incidence time is resolved with a resolution of 5 ms resp. 80 µs [2]. Every X-ray photon within the energy range that hits the detector is called an "event", characterized by its energy, position and time. WFI will perform a full sky survey helping to answer the two key astrophysical questions of the ATHENA science theme: 1) How do black holes grow and shape the Universe? 2) How does ordinary matter assemble into the large-scale structures we see today? [3]. For that, WFI will observe various X-ray sources. Table 1 lists three exemplary observation scenarios, categorized as low, medium and high regarding the incoming photon rates focused through the ATHENA mirror to the detectors [3].

A European consortium of more than ten institutions are working together in the development of WFI. It follows a model philosophy according to ESA's phased development approach. Currently, critical technologies of WFI like the detectors, the

978-3-9819263-4-7/DATE20/©2020 EDAA

optical blocking filters and the Detector Electronics are being developed to achieve a higher technical maturity.

Table 1: Exemplary observation scenarios categorized with low, medium and high photon rate.

Category	Observation scenario	Photon rate
Low	Chandra Deep Field South	28 events/s
Medium	1/8 Crab like point source	10000 events/s
High	Crab like point source	78000 events/s

Figure 1 shows a block diagram of WFI with focus to the onboard instrument control and data processing architecture. X-ray photons enter WFI through a Filter Wheel allowing to block photons in the UV and visible range. WFI has five detectors: a detector array with 4 large detectors, 512x512 pixel each and a fast detector with 64x64 pixel. The corresponding frame rates are 200 Hz for the large and 12.5 kHz for the fast detector [4].

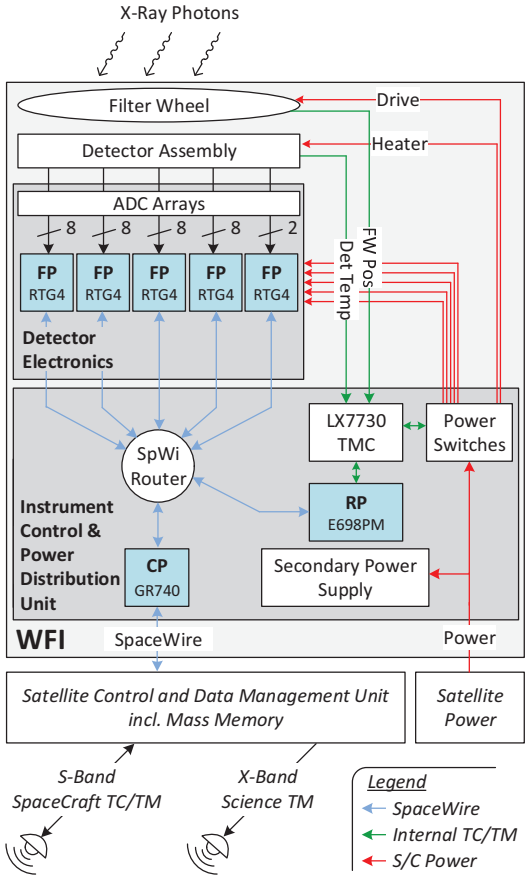

Figure 1: WFI instrument control and data processing architecture.

The output data of this Detector Assembly is digitized with ADC arrays. This yields a data stream of up to 3.65 Gbit/s [5] processed by five Frame Processors (FP) based on Microsemi RTG4 FPGAs. All of them are operated in parallel within the distributed Detector Electronics subsystem of WFI. A SpaceWire Router combines the processed data streams and forwards the resulting data with an average rate of 10 Mbit/s to the Central Processor (CP), a Cobham Gaisler GR740 [10], which is the main processor of the Instrument Control & Power Distribution Unit (ICPU). A Remote Processor (RP), E698PM from OMC technology [9] combined with a telemetry controller LX7730 from Microsemi [12], performs additional housekeeping and control tasks.

Further, the ICPU provides the interface to the Satellite Control and Data Management Unit (SCDMU) [6] and connects WFI to the Satellite Power. A Secondary Power Supply generates all required voltages in order to bias all electronics.

II. FPGA-BASED FRAME PROCESSING

A. Frame Processor Pipeline

As outlined in the previous section, the high output data rate of the Detector Array requires parallel processing. The four large detectors are read-out with 32 ADCs in parallel, 8 ADCs per large detector and another 2 ADCs for the fast detector as shown in Figure 1. The capability of parallel data processing is the reason for the implementation of FPGAs as first frame processing layer inside the WFI Detector Electronics. The flash-based Microsemi RTG4 FPGAs offer a radiation insensitivity compliant to the L2 environment with performance and resources high enough to process the entire data stream in real-time. Within the FP FPGA, a raw data processing pipeline has been implemented (see Figure 2).

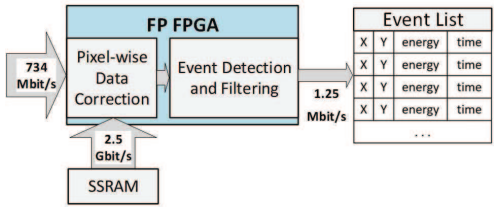

Figure 2: FPGA-based Frame Processing, here shown with one of the four large detectors.

Pixel-wise data correction includes offset subtraction, common-mode correction and bad pixel flagging. Event detection and filtering includes evaluation of energy thresholds and pattern recognition i.e. identification of neighboring events. The FP output is an event list, that includes all detected events including their position (x and y pixel coordinate), measured photon energy and photon incidence time. Table 2 summarizes the output data rate of one FP for the three exemplary observations with one large detector.

Table 2: Processed output data rate (only science data considered).

Cat.	Event list per large detector	FP output data rate on average	Data reduction
Low	60 bit	12 kbit/s	61000 x
Medium	830 bit	160 kbit/s	4500 x
High	6.3 kbit	1.25 Mbit/s	580 x

FP-based event detection and filtering reduces the data rates by three to four orders of magnitude.

For the pre-processing tasks executed by the FP, offset and noise data has to be available for each individual pixel. One of the critical development steps for the FP module was to connect large external memory with a high bandwidth to the FPGA. Table 3 summarizes the memory sizes including margin and contingency, taking into account the ESA margin philosophy, and provides values for Current Best Estimate (CBE) and the Maximum Expected Value (MEV).

Table 3: Memory estimation for FP modules.

Memory Estimation	Large Detector	Fast Detector
No. of pixels	512 x 512	64 x 64
Bit per pixel	16	16
No. of maps (CBE)	2	2
Total (CBE)	8.4 10^6 bit	0.13 10^6 bit
No of maps (MEV)	3	3
Total (MEV)	12.6 10^6 bit	0.20 10^6 bit
Margin & Contingency	50 %	50 %
Total Memory	**18.9 10^6 bit**	**0.29 10^6 bit**

Three pipelined 32 bit SSRAM components by Cobham have been selected as baseline and are connected to the FPGA in parallel. Thereby, a data rate at the memory interface of 7.7 Gbit/s can be achieved, which is approximately three times the required data rate.

In order to test the correct functionality of the FP FPGA, a programmable real-time emulator (PRE) has been developed [13]. The PRE serves as a Camera Head substitution and provides data streams to the FP, which are based on simulations of observation scenarios [7]. The digital value of each emulated pixel contains either the digitized X-ray photon energy, expected noise values, or invalid events that arise from e.g. ionizing particles that hit the detector. Figure 3 illustrates the test setup with RTG4-based FP development model, connected to PRE for performance verification. Expansion boards hold a SpaceWire interface connector and an external SSRAM memory board.

This verification concept, based on the PRE, allows operating the Frame Processing FPGA without an X-ray detector connected to it. Various observation scenarios can be simulated in a dedicated MatLab environment and the resulting data streams are transferred to the emulator and from there provided to the frame processor FPGA in real-time.

One test case was verification of the real-time capability of the FP. In order to test the worst-case scenario with regard to input data, the observation scenario labeled category "high" (see Table 1) was selected. Eight different test frames were generated that simulate this observation. These frames have periodically been repeated 12000 times and provided as input to the FP for a total test time of approximately one minute of test time. Comparison of simulated and processed data showed that hundred percent of the events contained in the emulated data stream have been identified by the Frame Processor. The Frame Processor pipeline works error free in real-time, thereby also demonstrating that the required memory bandwidth has been achieved.

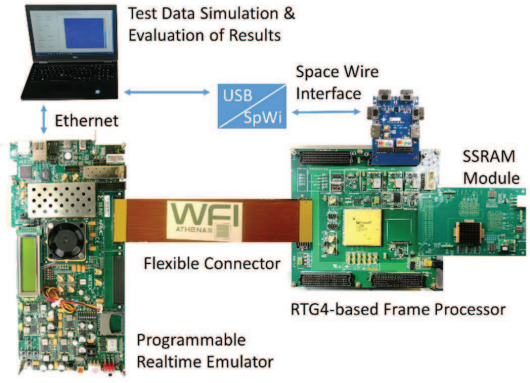

Figure 3: Frame Processor development model and RT Emulator.

B. *Softcore Evaluation*

Complementary to the development of the logic-based FP, the possibility of implementing an additional softcore processor has been investigated. Four different softcores, which are compatible to RTG4, are available: RISC-V, Cortex-M1, Leon-3, Leon-4, all being 32-bit RISC processors. The first three of them have been examined by implementation and testing in our FP breadboard (RISC-V and Leon-3 clocked at 50 MHz, Cortex-M1 clocked at 40 MHz).

The first step was a kind of benchmark testing using various algorithms. Here, two results based on AES (Advanced Encryption Standard) encryption [14] and integer arithmetic test (a repeated combination of multiplications, additions and division) are shown.

Table 4: Softcore Benchmark results.

	RISC-V	Cortex-M1	Leon-3
AES encryptions per second per MHz	26.5	23.3	28.5
Integer arithmetic runs per second per MHz	1870	1715	1626

In the benchmarks, RISC-V and Leon3 achieved the best results. An important advantage of RISC-V is that it has a free license and is officially offered and supported by the RTG4 vendor Microsemi. For this reason, further investigations have been carried out using RISC-V architecture. Table 5 lists a short characterization of the RISC-V softcore.

Table 5: RISC-V softcore for FP FPGA.

Max. Frequency for RTG4 [MHz]	63
Recourses of RTG4 [LUTs, %]	13081, 8.7%
ISA	RV32IM
Instruction Cache Size	8 KB
Data Cache Size	8 KB
Pipeline Stages	5
Bus Interfaces	AMBA,AXI,AHB

Raw-data processing of a 512x512 pixel-frame is not feasible with a softcore and a frame-rate of 200 fps. A softcore could, however, be used beneficially for non-timing critical applications which are difficult to implement in firmware. A use-case within WFI is the detector offset-map generation.

The purpose of the offset correction is to compensate deviations for any individual pixel of a 512x512 pixel array. For this reason, a so-called offset-map is calculated. Up to 256 dark frames are captured (closed Filter Wheel) before a measurement starts. During read-out of 256 frames, several pixels are illuminated by ionizing particles. To make sure that a realistic offset value can be calculated for each pixel, the five lowest and highest values of each pixel are deleted. This requires to execute a kind of sort algorithm (find min/max) on the measured values. Afterwards, the average level of each pixel is calculated and stored in an FPGA-external SSRAM (see Figure 3) as detector offset-map. A comparable approach, regarding computing effort and resources, is required for the generation of a detector noise-map.

For comparison, the functionality of offset-map generation has been implemented in the FPGA fabric and as software in the RISC-V softcore. The processor-based implementation requires approximately 6 minutes for offset-map generation running at 60 MHz. The fabric-based solution operates in real-time at 1.3 seconds. The logic resources required for fabric solution are, however, 60% of the logic required for softcore. As such, this would be lower than the resources for the softcore implementation. Nevertheless, implementing an additional scheme for noise-map generation will end at 120% or resources compared to the softcore solution. Hence, implementation of a RISC-V softcore, which would require less than 10% of the RTG4 resources could be beneficial.

Using a softcore means moving to a new abstraction layer where e.g. standard C/C++ code can be executed. This offers an easily modifiable design where short term changes of programs are possible. The main advantage, however, is to get a variety of functionality for a fixed portion of FPGA resources when using a softcore (as shown above). In the use-case described, the softcore can also do other tasks like event analyzation or housekeeping once finished with offset-map generation. Figure 4 shows the RISC-V implementation for RTG4 that has been tested for WFI.

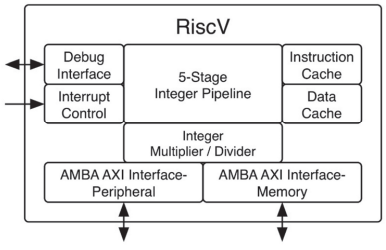

Figure 4: Block-diagram of the RISC-V implementation on RTG4.

Different components can be accessed by the connection to the 32-bit bus of the processor. The processor's subsystem can be connected to other components inside the FPGA design by the AMBA AHB/APB bus. The question if a RISC-V softcore will be implemented in the WFI FP FPGA has not been answered yet. The tradeoff between software/firmware implementation of detector maps calculation and other potential functionality is still ongoing.

III. Instrument Control & Housekeeping

A. Instrument Control

The Instrument Control and Power Distribution Unit (ICPU), is a WFI subsystem consisting of several modules. The SpaceWire router is one part of it and forwards the event lists generated by each individual FP to the Central Processor (CP). The CP merges the data streams received and performs data compression. Then, the CP forwards all science data to the SCDMU wherein it is stored in a mass memory until a ground link can be established and the data can be transferred to the ground station. The second major task of the CP is to interpret all Tele Commands (TC) received from the SCDMU and control WFI accordingly. This includes for example starting and stopping of observations, initiating WFI calibration and collecting all WFI-internal housekeeping data for status evaluation. The ICPU thereby is the main communication and power interface to the spacecraft and is responsible for distribution of spacecraft power to all subsystems by its secondary power supply and switch matrix (see also Figure 1).

B. Synchronization of Frame Processors

The five FPs send their processed data to the ICPU after each frame. The transmission time for each event list for the three observation categories is given in Table 6.

Table 6: Transmission time for the event list per FP assuming a SpaceWire bandwidth of 80 Mbps (only science data considered).

Category	Transmission time for FP event list
Low	< 1 us
Medium	10 us
High	80 us

Measured levels of bias voltages and currents add another 2 kbit per frame. In order to achieve undisturbed instrument operation, the five FPs have to be synchronized. Figure 5 shows the synchronization concept based on time-division multiplexing.

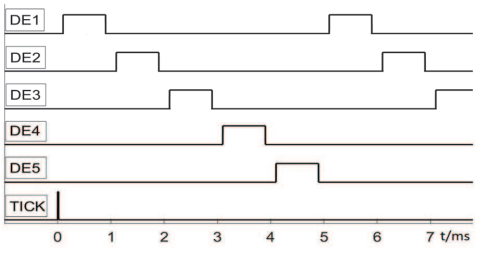

Figure 5: Synchronization of Detector Electronics data transfer to ICPU by time division multiplexing.

Each FP sends its output data with a rate of 5 ms. Since all FPs work in parallel, independent from each other, the data transfer could be mutually disturbed due to latencies, jitters or skews of the clock cycle. Eventually, these disturbances could lead to channel blocking, wherefore the WFI synchronization concept has been evaluated based on a dedicated test setup.

Two RTG4 evaluation boards have been used to measure the deviation of their internal clock rate under laboratory conditions. Due to limitations of available test hardware a lower data link rate at 40% was used for this test, wherefore the expected delay of two time slots for the same DE is 12.5 ms instead of 5 ms. Figure 6 shows the measurement results.

The average delay of two consecutive transmissions is offset by 0.35 ms (12.15 ms instead of 12.5 ms expected). Further, the results reveal that the clock rate errors in the range of 10 percent appear randomly because the FPGA internal clock circuitry is not stable enough. The outcome of these tests is to use FPGA-external oscillators with a higher stability in the area of 1500 ppb. Further, a SpaceWire based synchronization scheme via Time-Code broadcasting will be implemented with a synchronization period below one minute [8].

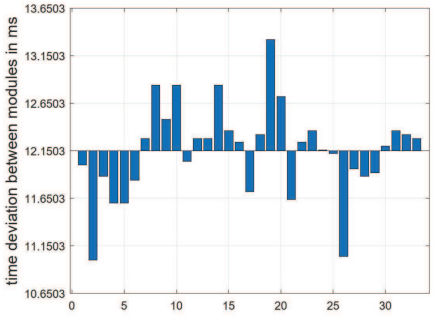

Figure 6: Deviation of DE synchronization due to clock jitter.

C. Housekeeping

In addition to science data processing and merging, the ICPU also performs housekeeping (HK). Since the WFI instrument can only be operated remotely, measurement and transfer of HK data, i.e. all relevant signal levels within WFI, are monitored and transferred to ground. This provides the mission operator with a good knowledge about the status of the instruments and thereby allows to perform on-ground assessment of the science data integrity. If, for example, the detector bias voltage levels change due to radiation effects or aging, the event data like measured photon energy can be different. The exact knowledge of bias voltages allows to identify the measurement error or even gives the possibility to recalibrate data on-ground to improve data performance.

Figure 7 shows the distributed HK concept of WFI. HK data is basically collected within each WFI subsystem, either controlled by one of the three processors CP, FP, RP or by a dedicated HK circuit as shown in Figure 8.

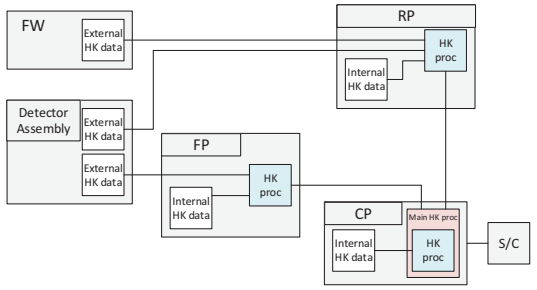

Figure 7: Distributed HK acquisition.

The Remote Processor (RP) performs a bunch of housekeeping and instrument control tasks. The RPs functionality includes switching on and off the DE units, control of the Filter Wheel position, control of detector temperature and read-out of corresponding housekeeping. The RP, however, is fully commanded by the CP.

One of the basic HK circuits used in WFI is depicted in Figure 8. A multiplexing ADC (12 bit resolution) measures voltages and currents via shunt resistors and differential amplifiers. The measurement values are provided via the ADC output interface, in this example a serial port interface. This circuit is implemented several times within WFI for any kind of voltage and current monitoring.

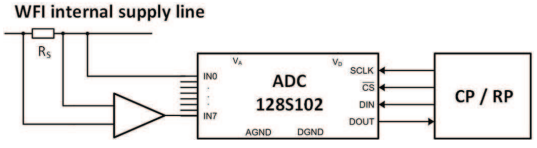

Figure 8: Multiplexing ADC for HK Data Acquisition.

Another implementation for HK is based on the telemetry controller LX7730 [12]. This component allows to measure 64 channels of HK data. Further, it provides current sources for biasing e.g. temperature sensors, bi-level inputs and internal ADC and DAC for input digitization and analog output supply. This circuit is used for detector temperature monitoring and sensing of Filter Wheel position via Hall sensor read-out.

IV. Conclusion and Outlook

The Wide Field Imager payload instrument will be the next generation X-ray camera system for the next generation X-ray observatory ATHENA. Its large detector array has Mega-pixel size and frame rates of 200 fps. The development of its onboard electronics is a challenging task requiring distribution and parallelization of processing and instrument control. In this paper, we have summarized the main part of the achievements regarding WFI control and data processing that has been performed by the instrument consortium up to now. The architecture has proven to be sound by successfully evaluating several test and analysis results.

One of the next steps in WFI development is the detailed definition of the system including a consolidation of technical and performance requirements. This, together with first test results of the electronics operated with flight-like detectors will pave the way for the next phase, wherein the engineering model of the instrument will be developed in hardware and software and the full performance shall be demonstrated.

REFERENCES

[1] ESA Science & Technology Homepage, https://sci.esa.int/web/athena

[2] The Wide Field Imager for the ATHENA X-Ray Observatory, http://www.mpe.mpg.de/ATHENA-WFI

[3] The Athena X-ray Observatory: Community Support Portal, https://www.the-athena-x-ray-observatory.eu

[4] Meidinger N. et al.: The Wide Field Imager Instrument for Athena, SPIE Astronomical Telescopes and Instrumentation, Edinburgh, June 2016.

[5] Plattner M. et al.: WFI Electronics and On-Board Data Processing, Proceedings of Space Telescopes and Instrumentation 2016, Vol. 9905.

[6] Eickhoff J., Onboard Computers, Onboard Software and Satellite Operations, Springer Series in Aerospace Technology, 2012.

[7] Ott S. et. al: New evaluation concept of the Athena WFI camera system by emulation of X-ray DEPFET detectors, Journal of Instrumentation, Vol. 11, 2016.

[8] S. Parkes. „The Operation and Uses of the SpaceWire Time-Code," Space Systems Research Group, University of Dundee, www.spacewire.esa.int

[9] OCE Technology, E698PM Radiation-hardened SPARC V8 Quadcore Processor SoC, product brochure, http://ocetechnology.com

[10] Cobham/Gaisler, GR740 Quad Core LEON4 SPARC V8 Processor, Preliminary Data Sheet and User's Manual, 2018.

[11] Microsemi/Microchip, RTG4 FPGA Datasheet, August 2018.

[12] Microsemi/Microchip, LX7730 Datasheet, April 2018.

[13] Ott S.: Detector Emulation for Athena WFI Performance Verification, PhD thesis 2018.

[14] Quinn H. et al., "Using Benchmarks for Radiation Testing of Microprocessors and FPGAs," IEEE Transactions on Nuclear Science, vol. 62, pp. 2547–2554, 2015.