Testing Through Silicon Vias in Power Distribution Network of 3D-IC with Manufacturing Variability Cancellation

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***Abstract*—To detect open defects of power TSVs (Through Silicon Vias) in PDNs (Power Distribution Networks) of stacked 3D-ICs, a method was proposed which measures resistances between power micro-bumps connected to PDN and detects defects of TSVs by changes of the resistances. It suffers from manufacturing variabilities and must place one micro-bump directly under each TSV (*direct-type* placement style) to maximize its diagnostic performance, but the performance was not enough for practical applications. A variability cancellation method was also devised to improve the diagnostic performance. In this paper, a novel *middle-type* placement style is proposed which places one micro-bump between each pair of TSVs. Experimental simulations using a 3D-IC example show that the diagnostic performances of both the direct-type and the middle-type examples are improved by the variability cancellation and reach the practical level. The middle-type example outperforms the direct-type example in terms of number of micro-bumps and number of measurements.**

***Index Terms*—three dimensional integrated circuits, design for testability, through silicon via, micro-bump, open defect, manufacturing variability**

I. Introduction

Power distribution networks (PDNs) in integrated circuits are getting more complex due to low power techniques such as power gating and DVFS (Dynamic Voltage and Frequency Scaling) and heterogeneous integration. That raises demand for testing PDN as a part of shipment test. A method was proposed to measure power voltages of different points of the PDNs by on-chip monitor circuits for testing PDNs in multi-die ICs [1]. The monitor circuit measures periods of a ring oscillator and they are transformed to voltages where temperature dependence and process variation are taken into account. But the method has several disadvantages. First, it increases die area by adding the monitor circuits. Second, it is not clear that the 3D-IC under test should run which function during the power voltage measurements especially when its circuits have many functional modes. In general, the function which consumes power the most is selected, but it is not guaranteed that it causes the maximum voltage drops at the monitored points. Furthermore, the test method is a functional test and its test coverage over defects cannot be known.

Based on structural test approach, a method was proposed to detect open defects of TSVs which connect PDNs in different dies of a 3D-IC [2]. The method places a micro-bump (μbump) directly under each TSV and measures resistances between pairs of μbumps. One of the issues in practical application of the method is that it needs to place a μbump exactly under each TSV since its diagnostic performance is getting worse rapidly when the distance between bump and TSV is increased. Furthermore the method suffers from manufacturing variabilities and its diagnostic performance is not enough for practical applications (i.e. too much false diagnoses). To overcome the issues, variability cancellation method was proposed afterwards which cancels manufacturing variabilities and improves diagnostic performance of the above method [3]. But the performance of the cancellation method is only evaluated by testing 13 TSVs while 3D-IC under test has 70 TSVs in [3].

In this paper, a novel middle-type μbump placement style is proposed. Compared to the conventional direct-type placement style, the proposed middle-type can reduce number of μbumps and number of resistance measurements while maintaining its diagnostic performance to practical level. Performance evaluation of the cancellation method is conducted by testing all 70 TSVs in a 3D-IC example.

II. Test Method of TSV Open Defects in PDN

In this section, testing method proposed in [2] is reviewed. Fig. 1 is a cross-sectional view of PDN in an example 3D-IC. Two VDD distribution networks in the known good dies (KGDs) are connected by 13 TSVs under which 13 μbumps are attached. It is assumed that the μbumps are not shorted in the package and resistance between bumps can be measured at package pins. When TSV1_7 has an open defect, resistance between μbump1_7 and μbump1_13 will change large enough to detect from its defect-free value while resistance between μbump1_8 and μbump1_13 will be almost unchanged. The method 1) places a μbump directly under each TSV in PDN,

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Fig. 1. Cross section of power distribution network in 3D-IC

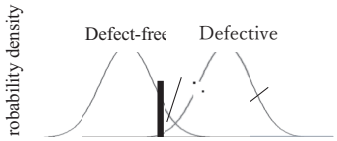

Fig. 2. Probability distribution of resistance between a μbump pair

2) finds a μbump pair for each TSV which can detect its open defect with enough diagnostic performance, 3) determine the threshold resistance for each TSV considering defect coverage and yield loss, 4) measures resistances between the μbump pairs to detect open defects of all TSVs and 5) diagnoses as defective if one of the resistances exceeds its threshold.

A. Measurement Point Selection

Even though temperature of devices under test can be controlled to be constant, resistance between the selected μbump pair is different from device to device due to the manufacturing process variation. The probability distribution of the resistance will change when a TSV has an open defect compared to defect-free case as shown in Fig. 2. When the measured resistance is above the threshold, the device is rejected as a defect one. When the two probability distributions overlap with each other as shown in Fig. 2, a diagnosis falls into one of the four cases shown in Fig. 3. For example, the case when a defective device is rejected by the test is called *true rejection*, and the number of such devices is denoted by *TR*. Here we define total number of defective devices $D = TR + FA$, total number of defect-free devices $DF = FR + TA$ and the following four test metrics.

$$\text{true rejection rate} \quad TRR = TR/D \tag{1}$$

$$\text{false acceptance rate} \quad FAR = FA/D \tag{2}$$

$$\text{true acceptance rate} \quad TAR = TA/DF \tag{3}$$

$$\text{false rejection rate} \quad FRR = FR/DF \tag{4}$$

Although we can control trade-off between *FAR* and *FRR* by changing the threshold, we have to find better μbump pair with the two probability distributions apart from each other to reduce the both false rate *FAR* and *FRR* simultaneously.

Running Monte Carlo analysis of circuit simulation tools, we can predict the two probability distributions as shown in Fig. 2. Several diagnostic performance metrics are proposed to evaluate the two probability distributions derived from simulations [4]. Using one of these measures, diagnostic performances of all μbump pairs are evaluated and the best one is selected to detect the specified TSV open defect. This process is repeated for all TSVs.

	Defective	Defect-free
Accept	(TR)	(FR)
	False acceptance (FA)	True acceptance (TA)

Fig. 3. Confusion matrix.

B. Threshold Determination

We have to determine a threshold for resistance between each μbump pair selected above to judge rejection or acceptance. Yield loss (Y_L) and fault coverage (F) defined in [5] change depending on the threshold and there is a trade-off between the two.

For a given target Y_L, the threshold R_i^{TH} for i-th TSV can be derived by the following equation [2], [3]:

$$R_i^{TH} = \text{norminv}(\sqrt[n]{1-Y_L}, \mu_i^{DF}, \sigma_i^{DF}) \tag{5}$$

where $\text{norminv}(x, \mu, \sigma)$ is the normal inverse cumulative distribution function with mean μ and standard deviation σ, n is the number of TSVs, μ_i^{DF} and σ_i^{DF} are the mean and standard deviation of the defect-free probability distribution of the measured resistance for i-th TSV, respectively.

From the thresholds, true rejection rate TRR_i for each i-th TSV can be derived by the following equation:

$$TRR_i = 1 - \text{normdist}(R_i^{TH}, \mu_i^D, \sigma_i^D) \tag{6}$$

where $\text{normdist}(x, \mu, \sigma)$ is the normal cumulative distribution function with mean μ and standard deviation σ evaluated at x, μ_i^D and σ_i^D are the mean and standard deviation of the resistance distribution when an open defect occurred at i-th TSV, respectively. Fault coverage F can be approximated by the following equation when all TSVs are tested and the probabilities of defect occurring at TSVs are equal and less than 0.1 [2], [3].

$$F \approx \frac{\sum_{i=1}^{n} TRR_i}{n} \tag{7}$$

III. Manufacturing Variability Cancellation

In this paper, relative mean difference RMD defined by the following equation is used as a diagnostic performance metric (larger is better):

$$RMD = (\mu_2 - \mu_1)/(\sigma_1 + \sigma_2) \tag{8}$$

where μ_1 and σ_1 are mean and standard deviation of measured resistances in defect-free case, μ_2 and σ_2 are mean and standard deviation of measured resistances in defective case. RMD should be greater than 3 for practical applications because we can find a threshold T which fulfills both conditions $\mu_1 + 3\sigma_1 < T$ and $T < \mu_2 - 3\sigma_2$ simultaneously. RMD can be increased by increasing mean difference $MD = \mu_2 - \mu_1$ or by reducing σ_1 and σ_2 of resistance variabilities caused by manufacturing variabilities. To improve diagnostic performance of the method explained in the previous section, variability cancellation method is proposed in [3]. Consider more than three TSVs and μbumps are in line as shown in Figs. 1 and

4. Hereafter, the resistance between two μbumps a and b is denoted by $R(a, b)$.

When one line connecting two μbumps d_1, d_2 and another line connecting two μbumps c_1, c_2 overlap with each other, it is considered that the variation of $R(d_1, d_2)$ and the variation of $R(c_1, c_2)$ are strongly correlated. For example, the correlation coefficient of $R(1\_7, 1\_13)$ and $R(1\_8, 1\_13)$ in Fig. 1 is 0.964 which is close to 1. For a given μbump pair of detection resistance R_d, the proposed method finds another μbump pair of the cancellation resistance R_c which has the following two properties.

1) correlation coefficient between R_d and R_c is close to 1
2) mean difference MD of R_c is negligible compared to that of R_d

The method measures R_c in addition to R_d and diagnoses by $R_{\text{diff}} = R_d - aR_c$ instead of R_d, where a is derived by regression analysis to approximate $R_d \approx aR_c + b$ in defect-free case. For example, the diagnostic performance of the detection resistance $R_d = R(1\_7, 1\_13)$ is $RMD = 2.07$. Using the cancellation resistance $R_c = R(1\_8, 1\_13)$, the diagnostic performance of R_{diff} is $RMD = 6.43$, where $a = 0.995$ [3].

IV. Proposed Middle-Type Micro-Bump Placement

Without the variability cancellation (VC) method, since the diagnostic performance is getting worse rapidly when the distance between bump and TSV is increased, a μbump is placed exactly under each TSV as shown Figs. 1 and 4 (called *direct-type* μbump placement style) [3]. With the help of VC, μbumps can be placed under the middle of two neighboring TSVs. *Middle-type* μbump placement style is derived by assigning only one μbump for two TSVs as shown in Fig. 5.

The following measurement point selection rule is applied to μbumps in each line. Detection resistance $R_d = R(d_1, d_2)$ and cancellation resistance $R_c = R(c_1, c_2)$ are selected as following rules for both direct-type and middle-type.

- d_1 is the nearest μbump to the TSV to be tested.
- d_2 is the farthest μbump from d_1 in the line.
- c_1 is the second nearest μbump to the TSV to be tested
- c_2 is the same μbump as d_2

The above rule is derived by simulations in the next section. The measurement points determined by the above rule do not always offer the best diagnostic performance, but always offer near the best diagnostic performance.

V. Simulation Results

A. Physical Structures and Models

Experimental simulations are conducted for a 3D-IC with two dies. There are many power nets such as GND and VDD in general, only one of the nets VDD is considered here. Both two dies are 13mm square and have on-chip PDN with the regular mesh structure as shown in Fig. 6. The mesh consists of two metal layers M6 (horizontal) and M7 (vertical). Cross-sectional dimensions of the wires are the same in the two layers. The mean width $\mu_W = 3\ (\mu m)$ and relative standard deviation of the width $\sigma_W/\mu_W = 5\%$. The mean thickness $\mu_T = 1\ (\mu m)$ and relative standard deviation of the thickness $\sigma_T/\mu_T = 5\%$. Resistance of a wire segment with length l, width W and thickness T is calculated by $R_{\text{wire}} = \rho \cdot l/(W \cdot T)$, where $\rho = 1.68 \times 10^{-8}(\Omega m)$ is the resistivity of Cu. W and T are constant within a layer, and are fluctuated independently with normal distribution between different layers. Resistances of vias between M6 and M7 are ignored in the experiment.

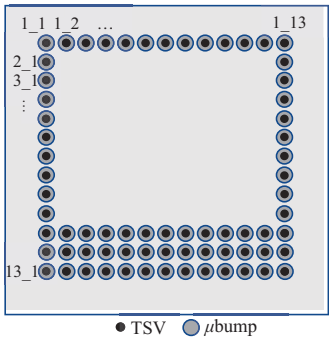

Fig. 4. Locations of TSVs and bumps in direct-type μbump placement style.

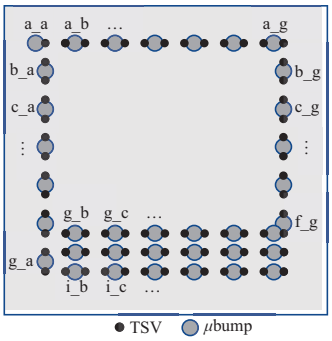

Fig. 5. Locations of TSVs and bumps in middle-type μbump placement style.

As an example of direct-type μbump placement style, 70 TSVs and 70 μbumps are placed as shown in Fig. 4. Their places are described as ⟨*row number*⟩_⟨*column number*⟩ as 1_13. TSVs are in cylindrical form and their mean radius $\mu_r = 1\ (\mu m)$ and relative standard deviation of the radius $\sigma_r/\mu_r = 5\%$. Fluctuation of their length $l = 100\ (\mu m)$ is ignored in the experiment. Resistance of a TSV is given by $R_{\text{TSV}} = \rho \cdot l/(\pi r^2)$, where $\rho = 1.68 \times 10^{-8}(\Omega m)$. Radius r is fluctuated independently for each TSV. Only open defect is considered among TSV defects and its resistance $R_{\text{open}} = 10^{12}(\Omega)$ when open defect occurs. Resistances of μbumps are ignored in the experiment.

As an example of middle-type μbump placement style, 36 μbumps are placed as shown in Fig. 5, where 70 TSVs are placed exactly at the same positions as the direct-type example shown in Fig. 4. The places of the μbump are described as ⟨*row alphabet*⟩_⟨*column alphabet*⟩ as a_g.

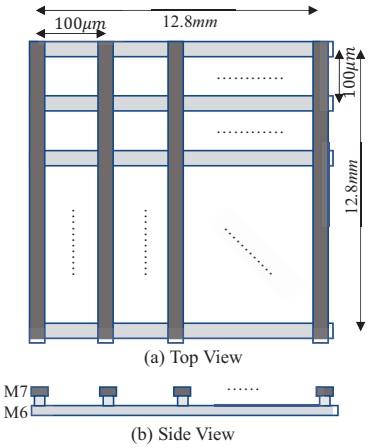

Fig. 6. Power grid dimensions.

TABLE I
DIAGNOSTIC PERFORMANCE OF THE DIRECT-TYPE EXAMPLE.

open TSV		1_1	1_2	1_3	···	1_13
without VC	d_1	1_1	1_2	1_3	···	1_13
	d_2	1_3	1_4	1_5	···	1_11
	RMD	2.51	2.31	2.25	···	2.51
with VC	d_1	1_1	1_2	1_3	···	1_13
	d_2	1_13	1_13	1_13	···	1_1
	c_1	1_2	1_3	1_4	···	1_12
	c_2	1_13	1_13	1_13	···	1_1
	RMD	6.88	6.68	6.58	···	6.88

TABLE II
DIAGNOSTIC PERFORMANCE OF THE MIDDLE-TYPE EXAMPLE.

open TSV		1_1	1_2	1_3	···	1_13
without VC	d_1	a_a	a_b	a_b	···	a_g
	d_2	a_e	a_e	a_f	···	a_d
	RMD	0.351	0.205	0.199	···	0.257
with VC	d_1	a_a	a_b	a_b	···	a_g
	d_2	a_g	a_g	a_g	···	a_a
	c_1	a_b	a_c	a_c	···	a_f
	c_2	a_g	a_g	a_g	···	a_a
	RMD	6.60	4.41	3.92	···	4.98

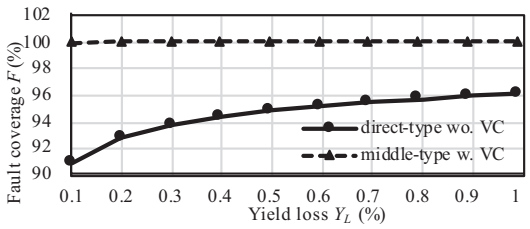

Fig. 7. Trade-off between yield loss and fault coverage of the direct-type and the middle-type examples.

TABLE III
COMPARISON OF THE μBUMP PLACEMENT STYLES

Style	var. cancel.	# μbump	# Meas.	F [a]
direct-type	without	70	58	90.864%
	with	70	82	99.992%
middle-type	with	36	48	99.984%

[a] Fault coverage when yield loss $Y_L = 0.1\%$.

B. Analysis Method

Resistance between a pair of μbumps is calculated by operating point analysis of a circuit simulator. One of the pair is connected to a grounded current source with 1A, and another μbumps is connected to the ground. Then the voltage across the pair is its resistance. To get the probability distribution of the measured resistance considering manufacturing variabilities, Monte Carlo analysis is performed for each TSV open defect in addition to defect-free case. The netlists are manually created and each netlist contains 65,606 resistors and 33,281 nodes. The resistor counts are the same for both the direct-type and the middle-type examples because resistances of μbumps are ignored. Number of samples generated by the Monte Carlo with Latin Hypercube sampling is 3,000. It takes 3,819.9 sec by modified spice3 run on MacBook Pro (Intel Core i5 2.7GHz, 8GB 1867MHz DDR3).

C. Analysis Results

The diagnostic performance of the direct-type example is shown in Table I. For each TSV in the upper horizontal line, performance metrics *RMD* are calculated with and without the variability cancellation (VC) method. The diagnostic performance of the middle-type example is shown in Table II.

Trade-off curves (fault coverage F vs. yield loss Y_L) for testing 70 TSVs are plotted in Fig. 7. The curve of the direct-type with VC is not plotted because its F is nearly the same as that of the middle-type with VC. The middle-type without VC is not plotted too because its diagnostic performance is not practical. The direct-type and the middle-type examples are compared in terms of number of μbumps, number of resistance measurements and fault coverage in Table III.

VI. CONCLUSIONS

With VC, the diagnostic performances of the both direct-type and middle-type μbump placement examples are improved to practically viable level, i.e. $RMD > 3$. The proposed middle-type example outperforms the direct-type one with respect to number of μbumps and number of measurements.

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