# Impact of NBTI Aging on Self-Heating in Nanowire FET

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***Abstract*—This is the first work that investigates the impact of Negative Bias Temperature Instability (NBTI) on the Self-Heating (SH) phenomenon in Silicon Nanowire Field-Effect Transistors (SiNW-FETs). We investigate the *individual* as well as *joint* impact of NBTI and SH on pSiNW-FETs and demonstrate that NBTI-induced traps mitigate SH effects due to reduced current densities. Our Technology CAD (TCAD)-based SiNW-FET device is calibrated against experimental data. It accounts for thermodynamic and hydrodynamic effects in 3-D nano structures for accurate modeling of carrier transport mechanisms. Our analysis focuses on how lattice temperature, thermal resistance and thermal capacitance of pSiNW-FETs are affected due to NBTI, demonstrating that accurate self-heating modeling necessitates considering the effects that NBTI aging has over time. Hence, NBTI and SH effects need to be *jointly* and *not individually* modeled. Our evaluation shows that an individual modeling of NBTI and SH effects leads to a noticeable overestimation of the overall induced delay increase in circuits due to the impact of NBTI traps on SH mitigation. Hence, it is necessary to model NBTI and SH effects jointly in order to estimate efficient (i.e. small, yet sufficient) timing guardbands that protect circuits against timing violations, which will occur at runtime due to delay increases induced by aging and self-heating.**

***Index Terms*—Self-heating, NBTI, interface traps, nanowire**

## I. Introduction

SiNW FET is one of the promising solutions to continue technology scaling due to its effective gate control, that suppresses short-channel effects, good transport properties, higher $I_{ON}/I_{OFF}$ ratio and CMOS compatibility [1], [2]. However, the nano-scaled dimensions of SiNW FET result in an ever-increasing power density due to the enhanced current drivability [3], [4]. Therefore, SiNW FETs suffer from inevitable degradations caused by electro-thermal (ET) effects like self-heating (SH) – especially at the 14nm node and below. This is due to limited silicon volume for heat dissipation during operation and the low thermal conductivity of gate oxide materials along with the geometrical confinement of the device nano structure [5], [6]. The heat transport in the nanowire channel is in quasi-1-D because the current flows along the channel from drain to source in one-dimension due to the very small diameter and channel length [3]. The key mechanism behind SH is attributed to carrier-phonon interaction in the high-electric-field region near the drain-to-channel junction. As lattice temperature increases, more carrier-phonon scattering occurs, leading to reductions in the mean free path (MFP) of carriers. SH degrades the performance of n-type and p-type transistors in terms of ON currents due to varied drifts in the electrical characteristics like transconductance ($g_m$), saturation velocity, etc. [6]–[8]. In addition, excessive generated heat within nanowire exacerbates the Hot Carrier Injection (HCI) near the drain area leading to reliability problems [9]. Additionally, leakage power exponential increases at elevated temperatures, which is unaffordable in many (like embedded) systems. In fact, each of sub-threshold leakage, reverse bias p-n junction leakage and gate leakage directly increase when the lattice temperature is higher [10]. It is noteworthy that SH still strongly affects the leakage power even though SH itself will be negligible during the OFF phase of switching (i.e. when $|V_g|<V_T$)[1] [11]. This is because excessive generated heat by SH during the ON phase (i.e. when $|V_g|>V_T$) propagates to the OFF phase and thus strongly affects the leakage power – this holds even more in current technologies because thermal time constant of transistor is typically larger than the switching period of digital circuits [4], [12] and thus insufficient timing for heat dissipation is available during the OFF phase [11].

In summary, SH reduces the performance [6], degrades the reliability [9] and increases the leakage power [11]. Therefore, there is an ever-increasing need to accurately investigate SH to understand how the Figure-of-Merit of nanowires will be affected from time-0 until the end of lifetime (EOL).

**NBTI Aging:** On the other hand, NBTI remains as a key concern for pMOS devices, whereas Positive BTI became negligible for nMOS, as Intel demosntrates [13]. NBTI leads, over time, to an increase in the threshold voltage ($V_T$) of transistor as well as a reduction in the carrier mobility ($\mu$). Both degradations (i.e. $V_T$ increase and $\mu$ reduction) lead to lowering the ON current of transistors and thus degrading their performance [14]. The underlying mechanism behind NBTI is due to the uncorrelated contributions of interface trap generation ($\Delta N_{it}$), trapping in the pre-existing defects ($\Delta N_{HT}$) inside the dielectric and trapping in bulk insulator traps ($\Delta N_{OT}$) [15]. $\Delta N_{OT}$ is significant only under harsh stress conditions (i.e. very high voltage and temperature stresses). In addition, the contribution of $\Delta N_{HT}$ is often negligible in well-optimized devices [15]. Therefore, under typical operating conditions, the overall NBTI degradation is dominated by interface traps [15].

**Impact of reductions in transistor ON current:** The sustainable frequency of a circuit is dictated by the maximum delay of the critical path. The latter is governed by the propagation delay of standard cells that form the critical path. The propagation delay of any cell, in turn, is inversely proportional to the drive current (ON current, $I_{ON}$) that its constituent transistors provide. Therefore, reductions in the ON current of transistors due to SH and/or NBTI effects will directly enlarge the critical path delay, leading to timing violations in the circuit due to the unsustainable clock frequency. To

[1]In the OFF phase, the drain current itself is extremely small and thus SH will be negligible due to the very low current densities.

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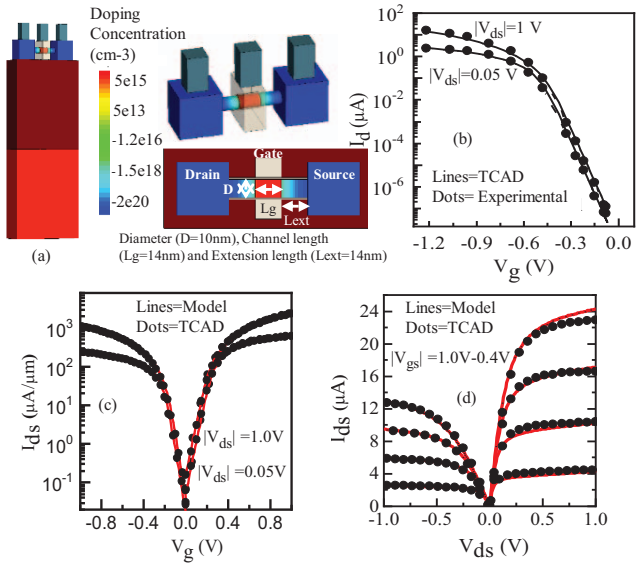


Fig. 1: (a) shows the pSiNW FET with doping profile in 3D structure and 2D cross sectional views. (b) $I_d$-$V_g$ (linear and saturation operation modes) comparisons of TCAD simulations with reported industrial data [1]. (c and d) show the validation of our developed Verilog-A compact model [16] (used within SPICE simulations) against TCAD data for pSiNW and nSiNW FETs in the case of (c) $I_d$-$V_g$ at high and low $V_{ds}$ and (d) $I_d$-$V_{ds}$ for various $V_{gs}$.

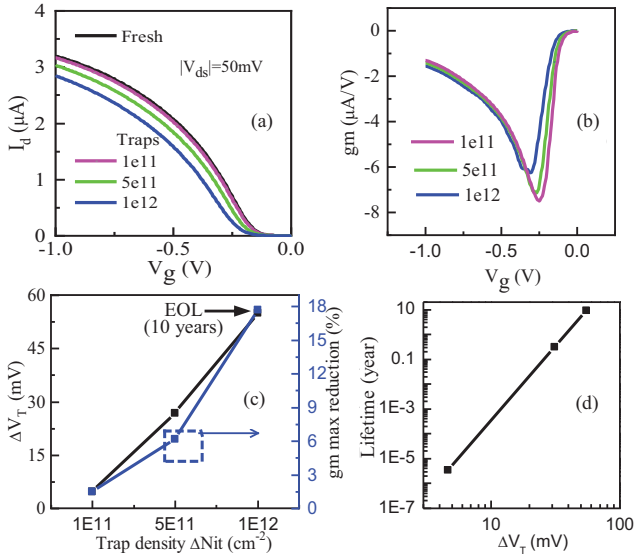


Fig. 2: (a) Shows the impact of varied NBTI-induced interface traps ($\Delta N_{it}$) on $I_d$-$V_g$ characteristics (at low $V_{ds}$) without self-heating. (b) $g_m$-$V_g$ analysis indicates the degradation in carrier mobility with the increase in trap density. (c) shows the threshold voltage shift ($\Delta V_T$) and relative $g_m$ reduction due to NBTI. $\Delta V_T$ is up to 55mV at the EOL (10 years), and maximum $g_m$ reduction is up to 18%. (d) shows the relation between $\Delta V_T$ and lifetime.

protect circuits during runtime against such timing violations, designers typically employ a timing guardband (i.e. an additional time slack) on top of the critical path delay in which any delay increase, caused by SH and/or NBTI, will be overcome. Including a timing guardband results in performance losses. *Hence it is necessary to accurately estimate the small, yet sufficient timing guardband in order to increase the efficiency.*

**Our key contributions within this work are as follows:**

(1) We investigate the *individual* impact of each NBTI and SH on the electrical characteristics of pSiNW FETs as well as the *joint* impact of them. In addition, we explore the impact of NBTI on mitigating SH effects demonstrating that NBTI- and SH- induced degradations should be studied and modeled *jointly* and not individually for accurate analysis.

(2) Electro-Thermal simulations are performed for the fresh device (i.e. in the absence of NBTI) and under the effects of interface traps at varied densities (representing induced degradations at different time steps from fresh to EOL). The key device parameters like $V_T$, $g_m$, $I_{ON}$, lattice temperature ($T_L$) and thermal resistance ($R_{th}$) are then analyzed to investigate the impact of NBTI on SH effects from fresh to EOL. For a more comprehensive analysis, we study devices with 1-wire and 2-wires, exploring how SH effects become much larger in multi-wire devices and how NBTI also affects them.

(3) The thermal capacitance ($C_{th}$) is also analyzed under different thermal time constants ($\tau_{th}$) and then the impact of SH on the maximum lattice temperature is explored for a wide range of switching frequencies in the fresh and EOL scenarios.

(4) We finally quantify the impact of modeling SH and NBTI effects *individually* instead of *jointly* on overestimating the overall delay increase in circuits for single-wire and multi-wire devices, demonstrating the necessity of a joint modeling for accurate timing guardband estimations.

## II. Our TCAD Setup for Self-Healing and NBTI Aging Analysis

The 3-D device simulations of nanowire are carried out using Synopsys TCAD tools. The pSiNW FET TCAD device is well calibrated with industrial published data [1]. Fig 1(a) shows the 3D structure of pSiNW FET along with the device calibration in which the I-V characteristics for the linear and saturation operation modes are compared to the reported experimental data (see Fig. 1(b)). The reported data is for a nanowire device with a channel length of $L_g$=30nm and oxide thickness of $t_{ox}$=2nm. After calibrations, the device was scaled down to lower dimensions ($L_g$=14nm, $t_{ox}$=1nm) according to the state of the art [2] for further device simulation and analysis. In addition, Fig. 1(c and d) demonstrate the validation of our developed Verilog-A compact model [16] (used within Synopsys HSPICE simulations) against the TCAD data for pSiNW FET and nSiNW FET in the case of $I_d$-$V_g$ at high and low $V_{ds}$ (c) and $I_d$-$V_{ds}$ for various $V_{gs}$ (d).

**Modeling SH effects in TCAD:** The drift-diffusion (DD) model with proper corrections for mobility and saturation velocity is used for device analysis in the absence of SH effects. Thermodynamic (TD) and hydrodynamic (HD) carrier transport models are jointly considered in the electro-thermal simulations for accurate SH analysis. On the one hand, the HD model simulates the electro-thermal aspects of carrier transport with quantitative estimates of carrier temperature profile. The TD model, on the other hand, solves lattice heat flow equations along with the DD model in order to obtain the lattice temperature ($T_L$) variations across the device. The Philips mobility together with high-field saturation is used to model carrier mobility. In all performed simulations, the ambient temperature of 300K has been assumed.

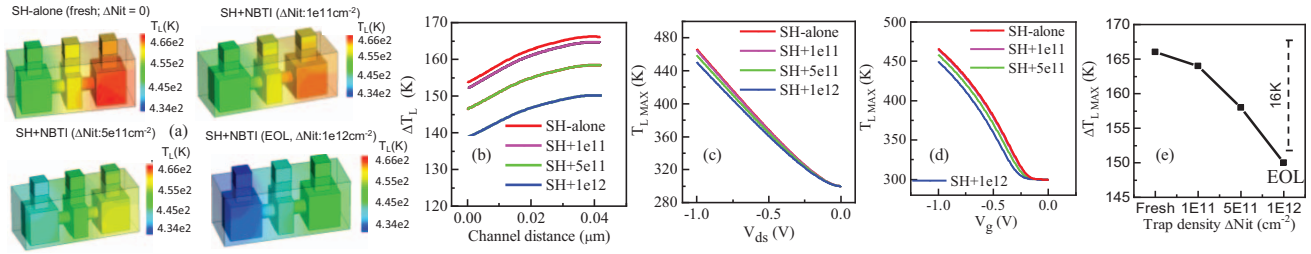


Fig. 3: (a) shows the thermal profile of pSiNW FET device due to SH effects with and without NBTI aging. As trap density ($\Delta N_{it}$) increases (i.e. higher NBTI), the impact of SH decreases (e.g., fresh case compared to EOL at $\Delta N_{it} = 1e12\text{cm}^{-2}$). (b) Increase in the lattice temperature $\Delta T_L$ along the channel at $|V_{ds}| = 1\text{V}$. (c, d) show the maximum lattice temperature ($T_{LMax}$) with applied gate and drain voltages, respectively, for the case of fresh (i.e. SH-alone) and SH+NBTI (under varied $\Delta N_{it}$). (e) shows $\Delta T_{LMax}$ from fresh to EOL. $\Delta T_{LMax}$ decreases by up to $\sim$16K under the influence of $\Delta N_{it} = 1e12\text{cm}^{-2}$.

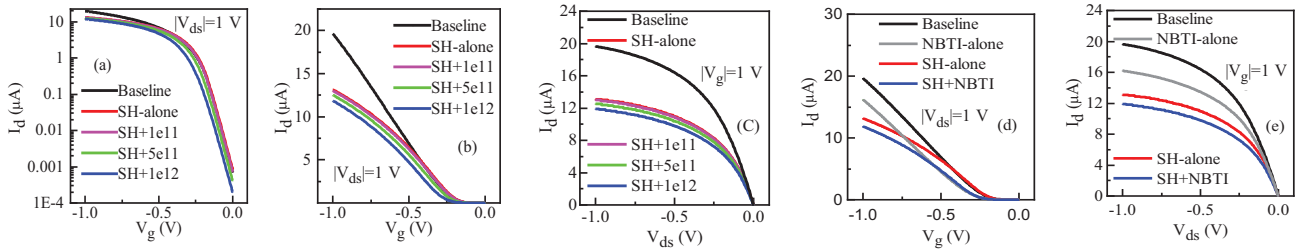


Fig. 4: $I_d$-$V_g$ plots (at high $V_{ds}$) in log- and linear- scales are presented in (a) and (b), respectively, showing the baseline (i.e. no SH, no NBTI), SH-alone (i.e. fresh device under SH effects) and SH+NBTI (i.e. both SH and NBTI effects are jointly considered under varied trap densities $\Delta N_{it}$). (c) $I_d$-$V_d$ (at high $V_g$) characteristic shows that the $I_d$ decreases under SH effects and NBTI causes further degradations on top. (d and e) show the $I_d$-$V_g$ and $I_d$-$V_d$ characteristics, respectively, for the baseline, NBTI-alone, SH-alone and SH+NBTI. The EOL (represented by $\Delta N_{it} = 1e12\text{cm}^{-2}$) is considered here in this analysis. The resulting $\Delta V_T$ and $\Delta I_{ON}$ are summarized in Table I.

**Modeling NBTI effects in TCAD:** To model the impact of NBTI on the electrical characteristics of nanowire, we simulate varied trap densities ($\Delta N_{it}$=$1e11$, $5e11$ and $1e12\text{cm}^{-2}$). Traps are uniformly distributed within the entire bandgap. The presence of traps at the interface layer lower the vertical electric field, which manifests itself as an increase in the threshold voltage ($V_T$) of pSiNW FETs. In addition, when lateral electric field is applied, NBTI-induced interface traps interact with the moving carriers and thus reduce their mobility ($\mu$) due to Coulomb scattering [14]. Degradations over time in both $V_T$ and $\mu$ contribute to ON current reductions.

In Fig. 2, we show the induced degradations due to NBTI alone (i.e. without SH) under the impact of varied trap densities. Fig. 2(a) shows $I_{ON}$ reductions with the increase in $\Delta N_{it}$. The reduction in carrier mobility is observed in Fig. 2(b) by the transconductance ($g_m$) reduction with $\Delta N_{it}$ increase. Fig. 2(c) summarizes the impact of varied $\Delta N_{it}$ (at low $V_{ds}$) on $V_T$ increase and $g_m$ reduction. At $\Delta N_{it}$ of $1e12\text{cm}^{-2}$, $\Delta V_T$ reaches 55mV, which corresponds to 10 years of operation and is considered to be endo of lifetime (EOL). Fig. 2(d) shows the relation between $\Delta V_T$ and lifetime. Note that NBTI-induced $\Delta V_T$ over time is governed by the power law with an exponent of 0.16 [15].

## III. Analyzing the Effects of Self-Heating and NBTI Aging *individually* and *jointly*

Fig. 3(a) shows the 3D device thermal profiles due to self-heating under the impact that NBTI-induced traps have from fresh to EOL for pSiNW FET. Generated heat across the nanowire becomes less with the increase in trap density ($\Delta N_{it}$) and therefore NBTI can mitigate to some degree SH effects. Fig. 3(b) shows the lattice temperature increase ($\Delta T_L$), under the effects of SH, along the channel including extension length. The maximum temperature ($\Delta T_{LMax}$) is $\sim$166K near the drain side and it is then reduced to $\sim$150K at EOL due to NBTI-induced traps. This is because NBTI causes $I_d$ reductions (Fig. 2(a)) due to $V_T$ increase and $\mu$ decrease (Fig. 2(c)). Hence, the total source power ($P$=$I_dV_{ds}$) decreases and thus SH effects become less (i.e. less heat is generated across the device akin to less power densities). Fig. 3(c and d) show the impact of drain and gate voltage ($V_{ds}$ and $V_g$) on $\Delta T_{LMax}$ and how the latter is reduced with the increase in $\Delta N_{it}$. Fig. 3(e) demonstrates the relation between $\Delta T_{LMax}$ and $\Delta N_{it}$ with a reduction in the $\Delta T_{LMax}$ by $\sim$16K when $\Delta N_{it}$=$1e12\text{cm}^{-2}$, which represents the end of lifetime (EOL) in our analysis (10 years, as shown in Fig. 2(d)).

### *A. Impact of NBTI and SH on the Electrical Characteristics of pSiNW FETs: $V_T$, $g_m$ and $I_{ON}$*

To understand better the induced degradation by each phenomena alone (i.e. NBTI and SH) and how they may cancel or magnify each other, we investigate the following scenarios:
**(1) Baseline:** It represents the fresh pSiNW FET without either NBTI or SH effects: i.e. NBTI (✗), SH (✗).
**(2) SH-alone:** It represents the fresh pSiNW FET but under the effects of SH only, i.e. NBTI (✗), SH (✓).
**(3) NBTI-alone:** It represents the pSiNW FET but under the effects of NBTI only, i.e. NBTI (✓), SH (✗).
**(4) SH+NBTI:** It represents the pSiNW FET under the effects of both NBTI and SH *jointly*, i.e. NBTI (✓), SH (✓), in which

| | $\Delta N_{it}(cm^{-2})$ | 0 (fresh) | 1e11 | 5e11 | 1e12 (EOL) |
|---|---|---|---|---|---|
| w/o self-heating: NBTI-alone | $\Delta V_T(mV)$ | 0 | +6.8 | +35 | +75 |
| | $\lvert\Delta g_m\rvert(\mu A/V)$ | 0 | 0.3 | 1.3 | 2.5 |
| | $\lvert\Delta I_{ON}\rvert(\mu A)$ | 0 | 0.3 | 1.7 | 3.4 |
| W/ self-heating: SH-alone and SH+NBTI | $\Delta V_T(mV)$ | −47 | −41 | −16 | +24.6 |
| | $\lvert\Delta g_m\rvert(\mu A/V)$ | 4.9 | 5.3 | 5.87 | 6.19 |
| | $\lvert\Delta I_{ON}\rvert(\mu A)$ | 6.47 | 6.59 | 7.09 | 7.75 |

TABLE I: Analysis at high $V_{ds}$ of $\Delta V_T$, $\Delta I_{ON}$ and $\Delta g_m$(max) with and without SH effects under varied densities of NBTI-induced traps from fresh to end-of-lifetime (EOL) for the case of single-wire pSiNW FET.

the interaction between varied NBTI-induced trap densities and SH (referred in figures as: SH+1$e$11, SH+5$e$11 and SH+1$e$12) are jointly considered within TCAD simulations.

Fig. 4(a-c) demonstrate the device characteristics $I_d$-$V_g$ (both in linear- and log-scale) and $I_d$-$V_d$ for each of baseline, SH-alone and SH+NBTI cases. As shown, generated heat by SH reduces $I_{ON}$ and then NBTI results in further reductions on top of that. In addition, we show in Fig. 4(d, e) comparisons between the baseline, NBTI-alone, SH-alone, SH+NBTI at EOL for both $I_d$-$V_g$ and $I_d$-$V_d$ characteristics. As can be noticed, the induced reduction in $I_{ON}$ due to SH is larger than NBTI. Both NBTI and SH can jointly degrade the ON current by around 40%.

Table I summarizes the induced $\Delta V_T$, $\Delta g_m$ and $\Delta I_{ON}$ from fresh to EOL with and without SH effects. Note that $\Delta g_m$ in our analysis always refers to the reduction in the *maximum* $g_m$. As can be noticed, SH still reduces $I_{ON}$ despite the reduction in $V_T$. Such an improvement in $V_T$ is actually due to the increase in the hole thermal energy. However, due to the large degradation in carrier mobility ($\mu$), which does dominate, improvements in $V_T$ is canceled out and therefore $I_{ON}$ gets, at the end, degraded. From results in Table I, the following key observations can be made:

- Without SH, NBTI-alone *increases* $V_T$, at EOL, by up to +75mV and decreases $|g_m|$ and $|I_{ON}|$ by up to 2.5$\mu$A/V and 3.4$\mu$A, respectively.
- Without NBTI, SH-alone *decreases* $V_T$ by −47mV and it deceases $|g_m|$ and $|I_{ON}|$ by 4.9$\mu$A/V and 6.47$\mu$A, respectively.
- Under the joint impact of SH and NBTI (SH+NBTI):
  (1) the overall increase in $V_T$ is up to +24.6mV. This is smaller than the sum of the *individual* $\Delta V_T$ caused by NBTI-alone (+75mV) and SH-alone (−47mV):
  $75 - 47 = 28\text{mV} > 24.6\text{mV}$.
  (2) The overall $|\Delta g_m|$ reduction is up to 6.19$\mu$A/V. This is also smaller than the sum of the *individual* $\Delta g_m$ caused by NBTI-alone (2.5$\mu$A/V) and SH-alone (4.9$\mu$A/V):
  $2.5 + 4.9 = 7.4\mu\text{A/V} > 6.19\mu\text{/V}$.
  (3) The overall $|\Delta I_{ON}|$ reduction is up to 7.75$\mu$A. This is also smaller than the sum of the individual $|\Delta I_{ON}|$ caused by NBTI-alone (3.4$\mu$A) and SH-alone (6.47$\mu$A).
  $3.4 + 6.47 = 9.87\mu\text{A} > 7.75\mu\text{A}$.

*Therefore, modeling the induced degradations by SH and NBTI individually results in overestimations. Hence, SH and NBTI effects need to be jointly modeled for accurate analysis.*

| | $\Delta N_{it}(cm^{-2})$ | 0 (fresh) | 1e11 | 5e11 | 1e12 (EOL) |
|---|---|---|---|---|---|
| $R_{th}(K/\mu W)$ | | 12.62 | 12.61 | 12.6 | 12.59 |
| $C_{th}(fJ/K)$ | $\tau_{th}$ = 200ns | 15.848 | 15.86 | 15.87 | 15.89 |
| | $\tau_{th}$ = 100ns | 7.92 | 7.93 | 7.94 | 7.95 |

TABLE II: Analysis of thermal resistance ($R_{th}$) and thermal capacitance ($C_{th}$) under different interface trap densities ($\Delta N_{it}$) induced by NBTI from fresh to end-of-lifetime (EOL). For the $C_{th}$ analysis, different thermal time constants ($\tau_{th}$) are considered.

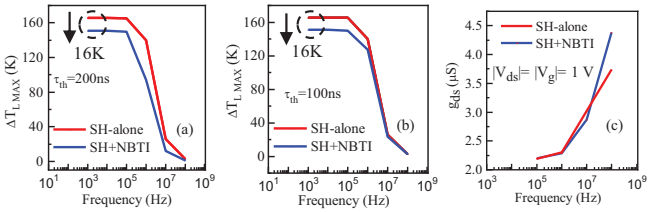


Fig. 5: (a and b) show, for a single-wire pSiNW FET, the variation of $\Delta T_{LMax}$ for SH-alone (no NBTI effects) and SH+NBTI (both SH and NBTI effects jointly) at EOL (i.e. $\Delta N_{it}$ = 1e12cm$^{-2}$) under a wide range of frequencies for $\tau_{th}$ = 200ns and 100ns, respectively. As shown, the impact of SH is suppressed at high frequency and NBTI leads to a lower temperature at low frequencies. The temperature reduction is ∼16K, which is consistent with the results in Fig. 3(e). (c) shows the relation between the drain conductance ($g_{ds}$) and switching frequency for the SH-alone (no NBTI) and SH+NBTI at EOL. Results obtained from TCAD simulations in which AC signals, at varied frequencies, are applied at the drain terminal of transistor.

### *B. Impact of NBTI and SH on the Thermal Characteristics of pSiNW FET: $R_{th}$ and $C_{th}$*

Based on the electro-thermal TCAD simulations, we extract the thermal resistance ($R_{th}$) from fresh to EOL based on described method in [17]. In practice, $\Delta T_{LMax}$ rises linearly with the dissipated power $P$ due to SH, allowing the extraction of $R_{th}$ from the slope of $\Delta T_{LMax} = R_{th} \times P$. Table II summarizes the results of $R_{th}$. As can be observed, with NBTI, $R_{th}$ decreases. Reductions in $R_{th}$, in turn, lead to reductions in the lattice temperature. This is consistent with the earlier analysis presented in Fig. 3(a-e) in which a reduction of 16K is observed in the maximum lattice temperature at EOL.

Table II also reports the thermal capacitance ($C_{th}$) from fresh to EOL. Since the thermal time constant ($\tau_{th}$) might have a range of values (varied heat dissipation process because of multiple heat spreading path), we extract $C_{th}$ at two different $\tau_{th}$: 100ns, 200ns. These values are within the reported data [4], [12]. Due to NBTI-induced $R_{th}$ reduction, $C_{th}$ increases as a result (see Table II), assuming that $\tau_{th}$ remains unaffected by NBTI. Based on the extracted $R_{th}$ and $C_{th}$, $\Delta T_{LMax}$ for a particular switching frequency can be calculated from Eq. 1, which shows the relation between the temperature increase and $R_{th}$, $C_{th}$ and $f_{th}$ [17]. Fig. 5(a and b) demonstrate the maximum lattice temperature for a wide range of switching frequencies for the two selected thermal time constants under the effects of SH-alone (i.e. fresh) and SH together with NBTI at EOL.

$$\Delta T(f) = \frac{\Delta(I_{ds}V_{ds}) \cdot R_{th}}{\sqrt{1 + (f/f_{th})^2}} \qquad (1)$$
$$f_{th} = 1/(2\pi\tau_{th}) \; ; \; \tau_{th} = R_{th} \cdot C_{th}$$

To study the thermal time constant ($\tau_{th}$), drain conductance ($g_{ds}$) method is typically applied [7], [8]. Therefore, in order to investigate whether NBTI may affect $\tau_{th}$, we perform, using

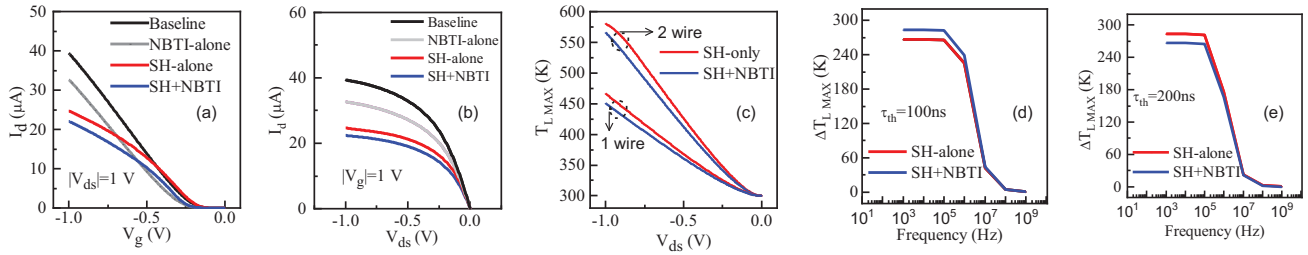


Fig. 6: Analysis of the *individual* impact of NBTI and SH as well as the *joint* impact for multi-wire (2-wires) pSiNW FET. (a and b) show the $I_d$-$V_g$ and $I_d$-$V_{ds}$ characteristics. Similar to the single-wire device, NBTI results in less degradation in the ON current compared to SH. (c) shows a comparison between single-wire and multi-wire devices w.r.t the maximum lattice temperature. The temperature increase is larger in the multi-wire device due to the much higher increase in current densities. (d and e) compare the effects of SH-alone and the joint impact of SH and NBTI (SH+NBTI) w.r.t the maximum temperature increase ($\Delta T_{LMax}$) under a wide range of switching frequencies for two different thermal time constants ($\tau_{th}$=100ns and 200ns).

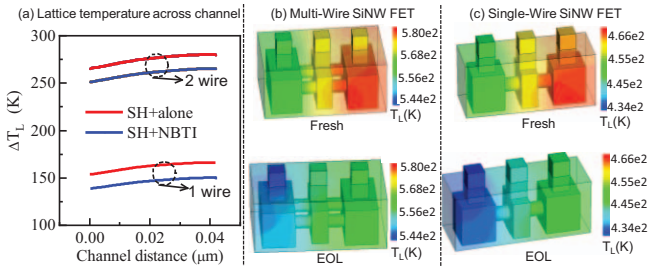


Fig. 7: Comparisons between single-wire and multi-wire pSiNW FETs w.r.t the increase in lattice temperature due to SH effects for both cases (SH-alone and SH+NBTI). (a) shows $\Delta T_{LMax}$ across the channel. (b, c) show a comparison (for the case of single-wire and multi-wire devices, respectively) between the 3D thermal profiles under the effects of SH alone (i.e. fresh) and under the joint impact of SH and NBTI at EOL.

| | $\Delta N_{it}(cm^{-2})$ | 0 (fresh) | 1e12 (EOL) |
|---|---|---|---|
| w/o self-heating: NBTI-alone | $\Delta V_T(mV)$ | 0 | +72.8 |
| | $\lvert\Delta g_m\rvert(\mu A/V)$ | 0 | 9.7 |
| | $\lvert\Delta I_{ON}\rvert(\mu A)$ | 0 | 6.7 |
| W/ self-heating: SH-alone and SH+NBTI | $\Delta V_T(mV)$ | −54 | +1.4 |
| | $\lvert\Delta g_m\rvert(\mu A/V)$ | 9.73 | 10.44 |
| | $\lvert\Delta I_{ON}\rvert(\mu A)$ | 14.67 | 16.97 |

TABLE III: Analysis, at high $V_{ds}$, of $\Delta V_T$, $\Delta I_{ON}$ and $\Delta g_m$(max) with and without SH effects for the case of multi-wire pSiNW FET. Analysis is done for the fresh (i.e. no NBTI) case and the end-of-lifetime (EOL) case.

TCAD, AC conductance simulations for drain conductance in which AC signals, at varied frequencies, are applied at the drain terminal of pSiNW FET. Fig. 5(c) shows the results for the fresh and EOL cases. As can be seen, when $\tau_{th}$=100ns or 200ns (i.e. $f_{th}$=10MHz, 5MHz), the effects of SH and NBTI (i.e. SH+NBTI) at EOL result in a negligible change in $g_{ds}$ compared to the impact that SH alone without NBTI (i.e. SH-alone) has. This indicates that NBTI does not lead to an observable change in thermal time constant.

## IV. Multi-Wire SiNW FET Devices

For a more detailed analysis, we also investigate how the *individual* impact of NBTI and SH as well as their *joint* impact affect the electro-thermal characteristics of multi-wire (2-wires) pSiNW FETs. Fig. 6 summarizes our analysis in which (a and b) show the the $I_d$-$V_g$ and $I_d$-$V_{ds}$ characteristics for the baseline (i.e. no NBIT, no SH), NBTI-alone, SH-alone and the effects of SH together with NBTI (SH+NBTI). Note that the ON current is 2x higher compared to the ON current in the case of a single-wire pSiNW FET (see Fig. 2(b)). This is due to the duplication in number of wires.

Similar to the single-wire device, NBTI results in less degradation in the ON current compared to SH. The overall $I_{ON}$ degradation due to both NBTI and SH is around 50%, which is higher than the overall $I_{ON}$ degradation in the case of single-wire device. Fig. 6(c) demonstrates a comparison between single-wire and multi-wire devices w.r.t the maximum lattice temperature ($T_{LMax}$) (further details in Fig. 7(a and b). The temperature increase is larger in the multi-wire device due to the much higher increase in current densities. However, the impact of NBTI on mitigating SH effects (i.e. the impact of NBTI traps on reducing $T_{LMax}$) remains very similar (around 16K in both single-wire and multi-wire devices). Then, as explained above, we calculate the thermal resistance and capacitance ($R_{th}$ and $C_{th}$) for the multi-wire device in order to analyze SH dependence with frequency. Compared to the single-wire device, we found $R_{th}$ to be slightly smaller (12.01K/$\mu$W), due to the larger surface to dissipate heat [18]. NBTI reduces $R_{th}$ at EOL to 11.9K/$\mu$W, which explains the lower lattice temperature when NBTI and SH effects are jointly analyzed (see Fig. 7(b)). Fig. 6(d and e) compare the effects of SH-alone and the joint impact of SH and NBTI (SH+NBTI) w.r.t the maximum temperature increase under a wide range of switching frequencies for the two thermal time constants ($\tau_{th}$=100ns and 200ns). Fig. 7(a) demonstrates a comparison between single-wire and multi-wire pSiNW FETs w.r.t the increase in lattice temperature across the channel due to SH effects alone (SH-alone) and the joint impact of SH and NBTI (SH+NBTI). Fig. 7(b, c) shows a comparison (for the case of multi-wire and single-wire devices, respectively) between the 3D thermal profile under the effects of SH alone (i.e. fresh) and the 3D thermal profile under the joint impact of SH and NBTI at EOL. As can be noticed, multi-wire devices suffer more from SH than single-wire devices and in both cases NBTI mitigates SH and reduces the generated heat.

Table III summarizes the reductions in $V_T$, $g_m$ and $I_{ON}$ for the case of NBTI-alone (i.e. no SH) and the case of NBTI+SH. As shown, the overall $\Delta V_T$ at EOL due to NBTI and SH effects is merely 1.4mV. *This shows how induced degradation by SH and NBTI cancel each other w.r.t* $\Delta V_T$. In Fig. 8(a) we summarize the estimation error when NBTI and SH are *individually* modeled compared to modeling them jointly. As shown, both single-wire and multi-wire devices exhibit a similar error in the case of ON current degradation (around 20%). However, the error is quite large (92%) in

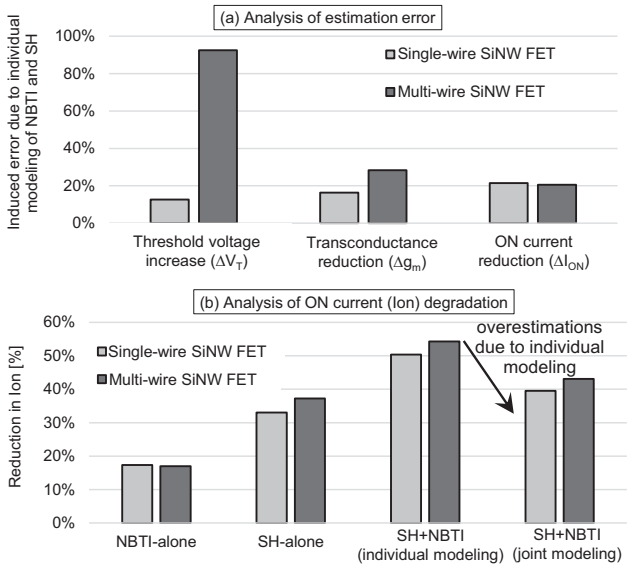


Fig. 8: (a) Estimation errors in the electrical characteristics of single-wire and multi-wire pSiNW FET stemmed from the individual modeling of NBTI and SH. (b) Reduction in ON current due to NBTI-alone, SH-alone and SH+NBTI (under individual and joint modeling).

the case of $\Delta V_T$ degradation due to the cancellation effect. Fig. 8(b) clarifies the ON current reductions in single-wire and multi-wire devices under the individual and joint impact of SH and NBTI. As shown, treating NBTI and SH individually results in a noticeable overestimation, which later can drop the accuracy of any circuit delay analysis.

Finally, to put the analysis for SH and NBTI in a context, we study how the frequency of a 13-stages ring oscillator will be affected by NBTI-alone, SH-alone and SH+NBTI. Simulations are done in HSPICE using our Verilog-A model compact model for nanowires [16]. The model is well calibrated against TCAD data for both n-SiNW and p-SiNW FETs as shown in Fig. 1(c, d). The compact model is augmented to consider the $I_{ON}$ reduction induced by NBTI-alone, SH-alone and SH+NBTI (joint modeling), as obtained from TCAD analysis. To study the impact of SH and NBTI but under an individual modeling, we sum up the individual $\Delta I_{ON}$ caused by each NBTI alone and SH alone. Fig. 9 demonstrates how SH results in a larger reduction in frequency compared to NBTI, which is expected due to the larger induced reduction in $I_{ON}$ (see Fig. 8(b)). In addition, modeling NBTI and SH individually instead of jointly leads to a noticeable overestimation of frequency reduction. Such overestimation will result in employing inefficient (i.e. larger than what is actually required) timing guardbands. As explained in Section I, these guardbands are needed to protect circuits against timing violations caused by SH- and NBTI-induced delay increases over time.

## V. Summary and Conclusions

We analyzed the effects of self-heating and NBTI in single-wire and multi-wire pSiNW FETs. Our investigation showed that generated traps by NBTI mitigate to some degree the effects of self-heating leading over time to reductions in the lattice temperature. We demonstrated that NBTI and SH

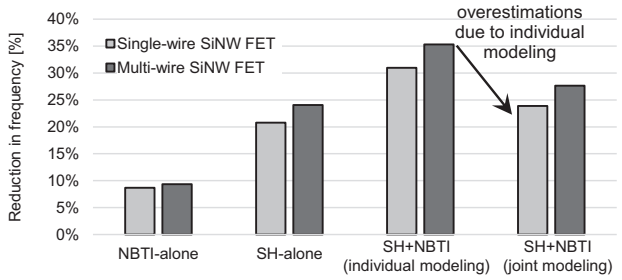


Fig. 9: Reduction in the frequency of 13-stages ring oscillator for both single-wire and multi-wire devices, demonstrating how individual modeling of NBTI and SH leads to a noticeable overestimation of frequency reduction. In this analysis, nSiNW FET remains non-degraded (i.e. no SH, no NBTI).

degradations need to be modeled jointly and not individually due the existing interdependencies between them. *Neglecting that leads to inaccurate analysis for device parameters (e.g., $V_T$, $g_m$ and $I_{ON}$) as well as for circuits delay estimations.*

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