BeLDPC: Bit Errors Aware Adaptive Rate LDPC Codes for 3D TLC NAND Flash Memory

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***Abstract*—Three-dimensional (3D) NAND flash memory has high capacity and cell storage density by using the multi-bit technology and vertical stack architecture, but degrading data reliability due to high raw bit error rates (RBER) caused by program/erase (P/E) cycles and retention periods. Low-density parity-check (LDPC) codes become more popular error-correcting technologies to improve data reliability due to strong error correction capability, but introducing more decoding iterations at higher RBER. To reduce decoding iterations, this paper proposes BeLDPC: bit errors aware adaptive rate LDPC codes for 3D triple-level cell (TLC) NAND flash memory. Firstly, bit error characteristics in 3D charge trap TLC NAND flash memory are studied on a real FPGA testing platform, including asymmetric bit flipping and temporal locality of bit errors. Then, based on these characteristics, a high-efficiency LDPC code is designed. Experimental results show BeLDPC can reduce decoding iterations under different P/E cycles and retention periods.**

I. Introduction

Three-dimensional (3D) NAND flash memory [1, 2] adopts vertical stack architecture and stores multi-bit per cell, introducing high capacity and cell storage density. However, high raw bit error rates (RBER) are induced by program/erase (P/E) cycles and retention errors, reducing data reliability [3]. Low-density parity-check (LDPC) codes [4] are more popular error-correcting technologies to ensure data reliability for 3D NAND flash memory. Although LDPC codes have strong error correction capability, high RBER leads to more decoding iterations, increasing decoding latency. For decreasing decoding iterations and latency, it is necessary to propose LDPC codes with high-efficiency for 3D TLC NAND flash memory.

Many prior works are proposed to investigate error patterns of 3D NAND flash memory and LDPC codes. Luo et al. [1] observed new error characteristics in 3D NAND flash memory through real experiments and proposed the HeatWatch [2] scheme to improve the lifetime of 3D NAND flash memory by adjusting the reading reference voltage. Liu et al. [5] characterized reliability and threshold shifting characteristics in 3D charge trap (CT) TLC NAND flash memory. Wu et al. [6] and Xiong et al. [7] studied the error modes of 3D CT TLC and floating gate (FG) multi-level cell (MLC) NAND flash memories on the real FPGA platform, respectively. Exploiting flash errors can reduce sensing levels [4, 8] of LDPC codes and improve decoding throughput [9, 10]. Using a machine learning method to classify [11] and predict [12] RBER is helpful to decrease LDPC decoding latency. These prior works do not fully explore and study the bit error characteristics in 3D TLC NAND flash memory, without considering to exploit the bit error characteristics to design effective LDPC codes for improving data reliability and while reducing decoding latency.

This paper develops BeLDPC: bit errors aware adaptive rate LDPC codes for 3D TLC NAND flash memory. Firstly, bit error characteristics in 3D CT TLC NAND flash memory, such as asymmetric bit flipping and the temporal locality of bit errors, are investigated by exploiting a real FPGA hardware testing platform. Through real experiments, there exists seriously unbalanced bit flipping from 1 -> 0 and 0 -> 1 among the most significant bit (MSB), central significant bit (CSB), and least significant bit (LSB) pages. The bit error rate from 1 -> 0 in LSB pages is much higher than that of CSB and MSB pages as the increase of P/E cycles and retention periods. More interestingly, bit errors happen to the same locations at a short retention period, called temporal locality of bit errors. These bit error characteristics are beneficial to design more effective LDPC codes. Then, BeLDPC with high-efficiency is proposed to guarantee data reliability and reducing decoding latency. LDPC codes with different rates are selected to encode according to the change of RBER for lowering down the decoding iterations and ensuring data reliability. Moreover, during decoding, log-likelihood ratio (LLR) information is adjusted to assign different weights for bit 1 and 0 for accelerating decoding convergence.

The main contributions of this paper are as follows:

- By exploiting a real FPGA hardware platform, bit error characteristics in 3D CT TLC NAND flash memory are first studied. By collecting and analyzing experimental data, this paper observes that error rates of 1 -> 0 and 0 -> 1 in LSB pages, CSB pages, and MSB pages are abnormal. There is asymmetric bit flipping among these three pages, higher error rates from 1 -> 0 in LSB pages as P/E cycles and retention periods increase. Then, the temporal locality of bit errors is revealed under different retention periods. There are much higher repetitive bit error percentages in LSB pages than that of CSB and MSB pages.
- Motivated by the bit error characteristics, this paper proposes BeLDPC to reduce decoding iterations and latency. According to variations of RBER, performing LDPC encoding with different rates can effectively guarantee data reliability and reduce the decoding iterations. Furthermore, when implementing soft decoding algorithms, the LLR value of 1 and 0 is modified to improve updating precision and hence facilitating decoding.

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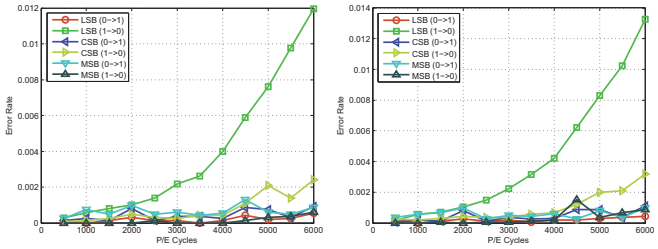


(a) Retention 1-week (b) Retention 2-week

(c) Retention 3-week (d) Retention 4-week

Fig. 1. Error rates from 1 -> 0 and 0 -> 1 in 3D TLC NAND flash pages.

- By conducting the simulation experiment, the effectiveness of BeLDPC is validated. Simulation results show decoding iterations are significantly reduced.

The rest is organized as follows. Section II presents bit error characteristics in 3D CT TLC NAND flash memory through real experiments. The proposed BeLDPC is introduced in Section III and the conclusion is made in Section IV.

II. Bit Error Characteristics in 3D CT TLC NAND Flash Memory

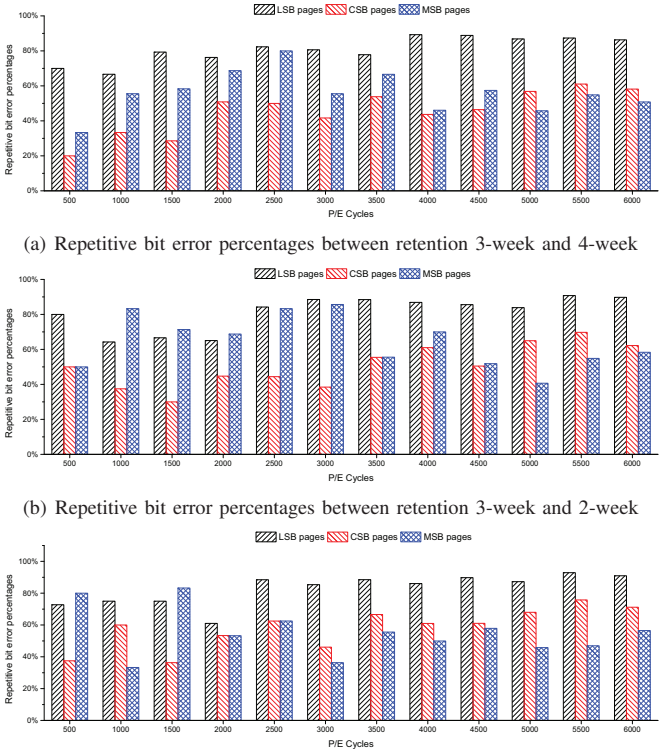
In this section, bit error characteristics in 3D CT TLC NAND flash memory are explored through real experiments. Firstly, the experimental methodology is described. Then, the observations are given by analyzing experimental results.

A. Experimental Methodology

The bit error characteristics are revealed via the real FPGA hardware testing platform. This platform is equipped with four sockets. The windows-based applications communicate with the hardware platform by using the PCIe interference that obeys the NVMe protocol. 3D CT TLC NAND flash memory is selected as the real testing chip. The read, program, and erase commands are sent to the testing chip. The chip under different retention periods is tested, i.e., 1-week, 2-week, 3-week, and 4-week. The P/E cycles are increased from 0 to 6000. The data is collected at the P/E interval as 500. Each block consists of 512 pages. The size of each page is 18KB, including 16KB user space and 2KB spare space.

B. Asymmetric Bit Flipping

We count the error rates from 1 -> 0 and 0 -> 1 in LSB pages, CSB pages, and MSB pages of 3D TLC NAND flash memory, as shown in Fig. 1. Experimental results show that there is asymmetric bit flipping under different P/E cycles and retention periods. It is much easier to happen bit flipping from 1-> 0 in LSB pages with higher error rates as P/E cycles and retention periods increase. When retention periods are fixed, the error rates rapidly increase with the increase of P/E cycles. For example, for retention 1-week, the error rate gets to 1.2×10^{-2} at the P/E cycle of 6000. Moreover, there is also much higher error rates from 1-> 0 in LSB pages with longer retention periods under the same P/E cycles. The error rates are improved from 1.2×10^{-2} at retention 1-week to 1.6×10^{-2} at retention 4-week when the P/E cycle is 6000.



(a) Repetitive bit error percentages between retention 3-week and 4-week

(b) Repetitive bit error percentages between retention 3-week and 2-week

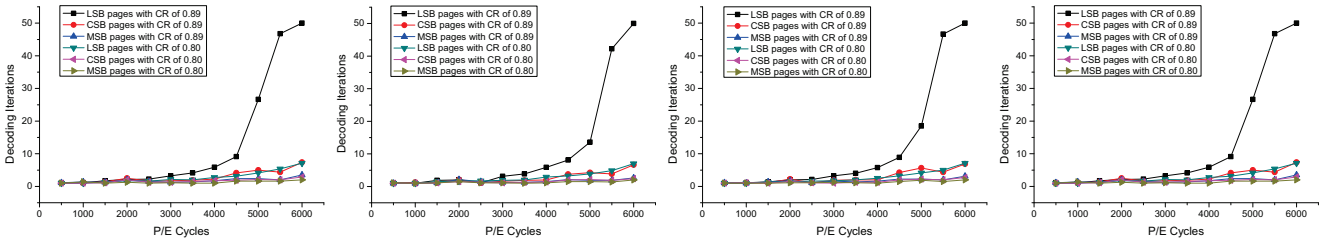
(c) Repetitive bit error percentages between retention 2-week and 1-week

Fig. 2. Repetitive bit error percentages of 3D TLC NAND flash memory.

There are much lower error rates for other bit flipping in different pages, such as 0 -> 1 in LSB pages, 1 -> 0 and 0 -> 1 in CSB pages, 1 -> 0 and 0 -> 1 in MSB pages. The error rates change smoothly with the increases of P/E cycles and retention periods. For example, most of the error rates are much lower than 2×10^{-3} when the P/E cycles are increased from 0 to 6000. The error rates are only higher than 2×10^{-3} when the P/E cycle is beyond 5000. The bit flipping from 1-> 0 in LSB pages dominates in 3D TLC NAND flash, leading to high error rates and lower data reliability. To ensure data reliability, it is very necessary to design LDPC codes with high error correction performance to lower down the bit flipping error from 1-> 0 in LSB pages and eliminate the asymmetric bit errors. This is because that once the errors in LSB pages exceed the error correction capability of error correction codes (ECC), the reliability cannot be ensured and the block is remarked as invalid.

C. Temporal Locality of Bit Errors

When suffering from different P/E cycles, we count repetitive bit error percentages under retention 1-week, retention 2-week, retention 3-week, and retention 4-week, as shown in Fig. 2. On the one hand, we investigate the repetitive bit error percentages



(a) Retention 1-week (b) Retention 2-week (c) Retention 3-week (d) Retention 4-week

Fig. 3. Variations of decoding iterations in LSB, CSB, and MSB pages under different P/E cycles and retention periods.

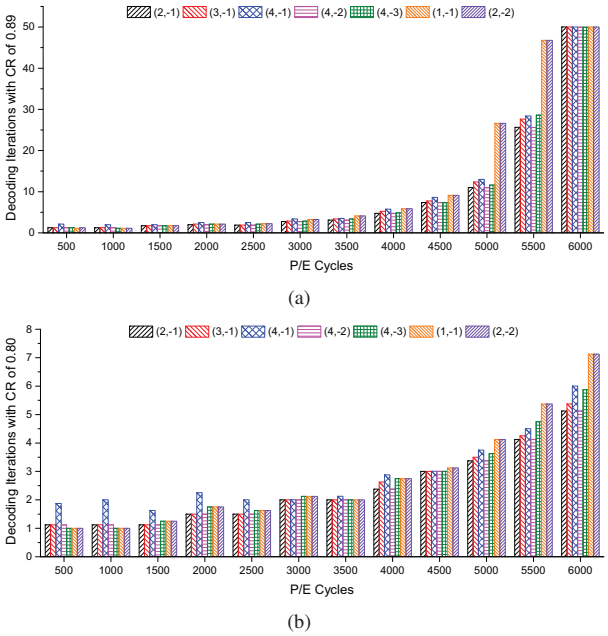


Fig. 4. The effects of different LLR weights on decoding iterations in the LSB pages when using different rates under P/E cycles and retention periods.

in the adjacent retention periods, as shown in Fig. 2 (a), Fig. 2 (b), and Fig. 2 (c). Experimental results show that there are much higher repetitive bit error percentages in the LSB pages than that of the other two pages. The repetitive bit error percentages fluctuate near 80% between the adjacent retention periods with the increase of P/E cycles. The repetitive bit error percentages reach to 90% between retention 4-week and retention 3-week, between 3-week and retention 2-week when the P/E cycles get to 5000 and 6000. The repetitive bit error percentages are relatively low when the P/E cycles are increased from 500 to 2000. The temporal locality of bit errors can be exploited to propose more efficient ECC to reduce the bit errors in 3D TLC NAND flash memory.

III. The Proposed BeLDPC

In this section, we first give the BeLDPC algorithm based on the bit error characteristics. Then, we describe the simulation results, including simulation setup and result analysis.

A. BeLDPC Work Process

The work process of BeLDPC includes encoding and decoding. In the first process described in Algorithm 1, bit data is encoded using adaptive rates for each logical page based on variations of bit errors induced by P/E cycles and retention periods. When P/E cycles and retention are greater than the threshold, the bit data in the LSB page is encoded with low rate R_1 and the bit data in the CSB and MSB is encoded with high R_2. The adaptive rate is exploited to improve decoding convergence speed. In the second process presented in Algorithm 2, when performing hard-decision decoding for the LSB page, according to the bit error features, the LLR information of bit 1 and 0 is adjusted to assign different weights for improving the decoding update accuracy and hence reducing decoding iterations. When implementing hard-decision decoding for the CSB and MSB pages, the LLR information is assigned same weights due to no obvious asymmetry in bit errors. BeLDPC selects different rates for encoding and different LLR weights for decoding based on bit error characteristics, which can minimize the decoding iterations and improve decoding efficiency.

Algorithm 1 BeLDPC Encoding Process

Input: P/E cycles and retention periods
Output: Encoded bit sequences

```
if P/E cycles Pe > thr1 and retention periods Rp > thr2 then
    Implement write and encoding operations
    if Write the LSB page then
        Encoding LSB using low rate R1
    else
        if Write the CSB page then
            Encoding CSB using high rate R2
        else
            if Write the MSB page then
                Encoding MSB using R2
            end if
        end if
    end if
end if
```

B. Simulation Results and Analysis

In this section, we describe the simulation results and give an analysis. In this simulation, we encode the bit data collected from the real FPGA platform. The LSB, CSB, and MSB pages are decoded using the normalized min-sum algorithm [9] performed on the Matlab simulation platform. The decoding iterations are counted with different rates and LLRs. When using rates of 0.89 and 0.80, we count the decoding iterations in LSB, CSB, and MSB pages under different P/E cycles and retention periods, as shown in Fig. 3. When decoding the LSB page with

Algorithm 2 BeLDPC Decoding Process

Input: Soft information of MSB and LSB
Output: Decoding bit sequences

if Decoding the LSB page **then**
  Obtain raw bit data $\overrightarrow{B_{\text{lsb}}} = (b_{lsb1}, b_{lsb2}, \cdots, b_{lsb(n-1)}, b_{lsbn})$ using hard decision reference voltage
  for i=1 from n **do**
    if $b_{lsbi} = 1$ **then**
      Soft information $L_{lsbi} = M$
    else
      $L_{lsbi} = -N$ $(M > N)$ M and N are positive integers.
    end if
  end for
  Set the maximum decoding iteration as N_{max} and take L_{msbi} as initial input to activate decoding operations
  Use the normalized min-sum algorithm to decode
end if
if Successful decoding **then**
  Record decoding results and iteration times
end if
if Decoding the MSB or CSB pages **then**
  Gain raw bit data $\overrightarrow{B_{\text{msb}}} = (b_{msb1}, b_{msb2}, \cdots, b_{msb(n-1)}, b_{msbn})$ and $\overrightarrow{B_{\text{csb}}} = (b_{csb1}, b_{csb2}, \cdots, b_{csb(n-1)}, b_{csbn})$ using hard decision reference voltages
  for i=1 from n **do**
    if $b_{msbi} = 1$ or $b_{csbi} = 1$ **then**
      Soft information $L_{msbi} = -Q$ and $L_{csbi} = -P$
    else
      $L_{msbi} = Q$ and $L_{csbi} = P$ (Q and P are positive integers).
    end if
  end for
  Set the maximum decoding iteration as N_{max} and take L_{msbi} and L_{csbi} as initial input to activate decoding operations
  Repeat Step 11 to Step 15
end if

code rate (CR) of 0.89, the decoding iteration increases with the increase of P/E cycles, regardless of retention 1-week, 2-week, 3-week, and 4-week. When P/E cycles are greater than 5000 and retention periods are 1-week, 2-week, and 3-week, the decoding iteration increases rapidly. When P/E cycles are greater than 4500 and retention periods are 3-week, the decoding iteration rises at a high rate. This is because the higher RBER caused by the longer retention period leads to more decoding iterations. When P/E cycles are 6000, the decoding iteration gets to the maximum value, failure to correct bit errors. This is because the RBER is beyond the error correction capability of LDPC codes. However, when decoding the LSB page with CR of 0.80, the decoding iteration is fewer and increases smoothly due to stronger error correction capability for lower CR. Furthermore, we study the effects of adjusting different LLR weights on decoding iterations in the LSB pages as shown in Fig. 4. For example, (4,-1) denotes $M = 4$ and $N = 1$ as explained in Algorithm 2. In this process of simulations, we take retention 1-week with CR of 0.89 and 2-week with CR of 0.80 as an example to give the effects of different LLR parameters on the decoding iterations. Experimental results show that the decoding iteration with different LLR values increases with the increase of P/E cycles. In the process of decoding, the most appropriate LLR parameter can be selected to reduce the number of decoding iterations in the LSB page.

IV. Conclusion

This paper first studies the characteristics of asymmetric bit flipping and temporal locality of bit errors in 3D CT TLC NAND flash on the real FPGA testing platform. Then, a case study is given, where the bit error characteristics are exploited to design high-efficiency LDPC codes with adaptive rates and LLR weights. In the process of encoding, according to variations of RBER induced by P/E cycles and retention periods, using different rates encodes the bit data in the LSB, CSB, and MSB pages. In the process of decoding, different LLR values are assigned for these three pages based on the bit error features. Simulation results show that the proposed scheme can significantly reduce decoding iterations.

V. Acknowledgement

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