Trading Sensitivity for Power in an IEEE 802.15.4 Conformant Adequate Demodulator

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***Abstract*—In this work, a design of an IEEE 802.15.4 conformant O-QPSK demodulator is proposed, which is capable of trading off receiver sensitivity for power savings. Such design can be used to meet rigid energy and power constraints for many applications in the Internet-of-Things (IoT) context. In a Body Area Network (BAN), for example, the circuits need to operate with extremely limited energy sources, while still meeting the network performance requirements. This challenge can be addressed by the paradigm of adequate computing, which trades off excessive quality of service for power or energy using approximation techniques. Three different, adjustable approximation techniques are integrated into the demodulation to trade off effective signal quantization bit-width, filtering performance, and sampling frequency for power. Such approximations impact incoming signal sensitivity of the demodulator. For detailed trade-off analysis, the proposed design is implemented in a commercial 40-nm CMOS technology to estimate power and in Python to estimate sensitivity. Simulation results show up to 64% power savings by sacrificing 7̃ dB sensitivity.**

***Index Terms*—Internet-of-Things, Wireless Networks, O-QPSK Demodulator, FIR Filter.**

I. Introduction

The power and energy constraints for various applications in the Internet-of-Things (IoT) context become progressively rigid. Extremely small sensor units are required to operate on a very small battery or an energy scavenging circuit. For femtocells with short transmission range, the low noise amplifier and power amplifier become less dominant in power/energy consumption. As highlighted in [1], next to the analog parts, the digital baseband computation and signal processing circuits turn into the main energy and power bottleneck. Such scenarios are insufficiently addressed in the literature. Therefore, in this work, we focus on the power and energy efficiency of the digital part of the wireless radio transceiver i.e. the Digital BaseBand (DBB).

The signal demodulator is the key element in the signal reception, converting the analog data to a digital representation of the received packet. IEEE 802.15.4 is a low-rate and low-power standard specification for physical and MAC layers popular in IoT. IEEE 802.15.4 conformant transceivers incorporate many effective power and energy reduction techniques, such as different ways to minimize the transmission time and simple, energy-efficient demodulation schemes. The IEEE 802.15.4 conformant demodulator utilizes Offset Quadrature Phase Shift Keying (O-QPSK) and Direct Sequence Spread Spectrum (DSSS) techniques that allow robust and simple demodulation suitable for low-power radios. The architecture

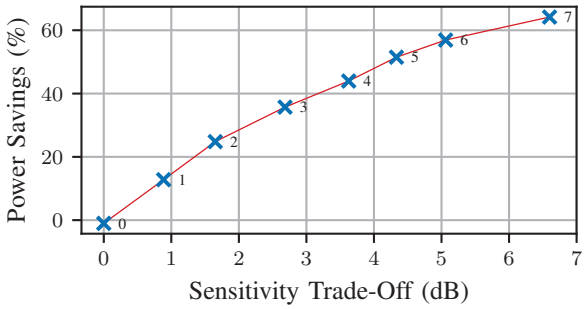

Fig. 1. Adjustable power-sensitivity trade-off with adequate demodulator.

of a typical O-QPSK demodulator is illustrated in Fig. 2. The signal is represented by In-phase (I) and Quadrature (Q) components. In order to align I and Q of an O-QPSK signal, first I is delayed by a half symbol time with the delay element D. After sampling and delay, the incoming signal is filtered with digital techniques such as a Finite Impulse Response (FIR) filter. The filtered signal is down-sampled and encoded using Return to Zero (RZ) coding and a DSSS correlation (CORR). The low complexity of the architecture allows power-efficient implementation. Further power reductions can be achieved through integration of the demodulator on chip with application of low-power digital design techniques such as clock gating, dynamic voltage scaling, and power gating.

Even with all conventional techniques applied, the rigid power constraints remain a challenge for some emerging applications such as BAN. Adequate computing [2] is an emerging technique, which is complementary to the conventional power/energy reduction techniques and provides additional savings. Adequate computing proposes to trade off excessive signal quality for power or energy savings, using techniques such as approximate computing or stochastic computing [3]. The idea of approximate computing in the digital baseband arises from an observation that errors in the digital computation can be masked by incoming channel noise and do not degrade the performance on one side, but

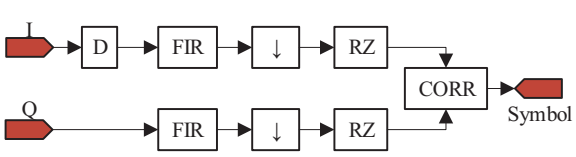

Fig. 2. Architecture of a typical 802.15.4 conformant demodulator.

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provide energy optimization opportunities on the other side. However, integration of adequate computing into the low-power transceiver is barely addressed in the literature.

In this work, the design of an IEEE 802.15.4 conformant O-QPSK demodulator is proposed, which can trade off the sensitivity for additional power savings. To enable this trade-off, we investigate techniques to control the filtering performance, sampling frequency, and bit-width of the signal. The approximations of these three aspects cause a reduction of the sensitivity on the one hand, and enable more power-efficient operating modes on the other hand. The relation between sensitivity and power is analyzed in a demodulator co-design at the signal level and the RTL level. The resulting design provides several operating modes which can be used in better-than-worst-case receiver operational conditions. Note that those modes can be configured at deployment time or run-time if the channel quality information is available. The trade-off is illustrated in Fig. 1, where the crosses indicate various operating modes. In Mode 0, the demodulator does not sacrifice any sensitivity, while in Mode 7, the demodulator trades around 7dB of sensitivity for 64% of power savings.

Contribution: This work addresses the power-efficiency need in the IoT domain and contributes to the following aspects:

- a novel sensitivity-adequate O-QPSK demodulator design with bypassable comparator, bypassable poly-phase filter stage, and discardable In-phase signal approximations;
- an adjustable power-sensitivity trade-off with 7 dB sensitivity degradation for 64% power savings;
- a bench-marking flow combining RTL-level simulations for power evaluation, and Python-based signal modeling.

The rest of this paper is structured as follows. In Section II, related literature is presented. The proposal of the demodulator design is given in Section III. In Section IV, the design is evaluated. The paper is concluded in Section V.

II. Related Work

State-of-the-art IEEE 802.15.4 Demodulators: Since the IEEE 802.15.4 standard is released, many energy and power-efficient transceiver designs have been proposed in the literature, such as described in [4]. In [5] the authors present the state-of-the-art design of an IEEE 802.15.4 conformant transceiver. However, the authors focus on the analog front end as main power hungry part of the transceiver and on their multi-standard DBB implementation. The DBB from [5] is highly flexible but inferior to our baseline in both power efficiency and sensitivity. Only few publications, such as [6], focus on energy efficiency of the digital part. In [6], the proposed improvement in the energy efficiency is based on the technique of under-sampling [7], which is briefly addressed in the last paragraph of this section.

State-of-the-art FIR Filters: For sufficient demodulation robustness against noise, the incoming signal is conventionally over-sampled with increased bit-width, and then filtered in the digital domain using decimation filtering techniques. In [8] multistage poly phase filtering and decimation is demonstrated,

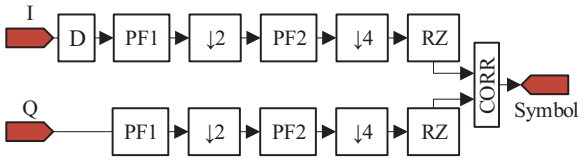

Fig. 3. The IEEE 802.15.4 conformant reference design.

which is more power-efficient than the single stage decimation filter design. In this work, the poly phase decimation filter is integrated as state-of-the-art in the reference design and then approximated to gain in power efficiency.

State-of-the-art Adequate Computing: In [2] and [9] the adequate computing paradigm is discussed and applied to one of the key elements in the transceiver - the Received Signal Strength Indicator (RSSI) with opportunities to save power in exchange for a tolerable error rate in channel assessment. In [6], the authors describe the run-time adjustable technique of under-sampling of the DSSS which results in adjustable power-quality trade-off. Our work has a similar objective, yet with a different approach and different baseline design. The authors from [6] do not address the sample decimation potential after the filtering. We use an architecture from [10] which applies the decimation after the matched filter, so that the DSSS decoding can be performed at a frequency of 1 MHz instead of 8 MHz with negligible performance loss. In this work this potential is exploited resulting in significant increase of power efficiency compared to [6]. In [11], a run-time control of the effective signal bit-width by configurable truncation of the LSBs in an OFDM receiver is presented. The conventional truncation in two's complement arithmetic has a different impact on positive and negative numbers. We exploit a different bit-width control technique, that avoids the shortcoming with the conventional truncation.

III. Adequate Demodulator

Baseline Demodulator Design: The baseline design is described in [10]. The structure of the original design is as illustrated in Fig. 2. This demodulator operates on 8 MHz sampling frequency. The original design is modified to have a state-of-the-art dual stage poly-phase decimation filter as described in [8]. The modifications provide more power-efficient classical operation as indicated in the results section. The modified demodulator is illustrated in Fig. 3. The FIR filters PF1 and PF2 are in total less complex than the original FIR filter and operate with lower clock frequency, with the same filtering performance. Without loss of generality, the bit-width of the design inputs is chosen to be 12-bit. This design is modeled in Python for Symbol Error Rate (SER) estimation, and implemented in a commercial 40-nm CMOS technology for power estimation. The SER and power values of this design are used as the reference for the evaluation of the adequate demodulator advantages.

To be able to trade off the demodulation performance for power savings, three different techniques are investigated in this work as follows:

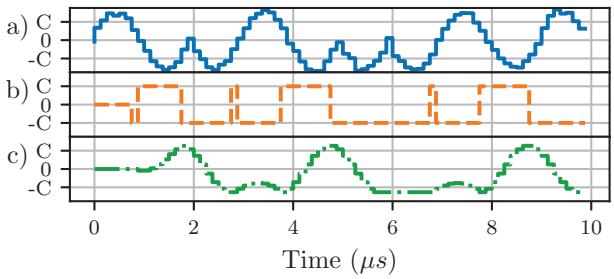

Fig. 4. The BCA effect: the original signal a) is degraded with BCA b) and interpolated back with FIR c).

- Bypassable Comparator Approximation (BCA),
- Bypassable Filter Approximation (BFA),
- Discard of In-phase signal Approximation (DIA).

Bypassable Comparator Approximation: With BCA, every sample of the signal is replaced according to the mapping rule represented in (1).

$$Y = \begin{cases} C, & \text{if } X >= 0 \\ -C, & \text{otherwise} \end{cases} . \quad (1)$$

X and Y are input and output vectors, respectively, of the digital signal. C is a constant which can be properly set to reduce the switching activity in the following computational chain. From the view of the CMOS circuit design, the power consumption can be reduced by decreasing the circuit switching activity. That is achieved through maximizing the number of zeros in the binary representation of C. In this work, we use $C = 2^{(N-2)}$, where N is the bit-width of a two's complement number representation. The values for C thus are $C = 01000...{}_2$ and $-C = 110000...{}_2$, so that both C and $-C$ have an equal maximal number of zeros. The consequence of this choice is that the effective bit-width of the signal is reduced to one, and the signal magnitude information is lost. However, in case of O-QPSK, the information carrier is the signal phase, which can still be recovered from the signal even with an effective bit-width of 1. Furthermore, if applied before the decimation step on the over-sampled signal, the signal can be partially recovered by the decimation filter, through interpolation. The operational principle of BCA is shown in Fig. 4. The original signal is illustrated in Fig. 4(a). This signal is distorted through BCA, resulting in the waveform illustrated in Fig. 4(b). However, after FIR filtering, the essential parts of the waveform are reconstructed. Successful demodulation therefore can still be performed. For the cases where the sensitivity is critical for successful signal demodulation, the performance degradation through BCA might be catastrophic. For those cases, the comparator can be bypassed. The generic circuit representation of BCA is illustrated in Fig. 5. In the

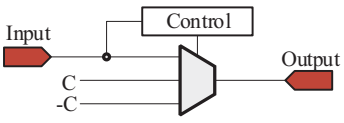

Fig. 5. Bypassable Comparator Approximation (BCA) circuit.

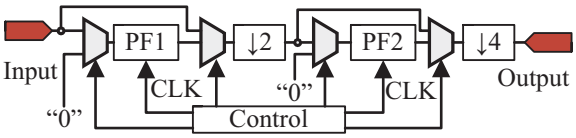

Fig. 6. Bypassable Filter Approximation.

control block, it is decided if the sample is replaced by C or $-C$, or forwarded without any change.

Bypassable Filter Approximation: The advantage of multi-stage decimation filtering is that the filtering performance is distributed over several stages. This property can be used to trade excessive filtering performance for power. With Bypassable Filter Approximation (BFA), every decimation stage is made bypassable. The proposed and implemented BFA structure is illustrated in Fig. 6. The bypassed filter parts are clock and input gated so that the power consumption is reduced by reduced switching activity. The control block configures the bypassing multiplexers and clock gating. The degradation impact of BFA is increased aliased noise, which is transferred to the baseband after decimation. The noise degradation caused by BFA is illustrated in Fig. 7. If that noise is sufficiently low, BFA provides an opportunity to save power. To enable separate BFA control in the I and Q chains, additional synchronization circuitry is necessary. For example, if PF1 of the I chain is bypassed, the signal arrives faster due to bypassed filter pipeline latency. As a consequence, the correlator and I-Q correlation become desynchronized and sensitivity degrades significantly. To keep the synchronization overhead low, only the I path is synchronized to the bypassed Q path configurations. To synchronize Q-only BFA, the delay element in the I chain is exploited. In O-QPSK demodulation, the I path needs to be delayed to compensate for the offset of the Q path at the transmitter. This delay element is used to compensate for the timing mismatch in I and Q chains due to bypassed filters in the Q chain.

Discard of In-Phase Signal Approximation: Another technique to trade off the demodulator sensitivity for power is discarding the I chain, which starts from I in Fig. 3. The consequence is that the information from the I path is discarded. Only one bit of the O-QPSK symbol can be recovered. However, because of the DSSS code robustness, the encoder

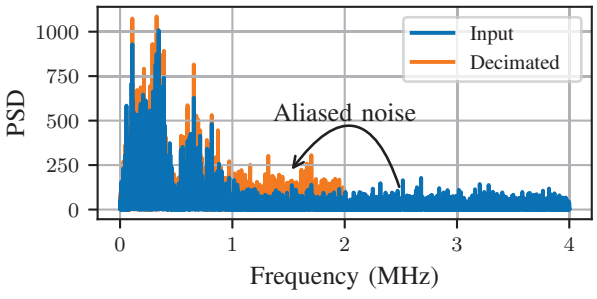

Fig. 7. The BFA impact on the signal Power Spectral Density (PSD): with bypassed filter, the noise is aliased into the baseband spectrum.

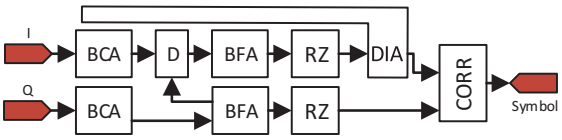

Fig. 8. Adequate demodulator design.

is still capable of recovering the original data if the signal to noise ratio is sufficiently high. The technique can be seen as a special case of the under-sampling technique presented in [7]. In contrast to [7], however, the focus of this work is on the whole demodulator instead of only the DSSS correlator. The demodulation with the signal separation in In-phase and Quadrature parts effectively decreases the minimum sampling frequency by a factor of 2. Instead of detecting the phase shifts of $\pi/2$ in the original signal, bigger phase shifts of π can be detected more easily in I and Q components, separately. Processing only one of the components can be seen as signal decimation or under-sampling by a factor of 2. In the IEEE 802.15.4 O-QPSK radio, the I and Q signals contribute to the odd and even bits, respectively, in the DSSS code. The bits in DSSS code words are also called chips. The sequence of 32 chips is interpreted as one symbol. There are 16 different symbols in total. The symbols also can be recovered from 16-chip long sequences using only the Q path information sacrificing noise rejection ability. If the remaining noise rejection is still sufficient for the current channel condition, power savings close to 50% for the whole demodulator can be achieved by sparing the I path computation.

Combination and Co-design of Techniques: For a fine-grained trade-off, all three above mentioned techniques are combined in a single system. For analysis, all possible BFA, BCA, and DIA combinations are investigated. According to the analysis results, the circuitry is simplified by keeping only Pareto-optimal configurations. It is necessary because the techniques are not orthogonal to each other. For example, the BCA impact depends on the filter performance so that simultaneous application of BCA and BFA results in less power savings for more performance penalty. The design of the adequate demodulator is illustrated in Fig. 8. BCA is placed at the beginning of the computation chain as BCA relies on the following filtering performance. The BFA block is placed after BCA. DIA technique is applied to the In-phase path. If DIA is enabled (Ioff), the whole I chain is input and clock gated while the correlator receives constant predefined values from the I chain. All possible configurations per technique are listed in Table I. DIA has only two modes: Ion and Ioff. BCA has four modes: in CB all comparators are bypassed; in CI only comparators in the Q chain are bypassed; in CQ only comparators in the I chain are bypassed; and in CIQ all comparators are enabled. BFA has seven modes: all filters enabled (FA), bypassed filters on Q chain (FQ1, FQ2, FQ3), or bypassed filters on both I and Q chains (FIQ1, FIQ2, FIQ3). The numbers indicate if only the first stage (FQ1, FIQ1) or the second stage (FQ2, FIQ2) or both stages (FQ3, FIQ3) are bypassed. In FA all filters are enabled. Together, there are $4 \times 7 = 28$ configuration points for Ion and $4 \times 4 = 16$ configurations for Ioff (=44 in total). In the rest of this work, we refer to any configuration point in the form of a tuple. For example, (Ion, CB, FA) is a configuration with enabled I-chain, bypassed comparator, and all filters enabled (this is the combination with best sensitivity).

TABLE I
POSSIBLE CONFIGURATIONS OF THE ADEQUATE DEMODULATOR.

DIA	BCA	BFA
Ion	CB (BCA is off)	FA (BFA is off)
Ioff	CI (BCA at I)	FQ1, FQ2, FQ3 (BFA on Q)
	CQ (BCA at Q)	FIQ1, FIQ2, FIQ3 (BFA on I, Q)
	CIQ (BCA at I, Q)	

IV. Adaptive Demodulator Evaluation

Analysis and Implementation Flow: The proposed design and the reference design are modeled in a Python environment for sensitivity calculation, and synthesized in a commercial 40-nm CMOS technology to estimate the realistic power values. The diagram of the used analysis flow is illustrated in Fig. 9. The HDL description of the design is first verified against the Python model in a MyHDL [12] co-simulation. Then sensitivity and power are computed using the simulation at the signal level with the Python model and the RTL level with the RTL description, respectively, of the proposed design. For the estimation of power and sensitivity, the stimuli are generated using the flow illustrated in Fig. 10. Randomly generated symbols are converted to DSSS chip sequences and modulated to an O-QPSK signal of Magnitude A, and a sampling rate of 8 MHz. Then white Gaussian's noise is added to the signal with a predefined Signal-to-Noise Ratio (SNR). The resulting signal is quantized to the bit-width of 12-bit (including the sign bit) in the digitizer block. To consider all possible scenarios, different stimuli sets are produced with different SNR in a range between -10 and 10 dB and magnitude values in a range of 80% to 0.15% of the maximal value for the signed 12-bit representation. The reported power and sensitivity values are averaged over values estimated for all magnitudes and SNR conditions.

Sensitivity Computation: For the sensitivity computation, the random symbol sequence used for stimuli generation and the symbol sequence produced by the demodulator are compared. The resulting SER-SNR relation can be used for

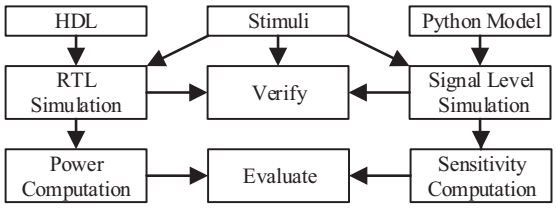

Fig. 9. The design and evaluation flow for the demodulators.

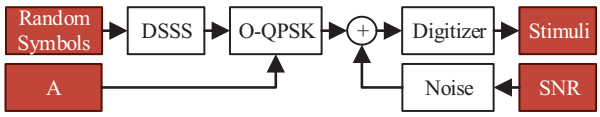

Fig. 10. The stimuli generation flow for sensitivity and power computation.

sensitivity estimation. In this work, the sensitivity is defined as the minimal SNR required to achieve the acceptable SER. According to the IEEE 802.15.4 specification, the tolerable Packet Error Rate (PER) is below $\text{PER}_{\text{max}} = 1\%$. The packets consist of maximum 133 octets which are converted to 266 DSSS symbols, because there are 16 different DSSS symbols (4-bit information). Therefore, the maximum SER (SER_{max}) can be computed with

$$\text{SER}_{\text{max}} = 1 - (1 - \text{PER}_{\text{max}})^{\frac{1}{266}} \approx 3.78 \cdot 10^{-5}. \quad (2)$$

Then the sensitivity is the minimum SNR that results in SER below SER_{max}.

Power Computation: For power computation, the adequate demodulator and reference demodulator are implemented at RTL level. With the MyHDL package, the RTL level description can be matched with the Python model in a co-simulation. After verification, the RTL simulation is performed to estimate the switching activity of the design at the RTL level. This switching activity is used for power estimation in Cadence Joules [13] through internal synthesis and technology mapping. This power estimation method is compared to conventional back-annotated gate-level simulation. The difference in results is below 1%. Therefore, these power values are used for the final evaluation.

Evaluation Results: After showing the sensitivity and power results of some selected configurations, which are discussed in more detail, the final combined power versus sensitivity results are presented.

Sensitivity Results: The sensitivity of the reference design is the same as that of the sensitivity of the original design [10] and the proposed adequate demodulator in (Ion, CB, FA) mode (-5.2 dB). The sensitivity estimation for this and a few other modes is illustrated in Fig. 11 as an example.Furthermore, the best SER performance of the design from [5] and [6] is plotted for reference. Further improvement of sensitivity can be achieved through higher sampling frequency and more filtering which is however not the focus of this work. Instead, it is shown how to trade sensitivity for power savings if it is not needed due to good signal quality at the given point in time. If BCA is enabled at both I and Q paths (Ion, CIQ, FA), the sensitivity drops to -3.3 dB. For the configuration of (Ion, CB, FIQ1), the sensitivity is -1.5 dB which is close to the sensitivity of (Ioff, CB, FA). The simulations in Fig. 11 are performed under signal magnitude of 40% of the maximum range. Assuming there are other signal magnitudes in the real application scenarios, the sensitivity is computed and averaged over the range of magnitudes from 80% to 0.15%. Because

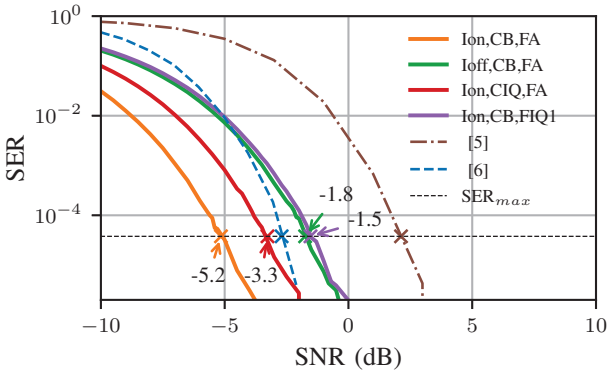

Fig. 11. Sensitivity calculation for several example configurations and the works from [6] and [5] at 40% of the maximum signal magnitude.

of quantization effects for smaller signal and overflow effects for bigger signals, the average maximum sensitivity value decreases to approximately -4.6 dB. Accordingly, the sensitivity for all other configurations is estimated. Note that the signal overflow effect varies with the approximation technique. BCA shows the best robustness against overflow effects with a good choice of constant C.

Power Results: As the base implementation, the design from [10] (Fig. 2) is modified to a dual-stage poly-phase FIR structure (Fig. 3) to increase power efficiency. The resulting design is used as a reference for the evaluation of the proposed approximation techniques. The power estimation of the adequate demodulator with few configuration modes together with the original design (ORIG), the design from [6] and used reference (DPFIR) are plotted in Fig. 12. The modification of the filters to a dual-stage poly-phase structure (DPFIR) results in a significant power-efficiency improvement of over 32% compared to ORIG and the design from [6]. The power consumption of the adequate demodulator in (Ion, CB, FA) configuration is slightly bigger than the reference because of additional multiplexers for the bypassing. In this mode, the sensitivity of the adequate demodulator is equal to the sensitivity of the reference design and original design. All

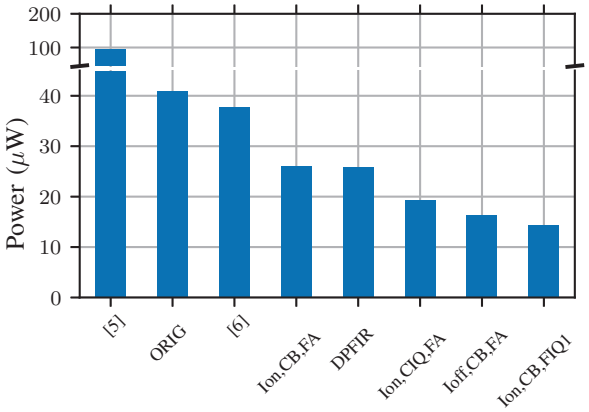

Fig. 12. Power consumption of the adequate demodulator, original demodulator (ORIG), demodulators from [5], [6], and dual stage poly-phase filter modification (DPFIR).

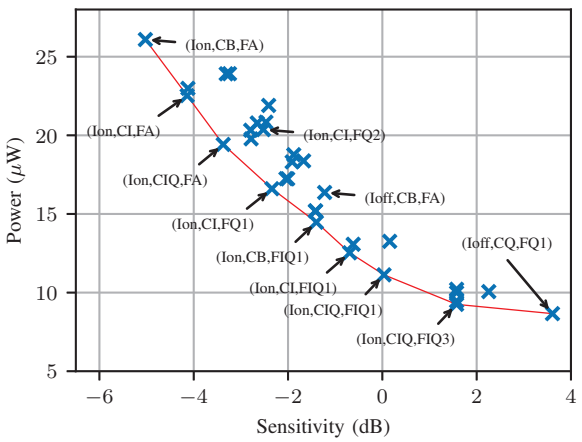

Fig. 13. Sensitivity-power trade-off with the adequate demodulator.

other configurations, such as (Ioff, CB, FA), consume less power than the original design. The power savings are 36% for (Ioff, CB, FA), 24% for (Ion, CIQ, FA), and 44% for (Ion, CB, FIQ1) compared to DPFIR in Fig. 12. The power is estimated in this way for all possible configurations of the adequate demodulator.

Sensitivity vs Power: Finally, the estimated sensitivity and power values are combined to qualify the desired trade-off. The sensitivity and power consumption of all possible configurations are plotted in Fig. 13. Some of the configuration points are sub-optimal and do not need to be provided in the final implementation. For example, the BFA configurations FI2, FIQ2, and FQ2 do not provide significant power savings. The mode (Ion, CI, FQ2) is inferior to (Ion, CI, FQ1). This is because in those configurations the last stage of the filter (PF2 in Fig. 3) is bypassed which works on a low clock frequency and its power contribution is less significant compared to the front filter stage. The configuration (Ion, CB, FIQ1) also consumes less power than (Ioff, CB, FA) while its sensitivity is similar. (Ioff, CQ, FQ1) may not be useful as significant sensitivity is sacrificed for marginal power savings compared to (Ion, CIQ, FIQ3). To keep the overhead of the approximation control multiplexers small, only the Pareto set is implemented. This results in the performance illustrated in Fig. 1 with eight operating modes giving power saving-sensitivity trade-offs from 15% power reduction for 1 dB to 64% power reduction for 7dB. Those operating modes with reduced sensitivity can be enabled at deployment or run-time when channel conditions are better than the worst case. This results in less energy needed for packet transmission and extended battery life for IoT devices. Note, the run-time adaptation needs a low-overhead sensing and control mechanism, e.g., based on RSSI.

V. Conclusion

In this work, we propose an *adequate* IEEE 802.15.4 conformant demodulator, which enables the trade-off between power and sensitivity. The trade-off can be configured at deployment or run-time if the channel quality information is available. The adequate demodulator is implemented in a commercial 40-nm CMOS node for power analysis and Python for fast sensitivity analysis. The power-sensitivity trade-off is implemented with a combination of three proposed run-time approximation techniques, namely Bypassable Comparator, Bypassable Filter, and Discard of In-phase signal approximations. Those techniques effectively trade excessive transceiver sampling frequency, bit-width, and filtering performance for power savings. The results show that up to 64% power savings can be achieved by exploring the channel quality variation over time with the proposed adequate demodulator. As the next step, we plan to develop a fully run-time adaptive demodulator that adapts on the fly to changing channel conditions.

Acknowledgment

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