Lightweight Thermal Monitoring in Optical Networks-on-Chip via Router Reuse

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***Abstract*—Optical network-on-chip (ONoC) is an emerging communication architecture for manycore systems due to low latency, high bandwidth, and low power dissipation. However, a major concern lies in its thermal susceptibility – under on-chip temperature variations, functional nanophotonic devices, especially microring resonator (MR)-based devices, suffer from significant thermal-induced optical power loss, which potentially counteracts the power advantages of ONoCs and even cause functional failures. Considering the fact that temperature gradients are typically found on many-core systems, effective thermal monitoring, performing as the foundation of thermal-aware management, is critical on ONoCs. In this paper, a lightweight thermal monitoring scheme is proposed for ONoCs. We first design a temperature measurement module based on generic optical routers. It introduces trivial overheads in chip area by reusing the components in routers. A major problem with reusing optical routers is that it may potentially interfere with the normal communications in ONoCs. To address it, we then propose a time allocation strategy to schedule thermal sensing operations in the time intervals between communications. Evaluation results show that our scheme exhibits an untrimmed inaccuracy of 1.0070 K with low energy consumption of 656.38 pJ/Sa. It occupies an extremely small area of 0.0020 mm^2, reducing the area cost by 83.74% on average compared to the state-of-the-art optical thermal sensor design.**

I. Introduction

Optical network-on-chip (ONoC) [1], [2] offers an attractive solution to satisfy the communication bandwidth and latency requirements with low power dissipation, particularly when employing wavelength division multiplexing (WDM) technology. However, this architecture is highly susceptible to chip temperature fluctuations. Under large thermal variations, functional nanophotonic devices, especially microring resonator (MR)-based devices, suffer from significant thermal-induced optical power loss, which may counteract the power advantages of ONoCs and cause bandwidth loss and even functional failures [3].

Chip temperature fluctuates temporally and spatially as a result of uneven chip power density and limited heat dissipation techniques [4]. Considering the typical 3D-stacked structure of ONoC-based chips [5], where optical routers are neatly placed at the top surface of the processor cores, large thermal gradients are caused in ONoCs. Extensive thermal-aware management techniques on ONoCs have been proposed from the system level down to the device level, such as thermal-balance task allocation techniques [6], thermal-sensitive routing mechanisms [2], [5], and control-based solutions compensating for the thermal effect on nanophotonic devices [7], [8]. As the foundation of these thermal-aware managements, accurate, efficient and reliable thermal monitoring is of fundamental importance for ONoCs.

Recent works [9], [10] adopt accurate and low-power MR-based thermal sensors for thermal monitoring on ONoCs. Compared to traditional electronic counterparts, they have favorable properties of natural compatibility with ONoCs, immunity to electromagnetic interference and robustness against mechanical shock and humidity. The well-modeled temperature dependence of MRs makes them practical as well. Work [10] proposed a process variation (PV)-tolerant optical thermal sensor design. Operated by monitoring the thermal-induced optical power losses of cascaded MRs with multiple on-chip lasers and photodetectors (PDs), this latest sensor design achieves effective and reliable temperature measurement with the capability of PV tolerance. However, the main drawback is the heavy area cost. Experimental results show that it averagely increases 11.7% router area to integrate a single PV-tolerant thermal sensor in an optical router. This overhead grows with the increasing number of sensors being integrated.

In this paper, we propose a lightweight scheme for accurate, efficient and reliable thermal monitoring on ONoCs. Our contributions are summarized as follows.

- We first design a thermal sensing module for generic optical routers. It introduces trivial overheads in chip area by reusing the components in routers. A major problem with reusing optical routers is that it may potentially interfere with the normal communications on ONoCs, which is not allowed because the routers are designed to communicate between processors.
- To address this problem, we further propose a time allocation strategy to utilize the idle time intervals between communications for thermal sensing operation.
- Evaluation results show that our scheme exhibits an untrimmed inaccuracy of 1.0070 K with low energy consumption of 656.38 pJ/Sa. It occupies an extremely small area of 0.0020 mm^2, reducing the area cost by 83.74% on average compared to the state-of-the-art optical thermal sensor design.

The rest of this paper is structured as follows: Section

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II briefly introduces related preliminaries; Our scheme is proposed in Section III; Performance evaluations are presented in Section IV and Section V concludes this paper.

II. Preliminary

ONoC architecture. We illustrate a typical mesh-based ONoC in Figure 1. 2D-mesh topology has been widely used by chip designers thanks to its simplicity and good scalability. Vertically on top of functional cores, a photonic network provides optical interconnects between optical routers for inter-core data transmission. An electronic network comprised of control routers and metallic interconnects is designed to perform logical control. The photonic and electronic networks together constitute an ONoC. We also provide a popular optical router *Cygnus* [11] as an example.

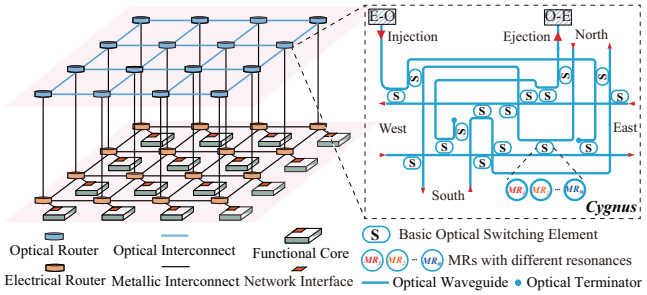


Fig. 1. A mesh-based ONoC architecture with an example optical router.

Conventional routing in ONoCs. An approach of *optical circuit switching* is employed on ONoCs for routing. When a functional core wants to communicate with another one, an electronic '*path-setup*' packet will be sent to the control router from the network interface (NI). When the packet arrives, the control router will route it in the electronic network and attempt to establish an optical path for data transmission. According to the routing information contained in the packet, the control routers internally flag the associated resources as 'reserved' and activate the corresponding basic optical switching elements (BOSEs) in the connected optical routers to establish an optical path. Along the path, bulk data can be transmitted end-to-end without in-flight buffering and processing.

Optical routers. As the core functional component of ONoCs, an optical router is comprised of a transmitter, a receiver and a switching network. The transmitter (i.e., E-O module) converts electrical signals into optical signals. Built-in microlaser sources, such as VCSELs [12], can be implemented in it. The VCSELs are connected with the underlying CMOS drivers using 3D integration technology and through silicon via (TSV) technique [13]. A preamplifier (PA) and a current mode logic amplifier (CMLA) are included in each CMOS driver for signal modulation. The output power of VCSELs is directly modulated by the driving current without optical modulators. The optical receiver (i.e., O-E module) uses high-resolution PDs [14], [15] to convert optical signals into electrical signals. Absorbed photons will cause photo-induced current carriers in the depletion region of PDs. A transimpedance amplifier (TIA) and a limiting amplifier (LA) are included for current-to-voltage conversion and voltage amplification, respectively [16]. Before optical signals reaching the PDs, a basic optical filtering element (BOFE) constituted by cascaded MRs is used in the receiver to demultiplex the WDM wavelengths. Between the transmitter and the receiver, BOSEs and waveguides compose an optical switching network, which performs the switching and transmission of optical signals, respectively. We illustrate the schematic structure of generic optical routes in Figure 3(a) and provides an example router *Cygnus* in Fig. 1.

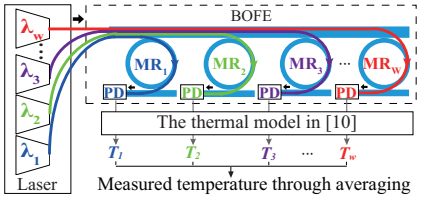


Fig. 2. The PV-tolerant optical thermal sensor design in [10].

The PV-tolerant optical thermal sensor design. As shown in Figure 2, a PV-tolerant thermal sensor is comprised of three parts: a multi-wavelength laser source, a BOFE, and multiple PDs. The MRs in the BOFE filter out their own designated resonant wavelengths from the input wavelengths, demultiplexing the W wavelengths before the optical signals reaching the PDs. For a single MR, we can derive a predicted temperature value according to the well-modeled temperature dependence of MRs formulated in [9], [10], which models the relation between the thermal-induced optical power loss of a MR and its ambient temperature. The details of this model refer to [10]. Utilizing the 'hidden' redundancy in WDM technology, for a BOFE, multiple predicted temperature value can be derived (e.g., T_1, T_2, ..., T_W in Figure 2). Extensive simulation results show that the PVs among MRs are random and follow Normal distribution [3]. When using the MRs for thermal sensing, the temperature errors caused by PVs may potentially cancel each other out with an average value of approaching zero. The impact of PVs on measurement accuracy is largely reduced (or even counteracted) by using the average value of the predicted temperatures as the measured temperature. With the ability to PV tolerating, this design enhances the monitoring accuracy and reliability of the prior optical thermal sensors. However, a main drawback is the heavy overheads of extra hardware resources (including on-chip lasers, BOFEs, and PDs) and chip area. Experimental results based on five typical optical router designs show that it averagely increases the router area by 11.7% when integrating a single PV-tolerant thermal sensor in a router, which grows with the increasing number of integrated sensors. To reduce the total overheads for on-chip thermal monitoring, we propose a lightweight thermal monitoring scheme in the next section.

III. Lightweight Thermal Monitoring Scheme by Adding TS Link and TS Arbiter

In this paper, we consider WDM-based ONoCs with 2D-mesh topology as the target platforms, where optical routers

are evenly distributed across the networks[1]. In these cases, optical routers are suitable to be used for ONoC temperature monitoring because it facilitates the run-time temperature monitoring of different network regions based on a fine granularity of one sensor-per-router.

The thermal sensor proposed in [10] can be built and implemented as a stand-alone module. We can place it in optical routers for temperature monitoring on ONoCs. To show the additional area overhead introduced by integrating a sensor into routers, we have conducted an experiment based on multiple typical optical routers, including [17]–[20] and *Cygnus* [11]. Table I presents the router areas with and without an integrated thermal sensor. It shows that, if integrating a dedicated thermal sensing module for each optical router, the router area will increase by 11.7% on average. This problem is more acute in small-size routers. These designs are originally based on single-MR-based switching elements. In this experiment, we have extended their structures using eight-MR-based switching elements and conservatively estimated their areas.

TABLE I
THE AREA OVERHEAD OF TYPICAL ROUTERS CAUSED BY INTEGRATING A SINGLE THERMAL SENSOR IN [10]

Router	# ports	# MRs	Area (mm^2) **w/o** sensor	Area (mm^2) **w/** a sensor	Avg. %(Area)
[17]	4	4×8	0.0312	0.04351	↑ **11.7%**
[18]	4	8×8	0.1058	0.1181	
[19]	5	8×8	0.5852	0.5975	
[20]	5	16×8	0.3511	0.3634	
Cygnus [11]	5	16×8	0.6600	0.6723	

Motivated by the fact that multi-wavelength laser sources already exist in optical transmitters, and BOFEs and PDs are existing components in optical receivers, in this section, we propose a lightweight thermal monitoring scheme for ONoCs by reusing the optical routers spatially and temporally. We first propose a thermal sensing module for generic optical routers. By reusing the components in routers, it introduces trivial overheads in chip area and hardware when performing thermal sensing. We then identify the problem with reusing optical routers is that, it may potentially interfere with the normal communications in ONoCs. A time allocation strategy is further presented to schedule the thermal sensing operation in the time intervals between communications.

A. Thermal sensing module for generic optical routers

Overview. Figure 3(a) illustrates a schematic view of generic optical routers. We extend the structure of generic routers by adding an optical link and an optical arbiter to implement **T**hermal **S**ensing operations, shown in Figure 3(b). We call them TS link and TS arbiter, respectively. For clarity, We illustrate the extended structure of the router *Cygnus* in Figure 3(c). TS link connects the E-O module and the O-E module directly. TS arbiter is designed to decide whether to conduct inter-core communication or to perform temperature sensing for the router. If normal communication is performed, TS link can be perceived as disconnected and the bulk data will be injected into the optical switching network for transmission. By contrast, if temperature measurement is performed, a small amount of data will be transmitted along the TS link from the transmitter to the receiver for performing thermal sensing. By reusing the laser sources in the transmitter, and the BOFE and PDs in the receiver, we can conduct temperature measurement in every optical router. Consequently, thermal monitoring for the ONoC is implemented.

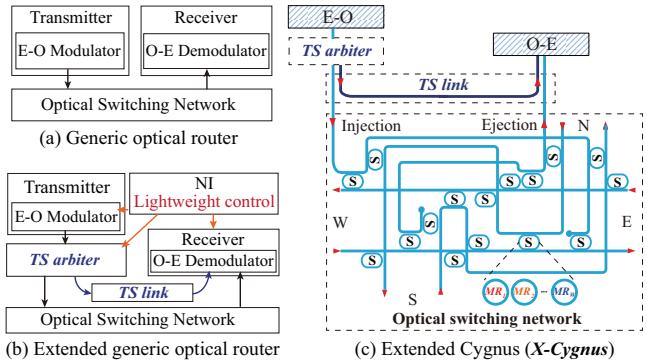


Fig. 3. Overview of the proposed thermal monitoring scheme.

TS Link and TS Arbiter. As shown in Figure 3(c), the TS link is essentially an optical waveguide that connects the transmitter and the receiver. As illustrated in Figure 4, TS arbiter is an optical switch (essentially a BOSE variant) constituted by cascaded MRs. When all the MRs in the TS arbiter are configured to be switched off, the optical signals from the *Input* port will be delivered to the Out_{off} port simultaneously. Otherwise, the optical signals are resonated into the rings and delivered to the Out_{on} port. This arbiter is at OFF state by default and will be activated when performing thermal sensing operations. If the arbiter is passive, the TS link can be perceived as disconnected. Under precise control, TS arbiter can guarantee reliable communications with trivial influences.

Control in NI. Lightweight controls are added in the NI to perform arbitration. We add two judgment instructions to distinguish the requests and data for thermal sensing (i.e., TS requests and TS data) from those for communication. We can simply add a new packet (or flit) type, *TS*, and label the type field of a packet (or flit) as *TS* if it is used for thermal sensing. In this way, the NI can determine the type of requests and data with negligible overhead.

Workflow. We illustrate the workflow of our scheme in Figure 4. When a NI receives a request from the functional core, it will determine what type of request it is. If it is a communication request, the NI will send a '*path-setup*' packet to the control router. The control router then routes the packet and establishes a proper optical path for inter-core communication. When the communication data are ready to be transmitted, they

[1]Our scheme is also applicable to ONoCs based on other direct network topologies, in which each optical router is connected to a functional core and is evenly distributed across the chip, such as torus, folded-torus, etc.

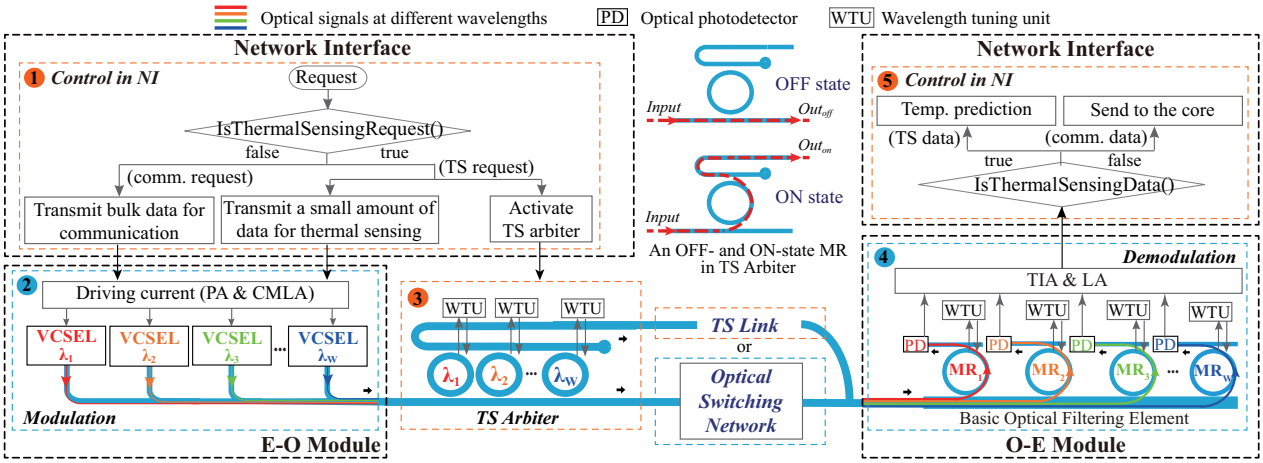


Fig. 4. The workflow of our thermal monitoring scheme. The operations in the blue dotted boxes represent the typical operations in the E-O and O-E modules while those in the orange dotted boxes are newly added by our scheme for thermal sensing implementation. (PA: preamplifier; CMLA: current mode logic amplifier; TIA: Transimpedance amplifier; LA: Limiting amplifier)

will be sent to the laser drivers to perform optical modulation. This process is the same as normal communications. While if a thermal sensing (TS) request is received, the NI will activate TS arbiter and a small amount of optical data will be sent from the laser source in the E-O module to the PDs in the O-E module, along the TS link. The BOFE in the O-E module would demultiplex the incoming W wavelengths before the optical data reaching the PDs. Similarly, after receiving the optical data, the NI will distinguish what type of date it is. If the data is used for inter-core communications, it would be send to the functional core. Otherwise, it will be used for temperature estimation by employing the thermal model proposed in [10].

B. Time allocation strategy

As optical routers are intended for inter-processor communications, it is not allowed to interfere with communications when reusing the routers to perform thermal sensing. To resolve the time conflict between them, we present a time allocation strategy here.

We give priority to inter-core communications for guaranteeing ONoC performance, and the thermal sensing operation will be scheduled in the idle time intervals between communications. This strategy guarantees the compatibility of our scheme with normal communications.

Two factors support the feasibility of our strategy. On the one hand, the proposed scheme achieves a high sampling rate. For a sampling operation, a TS data will be transmitted from the laser source to the receiver side, passing through a TS arbiter, a TS link, and the BOFE at the receiver end. We assume a TS-data packet is 512 bits which is the average size of payload data in ONoCs [21]. As all of the associated components achieve a transmission rate of higher than 25 Gbps, plus the time that takes for lightweight control in the NI, it costs around 30 ns to complete a sampling operation. Assumed that the sampling span is 10 ns, the sampling rate of our scheme is up to 25000 kSa/s.

On the other hand, chip thermal profiles take hundreds of milliseconds to change [22]. Before the next change, on-chip temperature distribution will be in relatively steady-state over a period of time. We define this time interval as a time window in this work, which is in the range of hundreds of milliseconds. The time required for inter-core communications and the sampling time need by our scheme are both in the range of nanoseconds, which is several orders of magnitude smaller than a time window. Therefore, for a router that is communicating, it is feasible to wait for communications to complete and then perform thermal measurements in the idle time intervals between communications. We can obtain the temperatures of all the routers within the same time window, with trivial measurement accuracy degradation. In addition, chip temperature potentially tends to peak when the inter-core communication is idle because the processor cores are performing computation during this period of time. It helps to capture the high temperature for ONoCs. To sum up, this strategy enables ONoC thermal monitoring without interfering with the routers intended purpose of communication.

IV. Evaluation

Compared to conventional communications between processor cores, there are two extensions in our scheme, which may cause design overheads. First, in order to reuse the components in optical routers for thermal sensing, we have added a TS link and a TS arbiter in each router. It introduces extra area. Second, the operation of temperature measurement consumes power. Besides, the temperature measurement accuracy is of importance as well.

In this section, we analyze and evaluate the characteristics of our scheme (including area cost, power consumption, and monitoring accuracy), and further compare it against the latest optical thermal sensor in [10] and multiple advanced CMOS-compatible electrical sensors. Table II lists the conservative parameters of the associated components used in the proposed

scheme. We consider WDM-based ONoCs that support eight wavelengths as target platforms in this work.

Area Cost. The thermal sensor proposed in [10] is comprised of eight on-chip VCSELs, one BOFE, eight PDs and their associated control circuits. Each occupies 0.0123 mm^2 of silicon area. By contrast, our scheme reduces area cost by reusing the laser sources in the transmitter, and the BOFE and PDs in the receiver. With a negligible-footprint TS link and a compact TS arbiter, the silicon area required by our scheme is only about 0.0020 mm^2. An average of 83.74% area reduction is achieved.

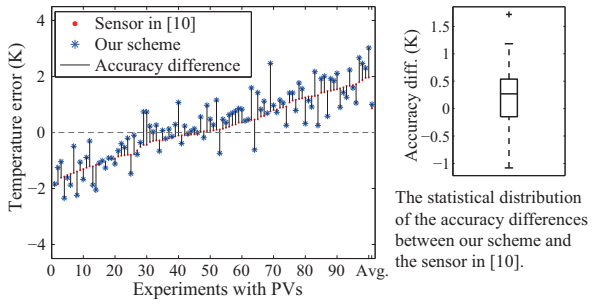
TABLE II
OUR SCHEME: AREA AND POWER

Component	Parameter		
VCSELs + PA&CMLA	Area	0.0053 mm^2 [15]	
	Power	25 mW [12]	
	Transm. rate	25 Gbps [12]	
PDs + TIA&LA [14], [15]	Area	0.0056 mm^2	
	Power	4.25 mW	
	Transm. rate	25 Gbps	
Eight-wavelen. BOFE [10]	MR	Radius	5+0.008×(n-1) μm (1≤n≤8, n∈ N^+)
		Cross-section	400 nm×180 nm
		Coupling gap	100 nm
		Adjacent MR spacing	5 μm
	Area	0.0014 mm^2	
	power	1.4 mW	
	Transm. rate	25 Gbps [23]	
TS link	Area	0.4×10^{-6} mm^2 [10], [24]	
TS arbiter	MR [10]	Radius	5+0.008×(n-1) μm (1≤n≤8, n∈ N^+)
		Cross-section	400 nm×180 nm
		Coupling gap	100 nm
		Adjacent MR spacing	5 μm
	Bend radius	2.5 μm [25]	
	Area	0.0020 mm^2	
	Power	1.4 mW [21]	
	Transm. rate	25 Gbps [23]	

Scheme	Power	Area
Sensor in [10]	30.65 mW	0.0123 mm^2
Our scheme	32.05 mW	∼0.0020 mm^2

Power Consumption. To perform thermal sensing, both the sensor in [10] and our scheme consume power, mainly including the power required by i) the VCSELs and the driven circuits to modulate a small amount of TS data; ii) TS arbiter activation; iii) the PDs and the receiver circuits to demodulate the TS data. Note that the operation of temperature prediction is typically performed in the functional cores. The power consumption of a processor core is determined by multiple factors such as manufacturing technology, operating frequency/voltage level, and working temperature that significantly affects the core's leakage power. We take no account of this part of power overhead for simplicity. In addition, as the time complexity of the temperature prediction operation is $O(1)$, the power consumed by the processors is trivial. Note that TS link is a passive optical component. Our scheme introduces only 1.4 mW more power to activate the TS arbiter than the sensor in [10].

Monitoring Accuracy. We conduct 100 groups of experiments to test the monitoring accuracy of our scheme, by comparing the measurement errors with the optical thermal sensor proposed in [10]. To simulate the associated photonic components and integrated circuits, we use Lumerical FDTD [26] and INTERCONNECT [27] simulation infrastructure. The cascaded MRs in an eight-wavelength BOFE have radii of 5+0.008×(n-1) μm (1≤n≤8, n∈ N^+). The coupling gaps between the waveguides and ring are 100 nm. The TS link is simulated as a 1 mm-length SOI waveguide because the silicon die sizes are usually in the order of 10 mm×10 mm [24]. The TS arbiter has the same parameters as the BOFE's. The bend radius of the bending waveguide in the arbiter is 2.5 μm, similar to the structure in [25]. All of the photonic components have a cross-section of 400 nm×180 nm. The PVs among them are characterized using Normal distribution with a standard deviation of 1.3 nm in waveguide width. In every group of experiment, the waveguide width of the TS link and those of the MRs in the BOFE are all randomly generated and follow Normal distribution, $N(400, 1.3^2)$. To separate normal communication processes and temperature measurement operations to ensure that they perform independently, the TS arbiter acts as an approximately-ideal switch. Therefore, the PVs in the arbiter would have been overcome by employing post-fabrication calibration and local wavelength tuning [7]. It guarantees the communication performance of ONoCs but consumes extra power, which has been taken into account in Table II. Given a random simulation temperature within the range from 300 K to 380 K (similar to the experiment setup in [10]), we can obtain the temperature errors of the two techniques.



The statistical distribution of the accuracy differences between our scheme and the sensor in [10].

Fig. 5. Accuracy comparison between our scheme and the sensor in [10].

As shown in Figure 5, the red dots and the blue asterisks are the measurement errors of the sensor in [10] and our scheme, respectively. The black lines represent their differences. The average measurement errors of the two schemes are 0.8650 K and 1.0070 K, with a difference of only 0.1420 K. We further present a box-and-whisker diagram to display the statistical distribution of the accuracy differences between them. An average accuracy difference of 0.4774 K is shown.

Comparison with advanced CMOS-compatible thermal sensors. To gain an intuitive understanding of the advantages

of the proposed scheme, we further compare it against multiple advanced CMOS-compatible thermal sensors.

As shown in Table III, CMOS-compatible electronic thermal sensors can be divided into three categories based on their basic operating principles: bipolar junction transistor (BJT), metal-oxide-semiconductor field-effect transistor (MOSFET) and electro-thermal filters (ETFs). Generally, ETFs achieve higher accuracy and lower cost compared with transistor-based sensors (including BJTs and MOSFETs) because they are less sensitive to leakage current, process spread, and the mechanical stress of packaging [28]; while the transistor-based sensors have advantages of high efficiency and low power dissipation. Compared to BJTs, the temperature dependence of MOSFETs is well modeled and have lower energy consumption, but it involves higher costs for calibration than do BJTs. It can be observed that our scheme outperforms the electronic designs and achieve effective and reliable thermal measurement.

TABLE III
PERFORMANCE COMPARISON OF THE PROPOSED SCHEME WITH ADVANCED CMOS-COMPATIBLE THERMAL SENSORS

Category	Electrical schemes			Optical schemes	
	BJT [29]	MOSFET [30]	ETF [31]	Sensor in [10]	Our scheme
Inaccuracy (K) (w/ PVs)	< 5	± 2.3	$\pm$ 1.4	0.8650	1.0070
Area (mm^2)	0.02	0.0082	0.0017	0.0123	$\sim$ 0.0020
Sampling rate (kSa/s)	1.2	> 45	1	25000	25000
Energy (pJ/Sa)	1.6×10^{6}	3.4×10^{3}	2.5×10^{12}	627.71	656.38

V. CONCLUSION

In this paper, we have proposed a lightweight scheme to perform accurate yet low-power thermal monitoring on ONoCs. Spatially, by reusing the components in ONoCs, it introduces trivial overheads in chip area. Temporally, a time allocation strategy is employed in our scheme to schedule thermal sensing in the time intervals between communications, such that it will not interfere with the normal communications in ONoCs. Evaluation results verify the favorable properties of the proposed scheme. Our design is now under architecture level, and we aim to make a more practical investments on its prototype realization at both device and system levels in the near future.

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