Symmetry-based A/M-S BIST (*SymBIST*): Demonstration on a SAR ADC IP

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***Abstract*— In this paper, we propose a defect-oriented Built-In Self-Test (BIST) paradigm for analog and mixed-signal (A/M-S) Integrated Circuits (ICs), called symmetry-based BIST (*SymBIST*). *SymBIST* exploits inherent symmetries into the design to generate invariances that should hold true only in defect-free operation. Violation of any of these invariances points to defect detection. We demonstrate *SymBIST* on a 65nm 10-bit Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) IP by ST Microelectronics.**

I. Introduction

BIST consists in embedding test instruments into the circuit with the aim to facilitate test. BIST can be functional targeting on-chip measurement of performances or defect-oriented targeting the detection of structural defects. Defect-oriented test has gained importance nowadays as it can help reducing test escapes down to sub-ppm levels. It is also a step towards guaranteeing functional safety if it is capable of detecting latent defects, as well as defects that will be triggered in the context of system operation in the field.

In this paper, we present a defect-oriented BIST strategy for A/M-S ICs, called symmetry-based BIST or *SymBIST*. *SymBIST* exploits symmetries into the design so as to build invariant properties whose violation points to defect detection. We demonstrate how *SymBIST* successfully applies to a 65nm 10-bit SAR ADC IP by ST Microelectronics achieving transparency to the operation, low area overhead, low test time, compatibility with 2-pin digital access mechanisms, and high defect coverage.

Existing works on ADC BIST focus on functional BIST [1]–[8]. The main reason for the lack of defect-oriented ADC BIST solutions is the long ADC simulation time, typically in the order of hours, which prohibits a defect simulation campaign. Thanks to the fast test time accomplished by *SymBIST*, and by using the recent mixed-signal defect simulator Tessent®DefectSim by Mentor®, A Siemens Business [9], we are able to run very fast in a automated workflow defect simulation for hundreds of defects and compute defect coverage for the entire IP.

The rest of the paper is structured as follows. In Section II, we provide an overview of the *SymBIST* concept. In Section III, we present the architecture of the SAR ADC IP. In Section IV, we show how *SymBIST* applies to this IP. In Section V, we specify the defect model and we provide an overview of the defect simulator. In Section VI, we present transient simulations and the defect coverage results. Finally, Section VII concludes the paper.

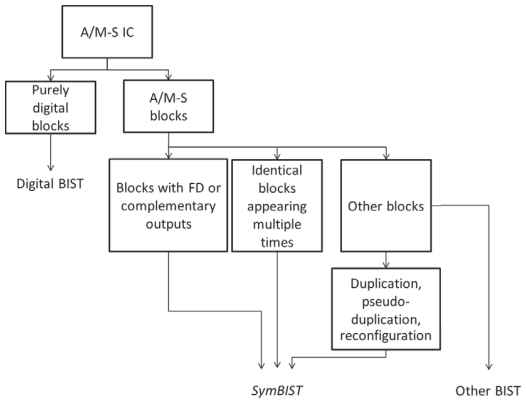

Fig. 1: High-level abstraction of *SymBIST* strategy.

II. *SymBIST* principle

The proposed *SymBIST* paradigm exploits existing symmetries into an A/M-S design and builds invariant properties that should hold true only in defect-free operation.

The underlying observation is that symmetries are inherent to virtually all A/M-S designs. Inherent symmetries exist thanks to fully-differential (FD) signal processing, complementary signal processing, and replication of identical blocks. Symmetries can also be created artificially with reconfiguration using switches, duplication of blocks, or pseudo-duplication of blocks [10], [11]. For example, for node pairs carrying FD or complementary signals we can build an invariance in the form of $V_1 + V_2 = \alpha$, where V_1 and V_2 are the nodes' voltages and α is a constant, i.e., in the case of FD signals $\alpha = 2V\text{cm}$, where $V\text{cm}$ is the common mode voltage [12], [13]. For identical blocks, duplicated blocks, or pseudo-duplicated blocks, we can drive them with the same input and build an invariance in the form of $V_1 - V_2 = 0$, where V_1 and V_2 are the blocks' outputs.

These invariances can be checked with a window comparator circuit implementing a comparison window $[-\delta, \delta]$, $\delta > 0$, to account for process, voltage, and temperature variations. If the invariance is violated, i.e. the invariant signal slides outside the window, then this points to defect detection. The parameter δ can be set to $k \cdot \sigma$, where σ is the standard deviation of the invariant signal computed by a Monte Carlo analysis and k is set accordingly so as to avoid yield loss.

A high-level abstraction of the proposed *SymBIST* strategy is illustrated in Fig. 1. The A/M-S IC is divided into purely digital blocks on one side and A/M-S blocks on the other side. We assume that the purely digital blocks are tested with standard digital BIST, i.e. with scan insertion and a

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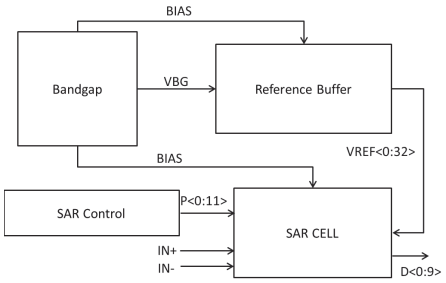

Fig. 2: Top-level architecture of SAR ADC.

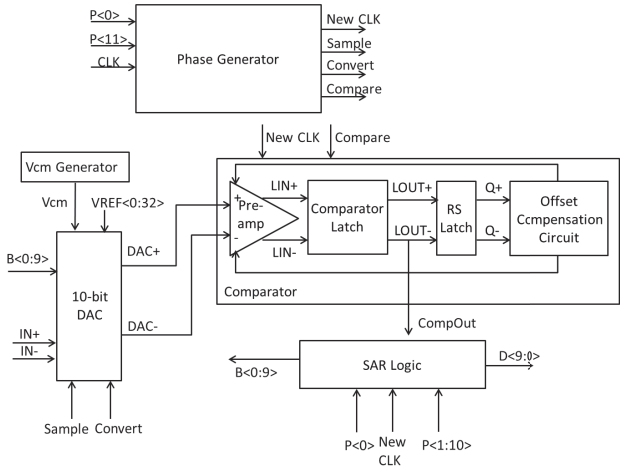

Fig. 3: SARCELL block-level architecture.

combination of stuck-at, bridging, I_{ddq}, and transitional Automatic Test Pattern Generation (ATPG). The A/M-S blocks are divided into three groups. The first two groups include blocks that are FD, perform single-to-FD conversion, provide complementary outputs, appear multiple times, etc. For these blocks invariances exist naturally and the *SymBIST* strategy applies directly. The third group includes the rest of the blocks. For some of these blocks it may be possible to perform reconfiguration or pseudo-duplication so as to apply *SymBIST*. We also have the option to perform direct duplication of blocks. For the remaining blocks that are not treated with *SymBIST*, we need to develop other BIST approaches.

III. Case study: SAR ADC IP

Our case study is a 65nm 10-bit SAR ADC IP by ST Microelectronics. The top-level architecture is illustrated in Fig. 2. The circuit accepts a FD analog input ΔIN=IN$^+$-IN$^-$ and provides a 10-bit digital output D<0:9>. The top-level blocks include:

SARCELL: It is the main block of the ADC which implements the SAR algorithm.

SAR Control: It creates 12 pulses P<0:11> used to control the sampling, conversion, and digital output capture phases in the SARCELL.

Bandgap: It creates the required biasing for all ADC blocks.

Reference Buffer: It creates the comparison levels VREF<0:32> used during the conversion.

The SARCELL block-level architecture is shown in Fig. 3. It includes the following sub-blocks:

10-bit DAC: The DAC sets the comparison level to which the input is compared at each conversion cycle. It has a resistive plus charge redistribution architecture. As shown in Fig. 4, it is composed of two sub-DACs and a switched-capacitor (SC) array. The two sub-DACs, namely SUBDAC1 and SUBDAC2, have 5-bit digital inputs B<5:9> and B<0:4>, respectively, where B<0:9> is the 10-bit digital output of the ADC during the conversion. The sample-and-hold (S&H) operation that keeps the input signal constant during the conversion is performed within the SC array. SUBDAC1 converts the 5 most significant bits (MSBs) B<5:9>, to comparison levels M+ and M-, while SUBDAC2 converts the 5 least significant bits (LSBs) B<0:4> to comparison levels L+ and L-. The Boolean functions implemented by SUBDAC1 and SUBDAC2 are given by:

$$\begin{aligned} \text{M+} &= \text{VREF}[\sum_{i=5}^{9} B_i \cdot 2^{i-5}] \\ \text{M-} &= \text{VREF}[32 - \sum_{i=5}^{9} B_i \cdot 2^{i-5}] \\ \text{L+} &= \text{VREF}[\sum_{i=0}^{4} B_i \cdot 2^{i}] \\ \text{L-} &= \text{VREF}[32 - \sum_{i=0}^{4} B_i \cdot 2^{i}] \end{aligned} \tag{1}$$

Phase Generator: It controls the timing of the operation by generating the phases for sampling, comparison, conversion, etc.

V_{cm} Generator: It generates the common mode voltage V_{cm} used inside the DAC.

SAR Logic: It controls the conversion process by providing the digital input to the DAC, it stores the result of each comparison, and provides the digital output D<0:9>=B<0:9> once the 10 conversion periods are completed.

Comparator: It compares the two outputs of the DAC and the outcome of the comparison is driven to the SAR Logic block in order to set the corresponding digital bit. It comprises a pre-amplifier, a comparator latch, an RS latch, and an offset compensation circuit for the pre-amplifier.

IV. *SymBIST* applied to SAR ADC IP

1) Invariances: Looking into the architecture of the SAR ADC IP, we observe that the two sub-DACs within the DAC are structurally identical, each sub-DAC has complementary outputs, the SC array has symmetrical paths, the pre-amplifier is FD, and the comparator and RS latches have complementary outputs. Based on these observations, we can build the following invariances that hold true for any FD input ΔIN and at every conversion cycle:

$$\begin{aligned} \text{M+}(i) + \text{M-}(i) &= \text{VREF}[32] \\ \text{L+}(i) + \text{L-}(i) &= \text{VREF}[32] \end{aligned} \tag{2}$$

$$\text{DAC+}(i) + \text{DAC-}(i) = 2V_{\text{cm}} \tag{3}$$

$$\text{LIN+}(i) + \text{LIN-}(i) = 2V_{\text{cm2}} \tag{4}$$

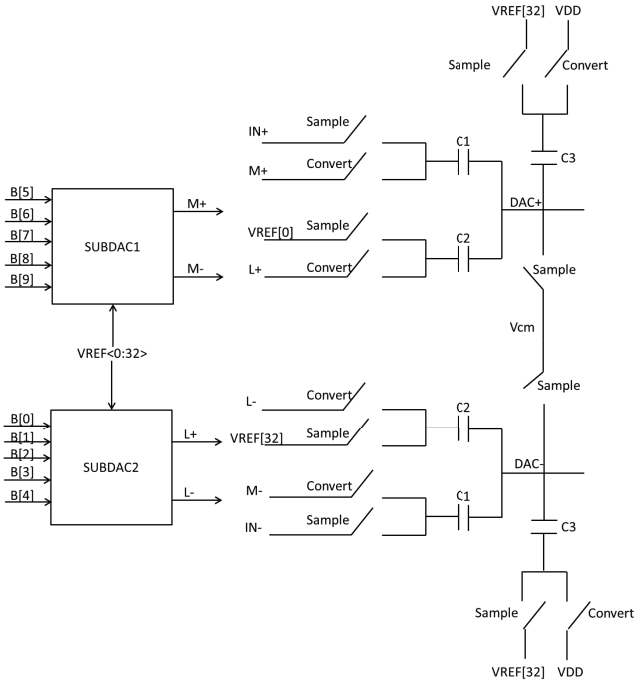

Fig. 4: 10-bit DAC block-level architecture.

$$\begin{aligned} \text{sgn}\left(\text{Q+}(i) - \text{Q-}(i)\right) &= \text{sgn}\left(\text{LIN+}(i) - \text{LIN-}(i)\right) \\ \text{Q+}(i) + \text{Q-}(i) &= \text{VDD} \end{aligned} \tag{5}$$

where V_{cm2} is the common mode at the outputs of the pre-amplifier, $\text{sgn}(\cdot)$ denotes the sign function, the argument (i) denotes the i-th conversion, and the rest of the signals are annotated in Figs. 3 and 4.

2) Test stimulus: The same test stimulus is used for checking all of these invariances. First, the FD input ΔIN stays constant at a DC value which can be set arbitrarily. Second, a 5-bit digital counter is used that generates all possible 2^5 bit combinations at the inputs B<0:4> and B<5:9> of the two sub-DACs. The rationale of this dynamic part of the test stimulus is that all components within the DAC are activated and also the comparator is extensively exercised with various inputs. The components within the bandgap and reference buffer are also activated since during this test all comparison levels VREF$[j]$, $j = 0, \cdots, 32$, are used within the DAC, as shown from Eq. (1). The V_{cm} Generator is checked directly with the invariance in Eq. (3).

3) Coverage of A/M-S part: With the 6 invariances in Eqs. (2)-(5) and the chosen test stimulus, *SymBIST* covers all A/M-S blocks of the SAR ADC IP. The purely digital blocks, i.e. SAR control, phase generator, and SAR logic, can be covered with standard digital BIST.

4) SymBIST infrastructure: The *SymBIST* infrastructure includes the 5-bit digital counter and one window comparator per invariance. Alternatively, we can employ a single comparator and switch it to check invariances sequentially. This choice reduces the area overhead at the expense of test time. A window comparator is connected via switches and buffers so as to be non-intrusive and avoid any performance penalty. *SymBIST* is embedded without imposing any design modifications in the IP. Moreover, since the test stimulus is digital and the comparator's output is a 1-bit pass or fail decision, *SymBIST* can be interfaced with a 2-pin digital test access mechanism. Overall, the area overhead of the *SymBIST* infrastructure is estimated to be less than 5%.

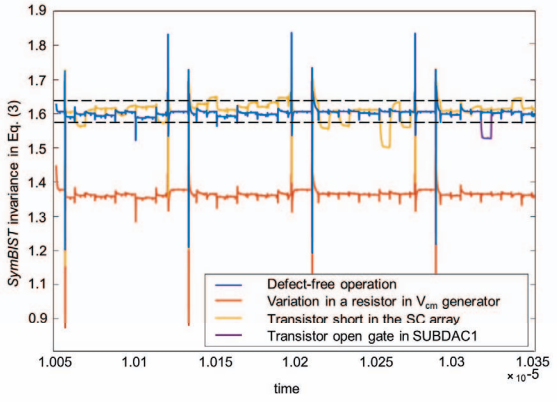

Fig. 5: Defect detection by checking invariance in Eq. (3).

5) Test time: Considering the scenario where the 6 invariances are checked sequentially, the test is completed very fast in $6 * 2^5 \cdot (1/f_{clk}) = 1.23\mu$sec, where $f_{clk} = 156$MHz is the clock frequency. This time equals about 16x the time to convert one analog input sample.

V. Defect Modeling and Defect Simulator

We rely on a standard defect model that includes short- and open-circuits across transistor and diode terminals and $\pm 50\%$ variations in passive components, i.e. resistors and capacitors. We use a short defect resistance of 10 ohms. A weak pull-up or pull-down is assigned to each open defect to account for the fact that an ideal open does not exist and, besides, it cannot be handled by a SPICE simulator [9].

Defects are simulated at transistor-level and in an automated workflow using the Tessent®DefectSim tool by Mentor®, A Siemens Business [9]. Defects are assigned a relative likelihood of occurrence that is estimated by combining global defect-type likelihoods, i.e. the likelihood of short-circuits is typically higher than the likelihood of open-circuits, and component-specific likelihoods, i.e. the expected component area on the layout, as explained in [9]. For this reason, we report the L-W defect coverage computed by the tool [9]. To reduce defect simulation time, we use the stop-on-detection and Likelihood-Weighted Random Sampling (LWRS) options [9]. When the LWRS option is used, the 95% confidence interval of the L-W defect coverage is also reported [9].

VI. Results

For our experiment we use a comparison window with $\delta = 5 \cdot \sigma$, i.e. $k = 5$, so as to guarantee that yield loss is negligible.

Fig. 5 shows the invariance signal in Eq. (3) for the defect-free case and for three randomly chosen defect cases within the blocks covered by this invariance, namely the SUBDACs, SC array, and V_{cm} generator. The comparison window is illustrated with the two dashed horizontal lines. The stop-on-detection option was disabled for these simulations. The

A/M-S blocks	# Defects	# Defects simulated	Defect simulation time (sec)	L-W defect coverage for k=5
BandGap	104	104	2035	94.22%
Reference Buffer	160	55	10620	1%
SUBDAC1	1260	112	2674	80.58%±6.68%
SUBDAC2	1260	112	2474	84.22%±5.89%
SC Array	44	44	1286	97.7%
$V_{\rm cm}$ Generator	6	6	310	30.88%
Preamplifier	24	24	700	94.12%
Comparator Latch	38	38	752	87.79%
RS Latch	40	40	983	68.09%
Offset Compensation circuit	20	20	1400	15.15%
Complete A/M-S part of SAR ADC IP	2956	101	6660	86.96%±3.67%

TABLE I: L-W defect coverage results with *SymBIST*.

instantaneous glitches are due to the switching operation. A clocked comparator is used to check the invariance with the checks performed when the node voltages are settled, thus no defect detection is flagged when the glitches exceed the range. As it can be seen from Fig. 5, while the defect in $V_{\rm cm}$ generator is detectable during the entire test duration, the defects within the SUBDAC1 and SC array are detectable during specific conversion periods.

Table I shows for the individual blocks of the SAR ADC IP and for its complete A/M-S part the total number of defects, the number of defects simulated, the total defect simulation time, and the L-W defect coverage values achieved using *SymBIST* including the 95% confidence interval when the LWRS option is used.

As it can be seen, for the entire A/M-S part of the IP, the defect coverage is $86.96\% \pm 3.67\%$. As a comparison, for two considerably smaller industrial A/M-S IPs, namely a bandgap and a power-on-reset circuit, the reported defect coverage values are 74% and 51%, respectively [9].

For certain blocks the L-W defect coverage values turn out to be very low. In fact, the absolute defect coverage is much higher, but the undetected defects have a high relative likelihood, thus dominating the L-W defect coverage.

The defect simulation times at first depend on the number of defects simulated, but by using the stop-on-detection option they also depend on the percentage of defects being detected, as well as on the detection time stamps during the test duration. For the entire A/M-S part of the SAR ADC IP, simulating 101 defects took approximately 6060s on a server with 16 cores@1.5 GHz and 128 GB RAM.

Undetected defects should be analysed carefully and it is also interesting to report the percentage of undetected defects that result in at least one specification being violated [14]. This is a tedious and time-consuming analysis and is out of the scope of this paper.

VII. Conclusions

We proposed the defect-oriented *SymBIST* paradigm for A/M-S circuits, which relies on building signals that by construction are invariant and deviate from the nominal expected value in the presence of defects. *SymBIST* is demonstrated on a 65nm 10-bit SAR ADC IP by ST Microelectronics achieving a L-W defect coverage of over 85% for the entire A/M-S part. *SymBIST* presents many advantages, including transparency to the design, very low area overhead, minimum test time, and compatibility with 2-pin digital test access mechanisms.

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