Design of Almost-Nonvolatile Embedded DRAM Using Nanoelectromechanical Relay Devices

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Abstract*—This paper proposes low-power design of embedded dynamic random-access memory (eDRAM) using emerging nanoelectromechanical (NEM) relay devices. The motivation of this work is to reduce the standby refresh power consumption through the improvement of retention time of eDRAM cells. In this paper, it is revealed that the tunable beyond-CMOS characteristics of emerging NEM relay devices, especially the ultra-high OFF-state drain-source resistance, open up new opportunities with device-circuit co-design. In addition, the pull-in and pull-out threshold voltages are tilled to fit the operating mechanisms of eDRAM, so as to support low-voltage operations along with long retention time. Excitingly, when low-gate-leakage thick-gate transistors are used together, the proposed NEM-relay-based eDRAM exhibits so significant retention time improvement that it behaves almost "nonvolatile". Even if using thin-gate transistors in a 130nm CMOS, the evaluation of the proposed eDRAM shows up to 63x and 127x retention time improvement at 1.0V and 1.4V supply, respectively. Detailed performance benchmarking analysis, along with the practical CMOS-compatible NEM relay model, the eDRAM design and optimization considerations, is included in this paper.

***Keywords*—Embedded DRAM (eDRAM), DRAM, NEM Relay, retention time, low power, beyond-CMOS.**

I. INTRODUCTION

With the development of the Internet-of-Things (IoT) and the sensor technologies, many embedded systems are dealing with the increasing amount of data. From the power efficiency and performance perspectives, this fact has required more memory to be embedded in the chips under strong constraints of limited area and power consumption budgets, especially for data-intensive edge-computing applications powered by batteries and ambient-energy harvesters [1]-[4]. Given the mature 3-transistor/cell (3T/C) embedded dynamic random-access memory (eDRAM) and the 6T/C static-random-access memory (SRAM), it may be more appropriate to adopt eDRAM when higher density is the critical need. Accordingly, optimization of the eDRAM design towards higher power efficiency plays a key role for embedded systems with a limited energy budget.

Targeting at higher power efficiency, it is inevitable to investigate the bottleneck in the conventional CMOS eDRAM: the refresh power. Providing longer data retention time, the refresh frequency could be reduced for lower power. From the circuit perspective, prior efforts [5][6] have thus investigated various methods to improve the retention time. While these efforts are indeed useful, the scope within purely CMOS-based solutions limits the achievable power efficiency.

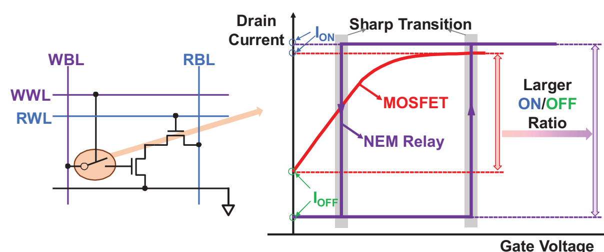

Fig. 1. NEM relay and MOSFET I-V comparisons for 3T/cell eDRAM.

Therefore, this paper targets at improving eDRAM with emerging beyond-CMOS technologies, thanks to the enhanced momentum motivated by the ending of the Moore's Law [7]. While many efforts in emerging nonvolatile memory devices have made significant progress [8]-[14], some limitations, like high write power, CMOS-incompatibility and large variations, still hinder the path towards commercialization. This paper extends the beyond-CMOS exploration by investigating the emerging nanoelectromechanical (NEM) relay, a CMOS-compatible device that has been fabricated and characterized [15]-[17]. NEM relays could be built to have different number of terminals. Fig. 1 illustrates a typical I-V curve in comparison with a traditional MOSFET. While both devices could be turned ON and OFF, it is clear that the NEM relay exhibits a unique hysteresis region. More importantly, away from the very sharp transitions at the hysteresis edges, the NEM relay shows flat resistance and a very high OFF-state resistance due to the mechanical switching mechanism. With NEM relays, a few circuit works have been proposed, showing interesting circuit functionalities or other advantages. For example, 3-terminal NEM relays have been applied in SRAM [15] and FPGA [18]. Also, data searching and nonvolatile CAM using 5-terminal NEM relays [19][20] both show high energy-efficiency. In addition, the 4-terminal NEM relays adopted in this paper, have also been exploited in digital logic [21][22].

For the eDRAM design, the key question lies in how to exploit these new device features for the eDRAM operations. While answering this question, this paper will reveal new opportunities for low-power eDRAM design with NEM relays, and present a new 2-MOSFET-1-NEM-relay/cell (2T1N/C) eDRAM using NEM relays to replace the write access transistor, as illustrated in Fig. 1. Itemized contributions include:

- The proposed 2T1N/C eDRAM, which, to the best of the authors' knowledge, uses a NEM relay as the write access switch for the first time;

- The device-circuit co-design that provides optimization of both device parameter tuning and circuit operating theories, which also guides the future NEM relay device engineering and memory architecture exploration;
- The benchmarking and analysis of the proposed eDRAM based on circuit simulations, showing exciting almost "nonvolatile" operation with thick-gate transistors, and 63x and 127x retention time improvement at 1.0V and 1.4V, respectively, with thin-gate transistors.

In the rest of this paper, section II reviews NEM relay background. Section III provides the details of the proposed eDRAM circuits and operating theories. Section IV presents the circuit simulation results compared with the CMOS-based eDRAM design. Section V discusses the proposed eDRAM for practical applications from a few other perspectives. Finally, section VI concludes this work.

II. NEM Relay Device Background

This section introduces the NEM relay device background, including the basic device structure, operating theory, recent development, VLSI modeling and feasible applications.

A. Device Basics and Opportunities

NEM relays could have 3, 4, or 5 terminals. The 4-terminal (4T) NEM relay is a CMOS-compatible device which comprises a gate electrode (G), a drain electrode (D), a source electrode (S) and a body electrode (B) [23]-[25], as shown in Fig. 2(a). A channel connecting the drain and the source is separated from the gate electrode by the gate dielectric. The device state is controlled by the electrostatic force generated by the voltage difference between the movable gate and the fixed body (V_{GB}). When V_{GB} exceeds a certain voltage, defined as the pull-in voltage (V_{PI}), the gate deflects towards the body, which makes the channel contact the drain and source. As a result, the current can flow through the channel between the drain and the source. When V_{GB} is below the pull-out voltage (V_{PO}), the channel is out of contact with the drain and the source. Many works [15][16] have shown a hysteresis in the I_{DS}–V_{GB} characteristic with $V_{PO} < V_{PI}$, as shown in Fig. 2(b). As the electrostatic attraction is ambipolar, a 4T NEM relay can also operate like a PMOS transistor by biasing the body at VDD.

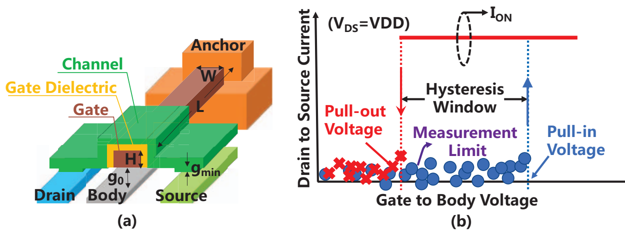

Fig. 2. The 4T NEM relay: (a) structure; (b) Typical I_D–V_G ([23]-[25]).

B. Recent Device Design and Fabrication Progress

NEM relays were proposed long ago [26]. The recent fast development has been boosted by a few breakthroughs. Some can operate in a CMOS-compatible voltage (~1V) [27][28] and high density can be also achieved by scaling and even 3D stacking [16][23]. Another significant breakthrough is the success of a back-end-of-line (BEOL) compatile process. A BEOL process makes it possible for NEM relays to be embedded in the CMOS back end, which is an appealing approach to the integration of NEM relays with CMOS transistors, and further footprint area savings [25]. Reports have even shown a 4T NEM relay for 7nm CMOS process implemented in BEOL stack [25]. These technologies have inspired more promising feasibility of design and experimental demonstration for NEM-MOS hybrid circuits in the near future.

C. NEM Relay Modeling and Applications Concerns

A NEM relay Verilog-A model is available in [15][23]. It has been used in a few works [18][29], and the ON-state and OFF-state are illustrated in Fig. 3. More device parameters will be provided and dicussed in section IV. It is clear that writing the NEM relay is essentially a process of charging or discharging the gate to body capacitor C_{GB}, and reading a NEM relay is to detect the drain to source current I_{DS}, or equivalently, the drain to source resistance R_{DS}.

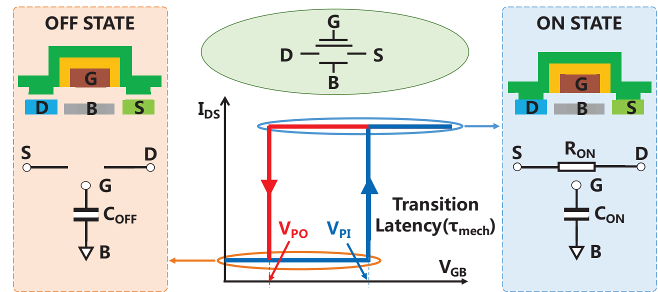

Fig. 3. Modeling the 4T NEM relay[15][16][23].

The 4T NEM relays are attractive in low-power and energy-efficient applications due to intriguing features: (i) ultra-low OFF-state leakage; (ii) sharp static subthreshold slope; (iii) low ON-state resistance without threshold voltage drop; (iv) the isolation of read and write operations. These fascinating features can be implemented in many digital circuit designs, especially in memory and logic [16][20]-[23].

As the NEM relay state is switched by the mechanical movement of the gate, the intrinsic latency required to displace the relay from OFF to ON (τ_{mech}) could be in ns, higher than that of MOSFETs [27]. This makes it more suitable for less speed-sensitive applications. Another concern is the relatively lower endurance ~10^{10} at this moment (without considering further device improvement) [30]. This device feature requires it to operate in less-active or event-triggering applications. As to be shown later, this endurance is far sufficient for the proposed eDRAM, thanks to the almost "nonvolatile" feature. Moreover, the increase of NEM relay endurance from 10^6 in [15] to 10^{10} cycles in [30] has witnessed possible improvement. In the future, more research for less latency and higher endurance will be of high impact from the perspectives of this work.

III. Proposed NEM-Relay-Based 2T1N/C eDRAM

This section presents the proposed design of NEM-relay-based 2T1N/C eDRAM in details, including the circuit scheme, the memory access operations, along with transient waveforms.

A. Proposed NEM-Based eDRAM Circuit Scheme

Fig. 4(a) shows a single 2T1N cell, consisting of two MOSFETs, one NEM relay, the write bit line (WBL), the read bit line (RBL), the word write line (WWL), and the read word line (RWL). The structure is generally the same as the conventional 3T/cell CMOS eDRAM, with the write-access transistor replaced by one NEM relay. The internal storage node, X_{store}, is connected to the gate of the data-storage transistor (T1), and bridged with the write bit line (WBL) through the NEM relay channel. Fig. 4(b) shows a 2x2 2T1N/C eDRAM array, which could be easily expanded into a larger size.

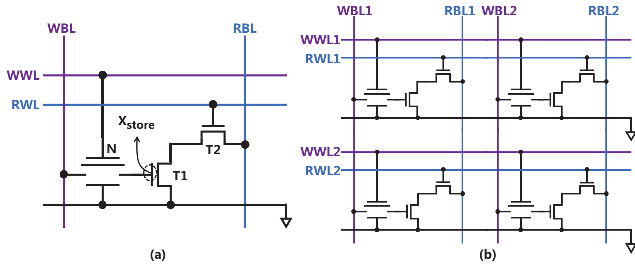

Fig. 4. Proposed 2T1N/C eDRAM: (a) a single cell; (b) a 2x2 array.

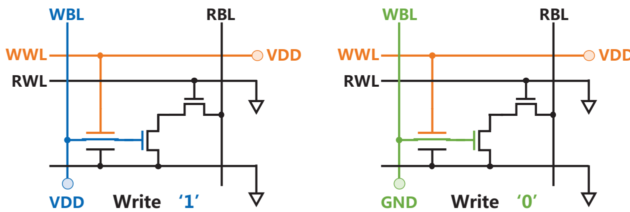

Fig. 5. Write scheme for the proposed 2T1N cell in Fig. 4(a).

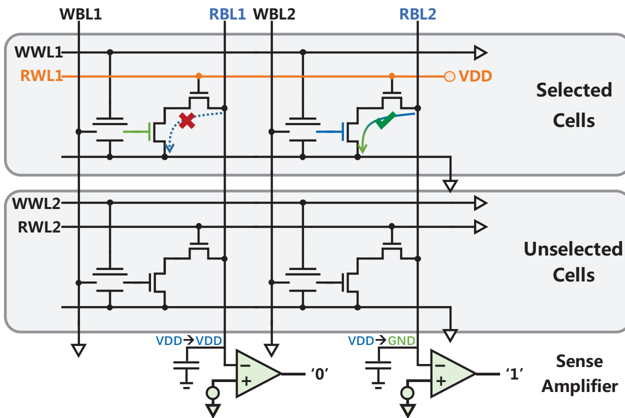

Fig. 6. Read scheme for the proposed 2T1N/C eDRAM array.

B. Write and Read Operations

The write operation of a 2T1N/C array is similar to that of the conventional 3T eDRAM. Fig. 5 shows detailed configuration. To carry out a write access, WWL switches to VDD and the write bit line WBL is set to either VDD or GND based on the bit of datum to be written into the eDRAM cell. When the NEM relay is actuated with an intrinsic latency, τ_{mech}, the voltage of X_{store} is set by WBL, to either VDD or GND. Considering that the electrical charging or discharging time at the node X_{store} is in picosecond range (<100ps) while τ_{mech} at this moment is expected to be in the range of nanosecond as reported in [27], the write time is mainly determined by τ_{mech}.

Read access is also similar to that in the CMOS eDRAM. The read bit line RBL is pre-charged and then T2 is turned on by driving the read word line RWL to VDD. If X_{store} is in the low voltage level, T1 remains OFF and RBL will stay at the pre-charged value; otherwise the RBL will be pulled down towards ground through T1 and T2. For less read latency, each RBL is connected to a sense amplifier (SA), as shown in Fig. 6. A trade-off between area, power and latency could be carried out based on the application need. This is mainly based on the fact that the minimum voltage on RBL that SA needs to distinguish between '1' and '0' (ΔV_{min}) is a function of SA input offset, bandwidth, gain, etc.

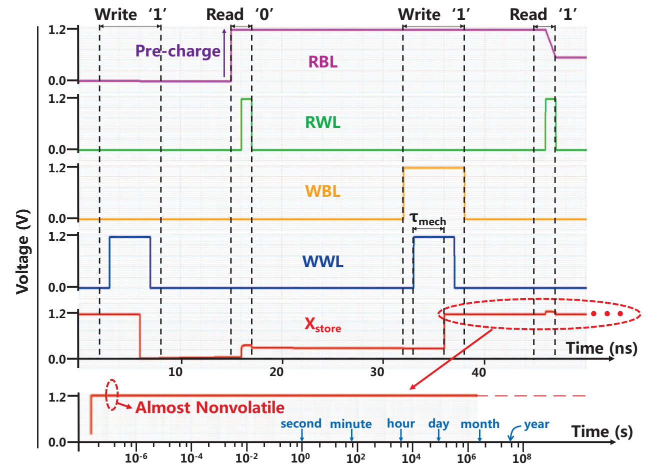

Fig. 7. Transient waveforms for the proposed 2T1N/C eDRAM.

C. Is Refresh Operation Literally Needed?

For both conventional CMOS eDRAM and the proposed NEM-relay-based eDRAM, the minimum refreshing frequency, corresponding to the retention time, depends on how the charge stored at the node X_{store} may leak over time. In CMOS eDRAM cells, the charge leakage at X_{store} is mostly caused by the non-zero write-access-transistor leakage current, and partially by the storage transistor T1 gate leakage. For the proposed eDRAM, an exciting fact is that, the OFF-state leakage current of a NEM relay is theoretically zero before it breaks down, thanks to the mechanical switching mechanism. Therefore, the retention time of the proposed NEM-relay-based eDRAM almost fully depends on the gate leakage of the internal storage MOSFET (T1 in Fig. 4(a)). With a proper CMOS process, it is possible to limit the gate leakage of T1 in Fig. 4(a) to be ultra low, leading to days and even years of retention time which makes the eDRAM almost "nonvolatile".

Fig. 7 shows a waveform snapshot of transient simulation results, where the write and read operations are carried out. In this simulation, the two MOSFETs in the proposed eDRAM are implemented in thick-gate NMOS in 65nm CMOS. In this case, the retention time could be expected to be up to years, making the proposed eDRAM almost "nonvolatile". More details about device parameters and simulation environment will be provided

in the subsequent section IV. In some cases of using a deeply-scaled thin-gate MOSFET as the internal storage transistor, the gate leakage may not be ignored and refresh operations are needed. A general refresh method is divided into two steps, which is similar to that in CMOS-based eDRAM: first read out the stored data and then write them back. As refresh operations consume significant energy and stall the normal read and write requests, the unique feature towards almost "nonvolatile" eDRAM provides an opportunity for ultra-low-power embedded memory solution.

D. Device-Circuit Co-Design

The NEM relay device analysis in prior arts has revealed the relationship between the electrical performance and the device physical parameters [15][23]. While most analysis at the device level could be beyond the scope of this work, the design space exploration of critical device parameters could exert significant impact on the proposed eDRAM. Therefore, we investigate the device-circuit co-design based on the two most significant device parameters for low-voltage operations: the gate length (L) and the gate thickness (H). Investigations show how they affect the pull-in voltage V_{PI} and the pull-out voltage V_{PO}.

Fig. 8 shows the impact of the gate length L and the gate thickness H. Increasing L from 180nm to 340nm, V_{PI} and V_{PO} reduce from 1.67V and 1.17V to 0.47V and 0.33 V, respectively. Increasing H, oppositely, increases both V_{PI} and V_{PO}. We choose L = 260nm and H = 10nm in this work for good balance between low-voltage operation and sufficient noise margin of 0.24V between V_{PI} and V_{PO}.

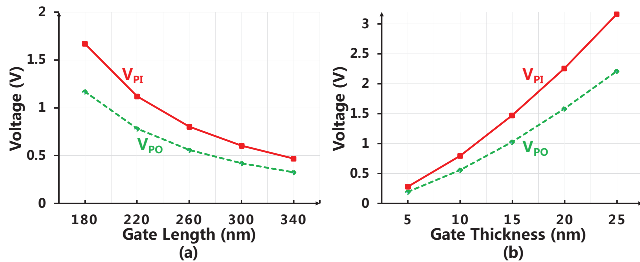

Fig. 8. The impact of gate length (L) and gate height (H) on V_{PI} and V_{PO}.

IV. BENCHMARKING THE PROPOSED 2T1N/C EDRAM

This section evaluates the performance of the proposed NEM-relay based 2T1N/C eDRAM in section III. The performance of nonvolatile characteristic, the retention time, and refresh power and are simulated and discussed.

A. Benchmarking Settings

The key simulation parameters of the NEM relay model are listed in TABLE I. The NEM relay ON-state resistance (R_{ON}) changes with V_{GB} [31], but its variance could be ignored as the electrical RC charging/discharging time in ps is much shorter than the mechanical switching latency τ_{mech} reported to be in ns, e.g. 3ns in [15][27]. This is similar to the total access latency in CMOS-based eDRAM for low-power devices.

The other two NMOS transistors (T1 and T2) are in commercial 65nm or 130nm CMOS processes. They could be either thin-gate transistors (typically for digital logic) and thick-gate transistors (typically for chip I/O interfaces). In this simulation, the column size is set to be 128 and the row size varies. Each word and bit line have been added with a capacitor to take the parasitic effect into account. The value of parasitic capacitance is set to 50fF for a size of 512 rows or columns.

TABLE I. NEM RELAY MODEL PARAMETERS

Structure parameters	L		W	H		g_0	g_{min}
	260nm		65nm	10nm		10nm	3.3nm
Simulation parameters	V_{PI}	V_{PO}	C_{ON}	C_{OFF}	R_{ON}		τ_{mech}
	0.80V	0.56V	20aF	15aF	1kΩ		3ns

Simulations are carried out with Cadence Virtuoso. For fair comparison in typical applications, at the end of the retention time, the read bit line (RBL) being read needs to exhibit a minimum voltage difference of ΔV_{min} equal to 100mV within 3ns between reading the states of '0' and '1'.

B. "Nonvolatile"-Mode Benchmarking

As described above, if the internal storage transistor T1 is using a thick-gate technology with ultra-low gate leakage, the retention time could be as high as up to years, which makes the 2T1N/C eDRAM operating in the "nonvolatile" mode. Fig. 7 has shown the X_{store} voltage of the 2T1N/C eDRAM for a long time scale, with almost no change leakage for up to a few months. In Fig. 9, the comparison of the X_{store} voltage between the 3T/C CMOS eDRAM and the proposed NEM-relay-based eDRAM is shown at 1.2V supply, in two different commercial CMOS technologies. For the 3T/C CMOS eDRAM, the X_{store} voltage decreases continuously due to the drain-source leakage current, and thus refresh operations are required when X_{store} voltage drops below 461mV (598mV), showing retention time of 75.1μs (62.1μs) in a 65nm process (a 130nm process). Differently, for the proposed 2T1N eDRAM, the X_{store} voltage keeps almost constant at VDD for long-time standby.

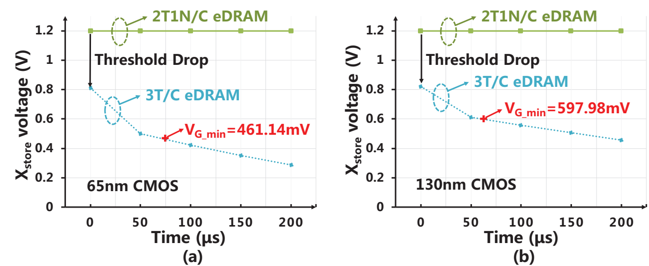

Fig. 9. Comparisons of the X_{store} voltage between the proposed "Nonvolatile" 2T1N/C eDRAM and CMOS 3T/C eDRAM using thick-gate NMOS transistors @VDD=1.2V: (a) in 65nm process, (b) 130nm process.

C. Retention Time Benchmarking with Thin-Gate MOSFETs

Using some thin-gate NMOS transistors in either 65nm or 130nm CMOS process as the internal storage transistors, the gate leakage could not be neglected and refresh operations are required. In the retention time simulations, the supply voltage VDD in both write operation and read operation ranges from 1.0V to 1.4V.

Fig. 10 shows the comparison of the retention time in this case, between the conventional 3T/C eDRAM and the proposed

2T1N/C eDRAM, where significant improvement of retention time could be observed. With the 130nm CMOS, the 2T1N/C eDRAM design improves the retention time to 0.55ms (~63x) at 1.0V, or 2.90ms (~127x) at 1.4V. With the 65nm CMOS, the proposed eDRAM improves the retention time to 1.70μs (~3.85x) at 1.0V, or 8.31μs (~10.62x) at 1.4V.

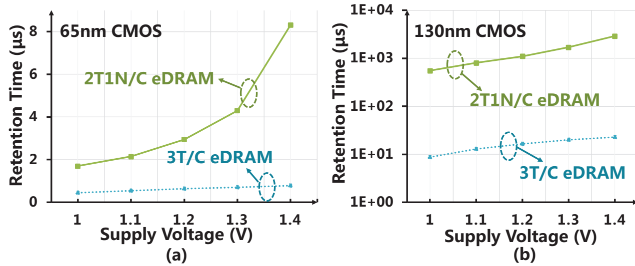

Fig. 10. Retention time evaluation: (a) using 65nm CMOS process; (b) using 130nm CMOS process.

There are two main contributors to this improvement. One is the zero threshold (V_{th}) drop of 4T NEM relay, which provides the internal node X_{store} at the 2T1N/C eDRAM with a higher initial voltage for the state of '1' after a write operation. This difference originates to the V_{th}-drop for a MOSFET to pass a VDD voltage which causes the initial X_{store} voltage to be VDD-V_{th} for CMOS eDRAM. The other contributor is the zero off-state drain-source leakage of the 4T NEM relay, which slows down the decrease of charges at the storage node significantly.

D. Refresh Power Benchmarking with Thin-Gate MOSFETs

This subsection evaluates the refresh power saving in 2T1N/C eDRAM as a function of the row size and the supply voltage. A 130nm CMOS process is used as an example for the MOSFETs. While comprehensive analysis of refresh power considering peripheral circuits could be carried out in the future, like in [32], we evaluate the refresh power consumed within the array sharing the same decoder, bit lines and word lines, and the sensing interface. In addition, the power performance is evaluated, rather than the refresh energy for a single refresh operation, so the refresh frequency is considered as well.

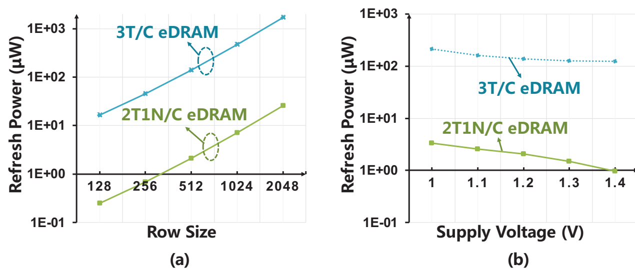

Fig. 11. Refresh power evaluation in a commercial 130nm process: (a) as a function of the row size with VDD = 1.2V; (b) as a function of supply voltage with row size = 512.

Fig. 11(a) summarizes the refresh power versus the row size with VDD fixed at 1.2V. In the refresh operations, most energy is spent in charging and pre-charging the bit line capacitance (C_{BL}). With a large row size, both C_{BL} and the refreshing traffic increase linearly, and the refresh power increases proportional to the square of the row size approximately. From the results, as row size ranges from 128 to 2048, the refresh power of 2T1N/C eDRAM increases from 0.25μW to 25.9μW, showing 98.5% power reduction from that in CMOS eDRAM.

Fig. 11(b) illustrates the refresh power versus the supply voltage with the row size fixed at 512. Note that the single-cell refresh energy and retention time both increase with a higher VDD. In this simulation, setting VDD at 1.4V can enable the lowest refresh power for the 2T1N/C eDRAM, as the refresh power of CMOS eDRAM and 2T1N/C eDRAM decreases from 211μW and 3.35μW (63.0x improvement) to 123μW and 0.97μW (127x improvement), respectively.

V. More Discussion

This section discusses the proposed eDRAM from a few other perspectives, including the device variations and other potential candidate devices similar to NEM relays.

A. Device Variations

It is known that device variations affect circuit performance and even functionality. Therefore, it is important to evaluate the possible influence caused by device variations and fluctuations, especially for beyond-CMOS devices. We investigate the variations to three key device parameters: the NEM relay width *W*, gate length *L*, and the gate thickness *H* (see Fig. 2 for device parameter details) and check their impact on the electrical parameters: V_{PI}, R_{ON} and τ_{mech}. Other parameters are not the main concern due to the mechanical switching behavior. The impact of large-scale changes to *L* and *H* has been investigated in section III. Here only small random deviations are considered.

Based on the relationships in [16], Fig. 12 shows the maximum impact on the mechanical delay τ_{mech} and the on-state resistance R_{ON}, indicating less than 3.6% (11.1%, 19.2%) and 3.1% (9.5%, 16.3%) absolute changes, respectively, for 1% (3%, 5%) device variations. Note that the minimum operating voltage is determined by V_{PI}, and that the maximum V_{PI} is still well within the practical VDD range without requiring a higher VDD even if with 5% device parameter deviations.

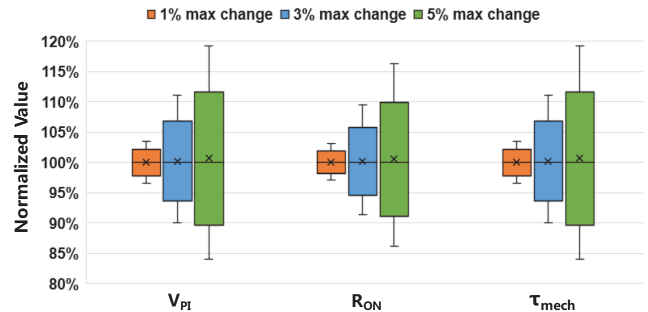

Fig. 12. The impact of device variations (*L*, *W* and *H*) on V_{PI}, R_{ON} and τ_{mech}.

B. Other NEM Relays and Other eDRAMs

This work could be intuitively extended in two other directions in future works. The first one is to use different types of NEM relays, e.g. 3-terminal NEM relays instead of the 4-terminal NEM relay in this work. In the 3-terminal NEM relay, the body is shorted to the source of the relay, and the pull-in

and pull-out switching behavior depends on the signal being delivered. While such dependency may introduce certain performance degradation, e.g. V_{th}-drop, simplification of the device terminals may bring extra benefits such as footprint saving. Another direction is to use NEM relays in other eDRAM topologies, such as 3-transistor-1-diode cells that incorporate an extra diode for more storage capacitance at X_{store}, and 2-transistor cells for refresh-less one-time-use eDRAMs.

VI. Conclusion

This paper has presented an almost "nonvolatile" NEM-relay-based eDRAM through the exploration of device-circuit co-design. The eDRAM exhibits up to years retention time when integrating with thick-gate MOSFETs, and up to 127x retention time improvement when integrating with thin-gate MOSFETs. Unique hysteresis characteristics, including low ON-state resistance, ultra-high OFF-state resistance, and tunable pull-in and pull-out voltages have been harnessed to enable the eDRAM. The impact of device variation is also evaluated. Future architecture exploration and further device improvement may provide even more promising outcomes.

Acknowledgment

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