A Method of Via Variation Induced Delay Computation

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***Abstract*— As process technologies are scaled down, interconnect delay becomes major component of entire path delay, and vias represent a significant portion of the interconnect delay. In this paper, a novel variation-aware delay computation method for vias is proposed. Our experiments show that this method can reduce over five percent of pessimism in arrival time calculation when it is compared with state-of-the-art solutions.**

Keywords—static timing analysis, STA, via, resistance, random variation, statistical static timing analysis, SSTA

I. Introduction

Static Timing Analysis (STA) [1] is not only one of the most crucial steps in the semiconductor chip signoff process but also the core engine of timing-driven implementation tools. To validate the timing robustness of a design with various process variations, an accurate and efficient model for cell and wire delay variation is required. Process variation can be classified into two types: global variation and local one [2]. While statistical STA (SSTA) [1], [3] can consider both global and local variation in delay calculation, it is too computation-intensive to be applied to all the paths in a design. Recently, instead of SSTA, industries adopted parametric on-chip variation (POCV) method [2], and new cell libraries such as Library Variation Format (LVF) [4] for modeling local random variation of cell delay. However, there has been no way to model local random process variation of interconnect yet.

Since 40nm, wire resistance induced delay has been getting serious. From 40nm to 7nm, capacitance increases by ten percent, while resistance has doubled [5]. As a result, resistance induced wire delay has increased rapidly. In the 40nm era, the ratio of wire delay to total delay was less than ten percent, but the ratio becomes about twenty five percent in 7nm, and forty percent in 5nm [5]. It is expected that the variation of via resistance will particularly increase at future technology nodes, and its impact on the performance degradation will become more critical [6]. RC corners are used to account for global wire variations. However, the local random variation of via resistance has not been considered in an accurate way.

To overcome this limitation, we propose a new model for local random variation of via resistance, and an efficient STA method that uses that model for accurately analyzing via variation induced delay. The proposed method averages out the random variation of the via resistance in each net, which result in reducing the pessimism in wire delay calculation. Our experimental results show that the method can reduce over five percent of the arrival time with small runtime and memory overhead.

II. Via Variation Induced Delay Computation

A. Via Resistnace Variation Modeling

Timing slack that is calculated using a STA engine is a standard metric for deciding the timing failure of a path [7]. When POCV-based commercial STA engines calculate the slack of a path, it considers the impact both of the global process variation and of the local (i.e. random) variation on cell delay. It is depicted how commercial STA engines calculate reported slack $Slack_{RPT}$ in (1):

$$Slack_{RPT} = Slack_{Global} - k\sigma_{Slack} \quad (1)$$

The slack with only global variation considered $Slack_{Global}$ is calculated using the cell libraries and the parasitic RC of each net in a specific RC corner. The sigma level k is combined with σ_{Slack} that is the standard deviation of the slack induced by local variation.

In this work, the global and local variation concept for the cell delay calculation is expanded to via resistance. Fig. 1 shows the correlation of the measured resistance of nearby via pairs of the same layer. It seems that the resistance of one via has no correlation with that of others. It is well matched with the previous research [8], and the via resistance is thought of as a random variable in the proposed model.

B. Implementation

A new statistical delay calculation method for via resistance variation has been implemented in STA tools in collaborating with an EDA company. The global via resistance variation is given to a STA tool as RC corners, and the local one is set using a separate technology file.

During the delay calculation for local variation of via

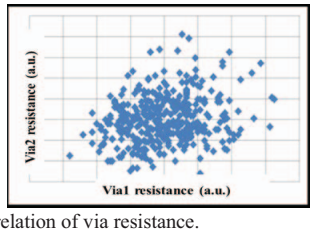

Fig. 1. The correlation of via resistance.

resistance, the resistance of vias is thought of as an variation source. Its impact on the delay of a specific cell and wire is calculated using the parametric form as shows in (2) and (3). For the *i*-th via in an interesting net, D_{Cell0} and D_{Wire0} are the driving cell delay and the wire delay between driving and loading cell, respectively, when the via has no local variation. The term $\partial D_{Cell}/\partial VIA_i$ and $\partial D_{Wire}/\partial VIA_i$ are the cell and wire delay sensitivity to the variation of the *i*-th via. The term σ_{VIA_i} is a standard deviation of via resistance, and p_{VIA_i} is a random variable that follows the normal distribution.

$$D_{Cell} = D_{Cell0} + \sum_i \frac{\partial D_{Cell}}{\partial VIA_i}\sigma_{VIA_i}p_{VIA_i} \quad (2)$$

$$D_{Wire} = D_{Wire0} + \sum_i \frac{\partial D_{Wire}}{\partial VIA_i}\sigma_{VIA_i}p_{VIA_i} \quad (3)$$

Once the parametric delay of each cell and wire in a path is computed, the variation of the path delay can be calculated as shown in (4). In (4), the variation of each cell and wire delay averages out. It can reduce the pessimism of the calculated path delay when it is compared to the previous approach where via resistance is fixed to its maximum value.

$$\sigma_D = \sqrt[2]{\sum_i \left(\left(\frac{\partial D_{Cell}}{\partial VIA_i} + \frac{\partial D_{Wire}}{\partial VIA_i}\right)\sigma_{VIA_i}\right)^2} \quad (4)$$

The computed via delay variation is statistically combined with the cell delay variation in LVF libraries to generate the final slack variation σ_{Slack} in (1).

III. Experimental Result

We tested the proposed method using a couple of CPU designs. First, the proposed method was compared with a Monte Carlo (MC) STA and a nominal STA to show its accuracy. In the nominal STA, via resistance was extracted from the global via resistance corner and local variation was not considered. In each MC analysis, each via resistance was randomly chosen based on the distribution that were used for the via variation STA, then the arrival time of the paths were calculated. The number of trials for the MC analysis was one thousand. Fig. 2 shows a comparison among the arrival time of selected paths in nominal STA (blue dots), that in the proposed method (red dots), and that in a MC analysis (black line). One thousand setup critical paths were selected from the nominal STA result, and each of them were tested one thousand times for the MC analysis. The result shows that the nominal STA result is optimistic than the MC based one, while the via variation STA result is well correlated to the MC STA result.

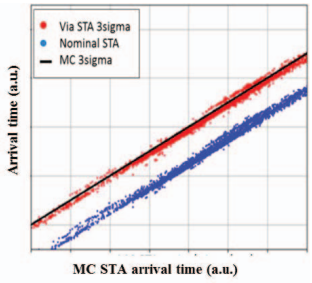

Fig. 2. Proposed vs MC STA.

TABLE I. Via Variation STA Results

Voltage (V)	Arrival Time Change (%)	
	Design 1	*Design 2*
1.0	-5.74	-5.94
0.8	-3.91	-4.06

TABLE II. Runtime and Memory Overhead

Design	# of Instances	Runtime Overhead	Peak Memory Overhead
Design 1	145k	1.0	1.1
Design 2	136k	1.0	1.0
Design 3	1,564k	1.2	1.0
Design 4	1,230k	1.1	1.1
Design 5	1,557k	1.2	1.0
Average		1.1	1.0

Second, we compared the arrival time of the proposed method with that of the widely used corner based method where via resistance is fixed to its maximum value by both the global and local variation. As shown in Table 1, the proposed method can reduce over five percent of the arrival time of the traditional STA results. The wire resistance gives a larger impact on delay when the supply voltage becomes higher. The amount of reduction becomes somewhat smaller as the supply voltage drops.

Finally, the runtime and memory ratio of the proposed method to those of the traditional STA is summarized in Table 2. The average runtime overhead is under ten percent, and it does not require much larger memory than the nominal STA.

IV. Conclusion

We developed a new method of via resistance variation-aware delay computation. We expanded global and local variation concept of cell delay to via resistance to reduce pessimism of the traditional corner based method.

References

[1] D. Blaauw, K. Chopra, A. Srivastava, and L. Scheffer, "Statistical timing analysis: From basic principles to state of the art," IEEE Trans. Comput. Des. Integr. circuits Syst., vol. 27, no. 4, pp. 589–607, 2008.

[2] A. Mutlu, J. Le, R. Molina, and M. Celik, "A parametric approach for handling local variation effects in timing analysis," in Proceedings of the 46th Annual Design Automation Conference, 2009, pp. 126–129.

[3] C. Visweswariah, K. Ravindran, K. Kalafala, S. G. Walker, S. Narayan, D. K. Beece, J. Piaget, N. Venkateswaran, and J. G. Hemmett, "First-order incremental block-based statistical timing analysis," IEEE Trans. Comput. Des. Integr. Circuits Syst., vol. 25, no. 10, pp. 2170–2180, 2006.

[4] Synopsys, "Library Compiler User Guide," 2019. [Online]. Available: https://solvnet.synopsys.com/dow_retrieve/latest/dg/libolh/Content/lcug1/ni/lcug1.pdf.

[5] C. Hou, "1.1 A smart design paradigm for smart chips," in 2017 IEEE International Solid-State Circuits Conference (ISSCC), 2017, pp. 8–13.

[6] I. Ciofi, P. J. Roussel, Y. Saad, V. Moroz, C.-Y. Hu, R. Baert, K. Croes, A. Contino, K. Vandersmissen, W. Gao, and others, "Modeling of via resistance for advanced technology nodes," IEEE Trans. Electron Devices, vol. 64, no. 5, pp. 2306–2313, 2017.

[7] R. B. Hitchcock, "Timing verification and the timing analysis program," in 19th Design Automation Conference, 1982, pp. 594–604.

[8] S. Yao, L. Clevenger, and N. Zamdmer, "A study of BEOL resistance mismatch in double patterning process," in 2015 IEEE International Interconnect Technology Conference and 2015 IEEE Materials for Advanced Metallization Conference (IITC/MAM), 2015, pp. 147–150.