High-Density, Low-Power Voltage-Control Spin Orbit Torque Memory with Synchronous Two-Step Write and Symmetric Read Techniques

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***Abstract*-Voltage-control spin orbit torque (VC-SOT) magnetic tunnel junction (MTJ) has the potential to achieve high-speed and low-power spintronic memory, owing to the adaptive voltage modulated energy barrier of the MTJ. However, the three-terminal device structure needs two access transistors (one for write operation and the other one for read operation) and thus occupies larger bit-cell area compared to two terminal MTJs. A feasible method to reduce area overhead is to stack multiple VC-SOT MTJs on a common antiferromagnetic strip to share the write access transistors. In this structure, high density can be achieved. However, write and read operations face problems and the design space is not sure given a strip length. In this paper, we propose a synchronous two-step multi-bit write and symmetric read method by exploiting the selective VC-SOT driven MTJ switching mechanism. Then hybrid circuits are designed and evaluated based a physics-based VC-SOT MTJ model and a 40nm CMOS design-kit to show the feasibility and performance of our method. Our work enables high-density, low-power, high-speed voltage-control SOT memory.**

Keywords—Spintronics, magnetic tunnel junction, MRAM, voltage-control spin orbit torque.

I. INTRODUCTION

Nonvolatile memories, such as resistive RAM (ReRAM), phage change RAM (PCRAM), magnetic RAM (MRAM), have been considered as promising technologies to address the leakage power issue as technology scales [1-3]. Among them, MRAM has advantages of high endurance, high speed and low power, and is mature for embedded applications. The mainstream MRAM utilizes spin transfer torque (STT) for data writing operation, which, however, still consumes more energy and latency compared to SRAM [4, 5]. The new generation MRAMs utilizing spin orbit torque (SOT) and voltage control mechanisms have attracted much attention for low-power (6 fJ/bit) and high-speed (1 ns) MRAM [6-8]. However, both mechanisms have their own drawbacks. For SOT, the three-terminal magnetic tunnel junction (MTJ) device structure needs two access transistors (one for write and the other one for read) and thus occupies larger bit-cell area compared to two-terminal STT MTJs [9,10]. Regarding voltage-control MTJ, the precessional toggle switching has big reliability issue [11-13]. Recently, a new MTJ switching method, called voltage-control SOT (VC-SOT), which fully takes advantages of both SOT and voltage-control, has been proposed and experimentally verified [14-18]. Based on the VC-SOT mechanism, experimental results have reported that the critical SOT switching current density can be modulated by 3.6 folds [15-17]. In addition, multiple MTJs can be stacked parallel on a common strip to share the write access transistors. In this structure, high density can therefore be achieved, similar to NAND flash memory, but with high speed and low power at the same time. The major problems of this structure are the write and read operations for random data access. To solve the problems, in this paper, we propose a novel synchronous two-step multi-bit write and symmetric read approach by exploiting the selective VC-SOT driven MTJ switching mechanism along a common strip.

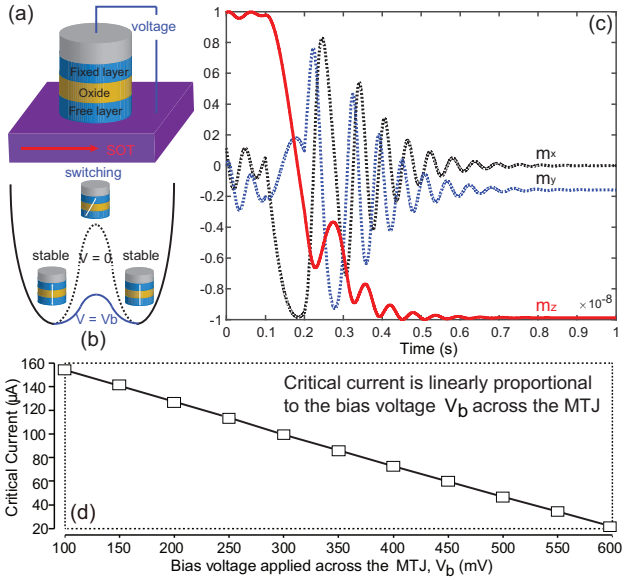

Fig. 1. The device structure of VC-SOT MTJ; (b) The voltage-control effect on the energy barrier; (c) Field-free magnetization switching dynamics of the MTJ under the VC-SOT mechanism. Here Mx, My, Mz denote the magnetization vector along the x, y, z directions; (d) Critical SOT switching current as a function of the bias voltage applied across the MTJ device [24].

II. FUNDAMENTALS OF VC-SOT MTJ DEVICE

The MTJ device includes three layers: ferromagnetic (FM) fixed layer, oxide layer and FM free layer. The resistance of an MTJ depends on the relative magnetization states between the fixed layer and free layer, including parallel state (low resistance, say denotes data bit "0") and anti-parallel state (high resistance, say denotes data bit "1") [19]. In the VC-SOT MTJ device, as shown in Fig. 1(a), the fixed layer is connected to a voltage source, while the free layer is in direct contact to an antiferromagnetic (AFM) layer (e.g., IrMn). For memory

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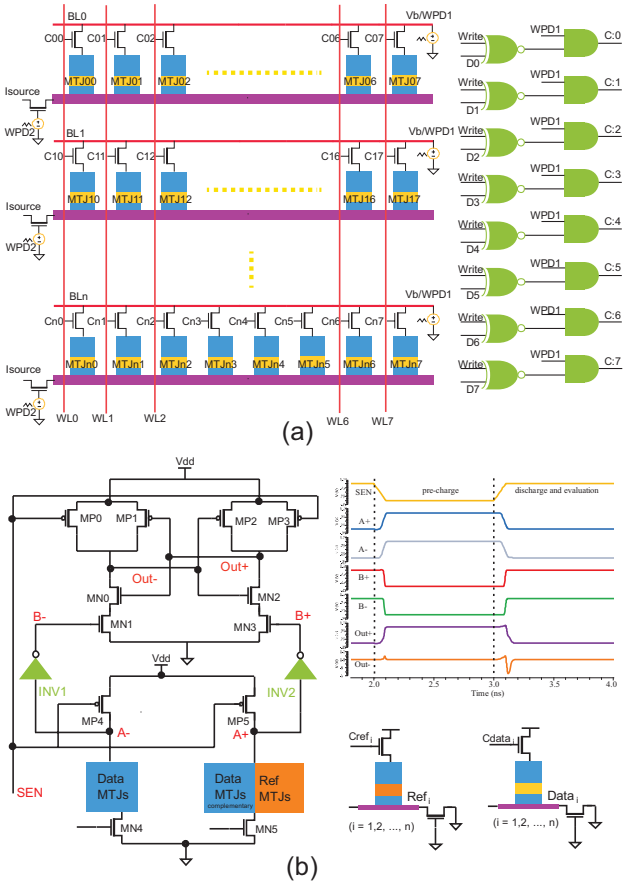

Fig. 2. (a) The VC-SOT MTJ array (8 bits along each strip as an example) and the associated write signals; (b) The sensing amplifier for read operation.

application, perpendicular MTJs are preferable than in-plane MTJs due to their better scalability, faster switching, and lower power consumption [20, 21]. However, an external magnetic field is commonly needed for switching of perpendicular MTJ (pMTJ) devices with VC-SOT. Recently, magnetic field-free switching of pMTJs were observed in the IrMn/CoFeB/MgO structure, where the AFM layer provides an exchange bias and SOT at the same time [22, 23]. This is essential and of practical significance for VC-SOT MTJ based advanced spintronic memories. Furthermore, the bias voltage applied on the MTJ can modulate the energy barrier and thus changes the critical SOT switching current density [24], shown in Fig. 1(b) and Fig. 1(d). Fig. 1(c) shows the field-free magnetization switching dynamics of MTJ under the VC-SOT mechanism with a bias voltage ($V_b = 1V$) and an in-plane SOT write current with amplitude of 45 μA. Both the SOT and voltage torques pull the magnetization of the free layer towards the in-plane direction. Moreover, the exchange bias field at the interface between the AFM/FM (IrMn/CoFeB) layers of the MTJ breaks the in-plane magnetic symmetry [22, 23]. Therefore, a deterministic and complete magnetization reversal of the free layer of the MTJ device can be achieved in sub-nanoseconds. VC-SOT pMTJ is promising for high-speed, low-power and high-density spintronic memory.

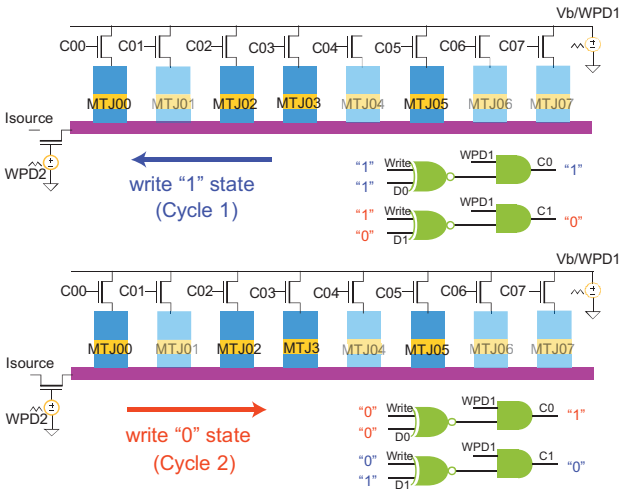

Fig. 3. Illustration of the process of the synchronous two-step multi-bit write approach on the VC-SOT MTJ array.

III. Proposed Approaches

Fig. 2(a) shows the VC-SOT MTJ array (8 bits along each AFM strip as an example) and the associated write signals. As can be seen, the bias voltage of each MTJ is applied through the bit-line (BL) by selectively activating the access transistor, while the SOT write current is applied through the AFM strip. Here WPD1 (write pulse duration 1) and WPD2 (write pulse duration 2) denote the pulse widths for the bias voltage and the SOT write current respectively. D0, D1, …, D7 are the data intending to be written into the cells.

A. Synchronous Two-Step Multi-Bit Write Approach

As described above, the critical SOT switching current of the MTJ depends on the applied bias voltage. Therefore, in our proposed write approach, the write operation is divided into two cycles: one cycle for writing MTJs targeting for data bit "0" and the second cycle for writing MTJs targeting for data bit "1". As depicted in Fig. 2(a), the WL signal, which comes from the logic circuit calculation at the right-hand side of Fig. 2(a), decides whether the corresponding column is selected to be operated. If the WL is high, the column will be connected to the bias voltage, then the corresponding MTJ will have a lowered energy barrier, thus a lowered critical SOT write current, and a proper SOT write current (between the lowered critical switching current and the regular switching current) can switch the MTJ; otherwise, if the WL is low, the column will be dis-connected to the bias voltage, then the corresponding MTJ will remain a regular energy barrier, thus the SOT write current cannot switch the MTJ. In this case, in the first cycle, the MTJs targeting for bit "1" are selected and a SOT write current with a proper current density (say in the left-hand direction to write data bit "1") flows through the AFM strip will switch the magnetization state of the selected MTJs to anti-parallel states while others remaining unchanged. Then in the second cycle, the MTJs targeting for bit "0" are selected and a SOT current with a proper current density (say in the right-hand direction to write data bit "0") flows through the AFM strip will switch the magnetization state of the selected MTJs to parallel states while the others remaining

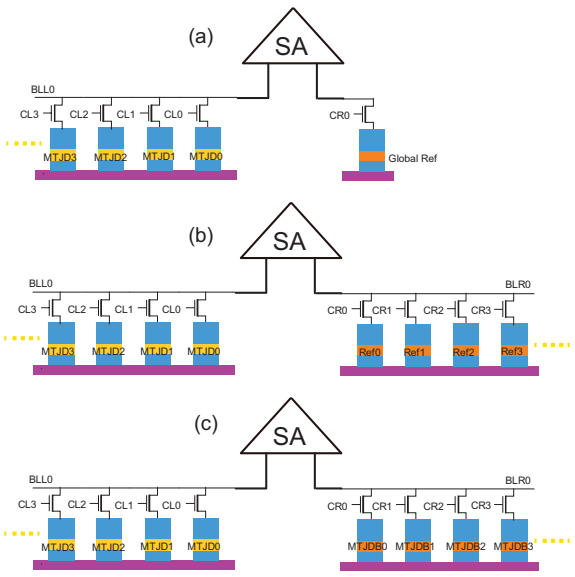

Fig. 4. The schematic of different read approaches; (a) with a single global reference cell; (b) with symmetric reference cells; (c) with symmetric complementary cells.

unchanged. Fig. 3 shows an example of writing a data sequence of "10110100" to one row of MTJs. In the first cycle, MTJ01, MTJ04, MTJ06, MTJ07 are written to "1", and in the second cycle, MTJ00, MTJ02, MTJ03, MTJ05 are written to "0". We can also change the order of writing data "0" and writing data "1". As can be seen, in our proposed synchronous two-step multi-bit write method, only two cycles are needed to write all the MTJs along the same AFM strip.

B. *Symmetric Read Approach*

Fig. 4 shows the schematic of the symmetric read scheme. Here we use a separated pre-charge sense amplifier (sPCSA), as shown in Fig. 2(b). More details on the principle of sPCSA can refer to [25]. Based on the VC-SOT MTJ array structure (see Fig. 4), we can find that the position of the MTJ along the AFM strip will affect the read performance owing to the different parasitic parameters. For example, MTJD0 will have smaller parasitic resistance and capacitance than those of MTJD4 owing to the different current paths. In this case, the read performance of different MTJ cells along the same AFM strip will vary if with a single global reference cell, as shown in Fig. 4(a). Fig. 4(b) shows the symmetric read approach with a train of reference cells with the structure as the same as the data cell strip. In this case, each data cell is sensed with the corresponding symmetric reference cell (e.g., MTJD0-Ref0, MTJD1-Ref1, MTJD2-Ref2, MTJD3-Ref3 in Fig. 4(b)), and both data and reference cells will experience similar parasitic resistance and capacitance conditions. This scheme improves the average read performance by adding more reference cells. Generally, the resistance of the reference cell is the average of the data cell in parallel and anti-parallel states and can be formed either by paralleling four MTJs (two in parallel states and the other two in anti-parallel states) in series [26] or by changing the oxide layer thickness of the MTJ, since the resistance of MTJ is exponentially proportional to the oxide layer thickness [27]. To improve the read margin, one can also utilize the symmetric complementary scheme, as shown in Fig. 4(c), where two cells are employed to store one single bit, sacrificing storage density.

IV. Evaluation Results

In this section, hybrid MTJ/CMOS circuits are designed and evaluated based on a physics-based VC-SOT MTJ compact model (written in Verilog-A language) [24] and a 40nm CMOS design-kit to show the feasibility and performance of our proposed method. The key device parameters (and default values) are listed in Table 1.

Table 1. Parameters and variables of the VC-SOT MTJ model

Parameter	Description	Default Value
K_i	Interfacial anisotropy density	$1.005 \times 10^{-6}\mathrm{KJ/m^2}$
M_s	Saturation magnetization	$1.2 \times 10^{6}\mathrm{A/m}$
ξ	Voltage control coefficient	$75\ \mathrm{fJ/V \cdot m}$
D	Diameter of the free layer	80 nm
t_{OX}	Oxide layer height	1.5 nm – 2.5 nm
t_{FL}	Free layer thickness	1.1 nm
l, w, d	Heavy-metal dimension	100nm, 100nm, 3nm
α	Magnetic damping constant	0.02
θ	Spin Hall angle	0.3
rho	Heavy-metal resistivity	$200\mu\Omega \cdot \mathrm{cm}$
H_{ex}	Exchange bias field	$-7956\ \mathrm{A/m}$
Constant	Description	Default Value
γ	Gyromagnetic ratio	$2.21276\times 10^{5}\mathrm{m/(A{\cdot}s)}$
μ_0	Permeability in free space	$1.2566 \times 10^{6}\mathrm{H/m}$
k_B	Boltzmann constant	$1.38 \times 10^{-23}\mathrm{J/K}$
e	Elementary charge	$1.6 \times 10^{-19}\mathrm{C}$

A. *Transient simulations*

Fig. 5 shows the transient simulation waveforms of our proposed synchronous two-step multi-bit write approach. Here MTJ00, MTJ02, MTJ03, MTJ05 (denoted as type1) are to be written data bit "0" and MTJ01, MTJ04, MTJ06, MTJ07 (denoted as type2) are to be written data bit "1". In the first cycle (0 to 10 ns or 20ns to 30ns), MTJ00, MTJ02, MTJ03, MTJ05 are switched from anti-parallel states to parallel states, while MTJ01, MTJ04, MTJ06, MTJ07 remain unchanged. Then in the second cycle (10ns to 20 ns or 30ns to 40ns), MTJ01, MTJ04, MTJ06, MTJ07 are switched from parallel states to anti-parallel states, while MTJ00, MTJ02, MTJ03, MTJ05 remain unchanged. The transient simulations verify the feasibility of our proposed write approach. Fig. 6 shows the transient simulation waveforms of the read approach for the complementary and symmetric reference cases. Here, for the symmetric reference case, MTJD0, MTJD2, MTJD4, and MTJD6 are in the parallel states, while MTJD1, MTJD3, MTJD5 and MTJD7 are in the anti-parallel states. We can find that all the MTJs have similar read behaviors but with slightly different latency (about 100ps to 150ps). Furthermore, the symmetric reference scheme has similar read performance as the complementary scheme.

B. *Successful Switching Conditions*

As discussed above, the critical SOT write current density depends on the bias voltage applied on the MTJ. In general, it fits in a linear relationship, shown in Fig. 1(d) [24]. Therefore, the switching conditions (between the bias voltage and the SOT

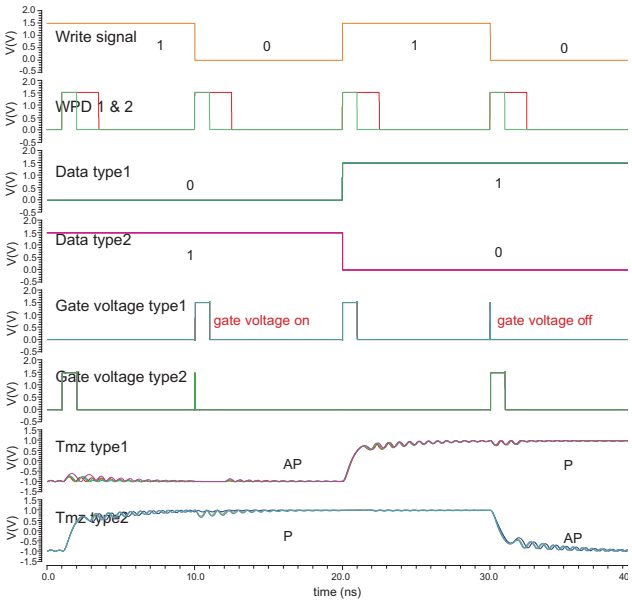

Fig. 5. Transient simulation results of the synchronous two-step multi-bit write approach based on the hybrid circuits.

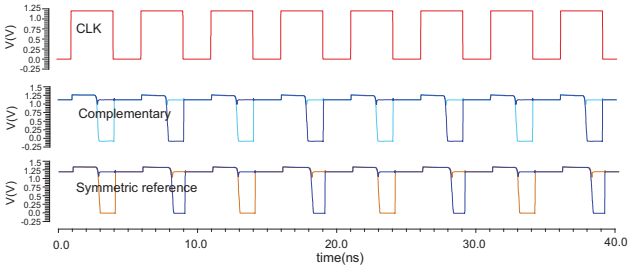

Fig. 6. Transient simulation results of the complementary and symmetric read approach based on the hybrid circuits.

write current) that all the MTJs along the same AFM strip can be switched successfully should be investigated. As shown in Fig. 7, if we sweep the bias voltage from 0.5V to 2.0V and sweep the SOT write voltage from 0.1V to 1.2 V, we can find a phase transition map showing the number of MTJs along the same AFM strip that can be successfully switched. Here in the first cycle, we tend to switch all the MTJs (8 in total) from anti-parallel states to parallel states while in the second cycle, we tend to switch all the MTJs from parallel states to anti-parallel states. We can also find that the phase transition map can be divided into three major regions, including non-switching region (blue), partial-switching region (green and yellow) and successful switching region (red) depending on the combination of the bias voltage and SOT write current. As can be seen from Fig. 7, the SOT write current dominates the MTJ switching behavior and the bias voltage provides an assistance role, corresponding to the physical principle. If the SOT write voltage is below 0.2 V, all the MTJs cannot be switched for any bias voltage. In this case, the magnetization will be in a precessional state [11]. On the other hand, if the SOT write voltage is above 0.3V, a bigger bias voltage will increase the MTJ switching

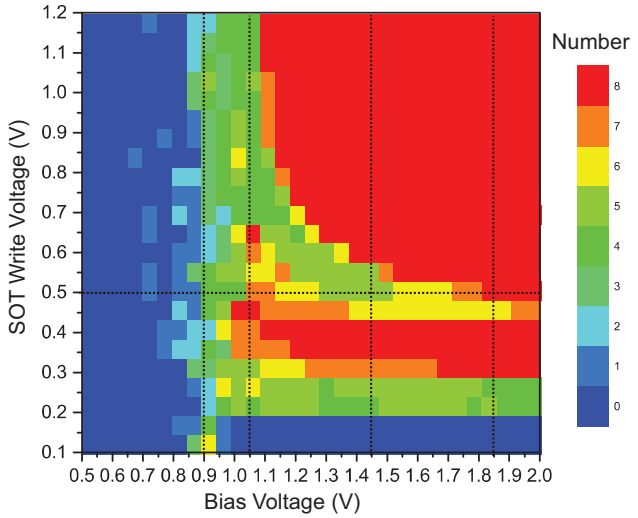

Fig. 7. The relationship between the bias voltage and the SOT write voltage for MTJ switching along the same AFM strip.

probability. More specifically, if we fix the SOT write voltage to be 0.5V (the corresponding SOT current is about 40 μA), but change the bias voltage, we can observe the variation of the MTJ switching probability. For example, Fig. 8 shows the eight MTJs' magnetization switching dynamics with four different bias voltages as 0.9V, 1.05V, 1.45V and 1.85V, respectively (see the dashed lines in Fig. 7). Here the colored square markers denote the position of the MTJs along the AFM strips. Please note here that the SOT induced MTJ magnetization switching is physically a probabilistic event, thus the eight MTJs may have different behaviors in different tries. In addition, the leakage current from the bias voltage will also affect the MTJ switching behaviors, which will be discussed below.

C. *Influence of Leakage Currens*

It should be noted that the MTJ resistance (from KΩ to MΩ, depending on the oxide barrier thickness) is limited in practice and the bias voltage will induce leakage current through the MTJ. Furthermore, the leakage current amplitude depends on the resistance (state) of the MTJ and the amplitude of the bias voltage. Therefore, since multiple MTJs are stacked along a common AFM strip, during the write operation, the MTJs will experience different write current conditions when taking into consideration the leakage currents, as shown in Fig. 9. Fig. 10 shows the leakage current conditions for the eight MTJs along the same AFM strip when writing different data bit patterns. Here the leakage current is calculated by subtracting the SOT write current. As shown in Fig. 10, the curve in blue with triangle markers denotes the case of writing eight MTJs (eight leakage currents) to parallel states; the curve in red with circle markers denotes the case of writing four MTJs (four leakage currents) to parallel states; the curve in black with square markers denotes the case of writing eight MTJs (eight leakage currents) to anti-parallel states; the curve in green with triangle markers denotes the case of writing four MTJs (four leakage currents) to anti-parallel states. Obviously, (a) the last MTJ suffers the biggest accumulated leakage current; (b) given the

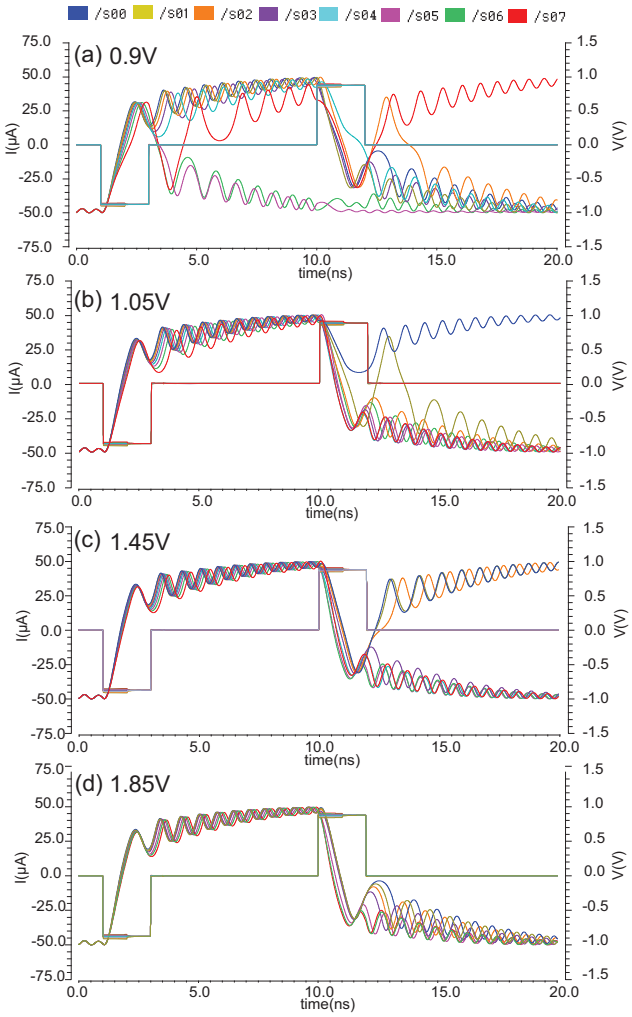

Fig. 8. The magnetization switching dynamics of the 8 MTJs along the same AFM strip corresponding to the four particular cases indicated in Fig. 7.

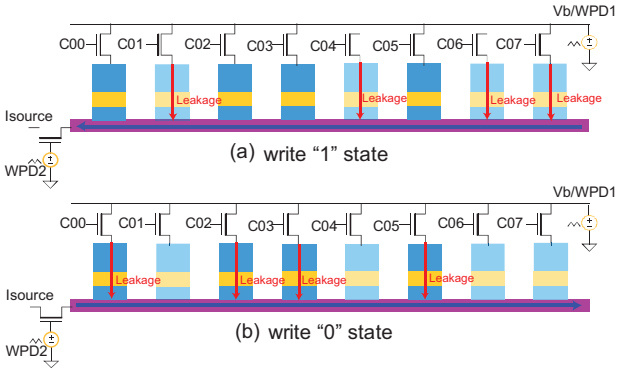

Fig. 9. Illustration of the leakage currents during the write operation; (a) In the first cycle; (b) In the second cycle.

same number of MTJs, the more the parallel states, the bigger the leakage current. Furthermore, Fig. 11 shows the leakage current conditions for the eight MTJs along the same AFM strip with different bias voltages. Obviously, (a) a larger bias voltage

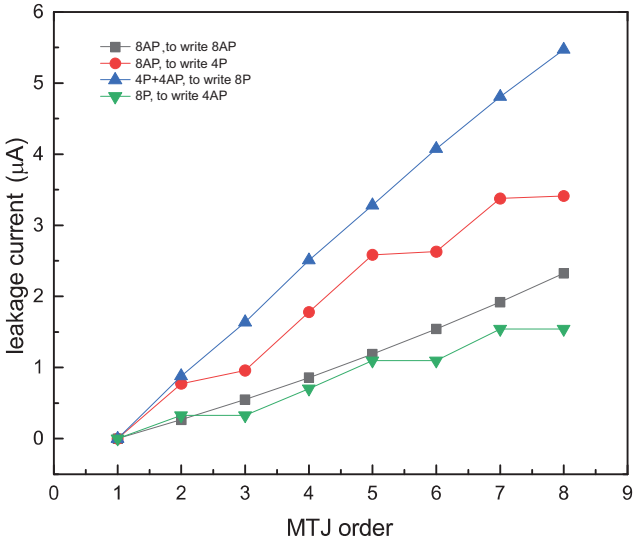

Fig. 10. The leakage current conditions for different MTJs along the AFM strips under different data bit patterns.

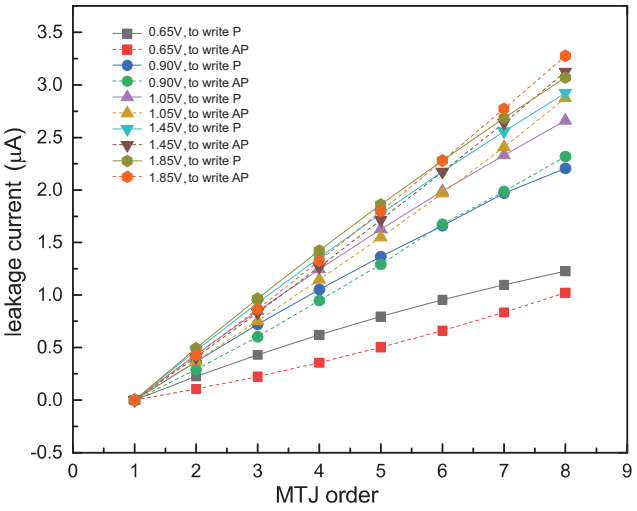

Fig. 11. The leakage current conditions for different MTJs along the AFM strips under different bias voltages.

will induce larger leakage current; (b) since the SOT write current direction for writing data "0" and "1" is opposite, the leakage current conditions are also different. In our design, the leakage current will actually assist the MTJ magnetization switching during the write operations but with extra power consumption. Furthermore, owing to the different leakage current conditions of the MTJs along the AFM strip, it also induce extra power consumption if considering the worst-case. In addition, the leakage current may bring oxide breakdown risk. Therefore, we generally prefer to remove/reduce leakage current by increasing the oxide barrier thickness of the MTJ.

V. Conclusions and Perspectives

In this paper, we have proposed an advanced high-density, low-power, high-speed VC-SOT memory associate with novel

synchronous two-step write and symmetric read techniques. Hybrid circuits were designed and evaluated based on our in-house developed VC-SOT MTJ model and a 40nm CMOS design-kit to show the feasibility and performance of our proposed design. Comprehensive analysis was then performed on the switching conditions and leakage currents and their influences on the robustness of the proposed VC-SOT memory. Although more efforts are required, in particular, on the process technology and device integration, this work presents some novel design methods and may pave the way for advanced spin memory and logic design beyond STT-MRAM. For example, the VC-SOT MTJ device is very suitable for high-throughput processing-in-memory application. Since the VC-SOT MTJ device has two inputs for each cell, i.e., the bias voltage and the SOT write current. In this case, logic functions can be directly implemented through exploiting the selective switching behaviors with a combination of the two inputs.

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