DATE PhD Forum 2020

The PhD Forum of the DATE Conference is a poster session and a buffet style dinner hosted by the European Design Automation Association (EDAA), the ACM Special Interest Group on Design Automation (SIGDA), and the IEEE Council on Electronic Design Automation (CEDA). The purpose of the PhD Forum is to offer a forum for PhD students to discuss their thesis and research work with people of the design automation and system design community. It represents a good opportunity for students to get exposure on the job market and to receive valuable feedback on their work.

The DATE PhD Forum is associated with the DATE 2020 Welcome Reception and will take place on Monday, March 9, 2020, from 1800 - 2100 at the DATE venue in the Lunch Area. All registered conference delegates and exhibition visitors are kindly invited.

Robert Wille, Johannes Kepler University Linz (Chair, DATE PhD Forum 2020)

PhD Forum Committee
Juergen Alt, Intel Germany
Iris Bahar, Brown University
Davide Bertozzi, University of Ferrara
Armin Biere, Johannes Kepler University Linz
Philip Brisk, University of California, Riverside
Luigi Carro, UFRGS
Anupam Chattopadhyay, Nanyang Technological University
Rolf Drechsler, University of Bremen/DFKI
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Ian Harris, University of California Irvine
Tsung-Yi Ho, National Tsing Hua University
Oliver Keszocze, Friedrich-Alexander University Erlangen
Martin Omana, DEI - University of Bologna
Felipe Rocha da Rosa, UFRGS
Andreas Steininger, Vienna University of Technology
Sander Stuijk, Eindhoven University
Daniel Tille, Infineon Technologies
Shigeru Yamashita, Ritsumeikan University

Admitted Presentations

FM01.1.1 Networks-on-Chip for Heterogeneous 3D Systems-on-Chip
Jan Moritz Joseph, Otto-von-Guericke Universität Magdeburg, Germany

FM01.1.2 Intelligent Scheduling Algorithms for Energy Optimization in Smart Grid
Nilotpal Chakraborty, IIT Patna, India

FM01.1.3 Enhanced Detection and Prevention Techniques to Ensure a Secured Hardware with Improved Performance Metrics
Sree Ranjani, IIT Madras, India

FM01.1.4 QoS-aware Cross-layer Reliability-integrated Design of Heterogeneous Embedded Systems
Siva Satyendra Sahoo, Technische Universität Dresden, Germany

FM01.1.5 Design and implementation aspects of post-quantum cryptography
Angshuman Karmakar, imec-COSIC, KU Leuven, Belgium

FM01.1.6 Security implications of power management systems in multicore devices
Philipp Miedl, ETH Zurich, Switzerland

FM01.1.7 Towards Sustainable Logic Encryption in an Age of Mistrust
Amin Rezaei, Northwestern University, United States

FM01.1.8 Architectures And Automation For Beyond-CMOS Technologies
Debjyoti Bhattacharjee, Nanyang Technological University, Singapore

FM01.1.9 On-chip Thermal Monitoring and Optimization for New-generation Manycore Systems
Mengquan Li, Nanyang Technological University, Singapore

FM01.1.10 Instruction-Level Abstraction (ILA): A Uniform Specification for System-on-Chip (SoC) Verification
Bo-Yuan Huang, Student, Taiwan

FM01.1.11 A Formal Approach towards Pattern Guided Scheduling in Embedded Control Systems
Sumana Ghosh, TUM, Germany

FM01.1.12 Design and Evaluation of Ethernet-based E/E-Architectures for Latency- and Safety-critical Applications
Fedor Smirnov, Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), Germany

FM01.1.13 System-Level Mapping, Analysis, and Management of Real-Time Applications in Many-Core Systems
Behnaz Pourmohseni, Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), Germany

FM01.1.14 Self Aware Nature Inspired Approaches Ensuring Embedded Security
Krishnendu Guha, University of Calcutta, India

FM01.1.15 CAD Frameworks for Advancing Design IP Protection
Satwik Patnaik, New York University, United States

FM01.1.16 Design Automation for Error-Tolerant Sample Preparation with Digital Microfluidic Biochips
Sudip Poddar, National Taiwan University of Science and Technology, Taiwan

FM01.1.17 Automated Test Generation with SystemC Designs for Pre-Silicon Validation
Bin Lin, Portland State University, United States

FM01.1.18 Dynamic Energy Management of Mixed-Criticality Real-Time Networks-on-Chip
Thawra Kadeed, TU Braunschweig, Germany

FM01.1.19 Proving Correctness of Industrial Multipliers using Symbolic Computer Algebra
Alireza Mahzoon, University of Bremen, Germany

FM01.1.20 A Holistic Approach to Functional Safety for Networked Cyber-Physical Systems
Enrico Fraccaroli, Università degli Studi di Verona, Italy

FM01.1.21 Automated Analysis of Virtual Prototypes at the Electronic System Level–Design Understanding and Applications–
Mehran Goli, University of Bremen, Germany

FM01.1.22 A Novel Test Flow for Approximate Digital Circuits
Marcello Traiola, LIRMM, France

FM01.1.23 Heterogeneous HW/SW Techniques for Reliable Systems
Florian Kriebel, Vienna University of Technology, Austria

FM01.1.24 Efficient Scale-Up and Scale-Out of Beam Longitudinal Dynamics Simulations
Konstantinos Iliakis, National Technical University of Athens, Greece

FM01.1.25 On Improving Statistical Model Checking by Qualitative Verification
Tim Gonschorek, Otto von Guericke University Magdeburg, Germany

FM01.1.26 Verifying Multipliers using Computer Algebra
Daniela Kaufmann, Johannes Kepler University, Austria

FM01.1.27 Energy-efficient Photonic Architectures for Large-scale Computing
Dharanidhar Dang, University of California, San Diego, United States

FM01.1.28 Energy Efficient and Reliable Deep Learning Accelerator Design
Jeff Zhang, New York University, United States

FM01.1.29 Connecting the Dots: From Theory to Application of IP Protection
Abhrajit Sengupta, New York University, United States

FM01.1.30 Realistic Scheduling Models and Analyses for Advanced Real-Time Embedded Systems
Georg von der Brüggen, TU Dortmund University, Germany

FM01.1.31 Energy-efficient and Performance-driven Implementation of Computational Pipelines of Whole Genome Sequencing on Embedded Platforms
Sidharth Maheshwari, Newcastle University, United Kingdom

FM01.1.32 Complexity Reduction for Embedded System-Level Design
Valentina Richthammer, Ulm University, Germany