DATE Best Paper Awards

Each year the Design, Automation and Test in Europe Conference presents awards to the authors of the best papers. The selection is performed by the award committee composed of the Track Chairs Franco Fummi, Ian O'Connor, Cristiana Bolchini and Valeria Bertacco and the following members: Philip Brisk, Andrea Calimera, Suhaib Fahmy, Frédéric Mallet, Ingo Sander, Ayse Kivilcim Coskun, Pascal Vivet, Jaume Abella, Georges Gielen, Tulika Mitra, Graziano Pravadelli, Dirk Ziegenbein.

The DATE 2019 best papers are:

D Track Enhancing Reliability of STT-MRAM Caches by Eliminating Read Disturbance Accumulation

*Elham Cheshmikhani*¹, *Hamed Farbeh*², *Hossein Asadi*¹ 1 Sharif University of Technology, 2 Amirkabir University of Technology

A Track

When Capacitors Attack: Formal Method Driven Design and Detection of Charge-Domain Trojans

Xiaolong Guo¹, Huifeng Zhu², Yier Jin¹, Xuan Zhang² 1 University of Florida, 2 Washington University in St. Louis

T Track

Error-Shielded Register Renaming Subsystem for a Dynamically Scheduled Out-of-Order Core

Ron Gabor¹, Yiannakis Sazeides², Arkady Bramnik¹, Alexandros Andreou², Chrysostomos Nicopoulos², Yanfeng Li², Karyofyllis Patsidis³, Dimitris Konstantinou³, Giorgos Dimitrakopoulos 1 Intel, 2 University of Cyprus, 3 Democritus University of Thrace

E Track

Data Subsetting: A Data-Centric Approach to Approximate Computing

Younghoon Kim¹, Swagath Venkataramani², Nitin Chandrachoodan³, Anand Raghunathan¹ 1 Purdue University, 2 IBM T. J. Watson Research Center, 3 Indian Institute of Technology Madras

Best Paper Award Nominations

D Track

HotR: Alleviating Read/Write Interference with Hot Read Data Replication for Flash Storage Suzhen Wu, Weiwei Zhang, Bo Mao Xiamen University

High-performance, Energy-efficient, Fault-tolerant Network-on-Chip Design using Reinforcement Learning *Ke Wang¹, Ahmed Louri¹, Avinash Karanth², Razvan Bunescu²* 1 George Washington University, 2 Ohio University

fbPDR: In-depth combination of forward and backward analysis in Property Directed Reachability *Tobias Seufert, Christoph Scholl* University Freiburg

CoDAPT: A Concurrent Data And Power Transceiver for Fully Wireless 3D-ICs Benjamin Fletcher¹, Shidhartha Das², Terrence Mark¹ 1 University of Southampton, 2 ARM Ltd.

Automated Activation of Multiple Targets in RTL Models using Concolic Testing Yangdi Liu, Alif Ahmed, Prabhat Mishra University of Florida

PINT: Polynomial in Temperature Decode Weights in a Neuromorphic Architecture Scott Reid, Antonio Montoya, Kwabena Boahen Stanford University

IR-aware Power Net Routing for Multi-Voltage Mixed-Signal Design Shuo-Hui Wang, Yen-Yu Su, Guan-Hong Liou, Mark Po-Hung Lin National Chung Cheng University

Improving the DRAM Access Efficiency for Matrix Multiplication on Multicore Accelerators Sheng Ma, Yang Guo, Shenggang Chen, Libo Huang, Zhiying Wang National University of Defense Technology

> "Unobserved Corner" Prediction: Reducing Timing Analysis Effort for Faster Design Convergence in Advanced-Node Design Andrew Kahng, Uday Mallappa, Lawrence Saul, Shangyuan Tong University of California San Diego

Enhancing Reliability of STT-MRAM Caches by Eliminating Read Disturbance Accumulation Elham Cheshmikhani¹, Hamed Farbeh², Hossein Asadi¹ 1 Sharif University of Technology, 2 Amirkabir University of Technology KC2: Key-Condition Crunching for Fast Sequential Circuit Deobfuscation
Kaveh Shamsi¹, Meng Li², David Z. Pan², Yier Jin¹
1 University of Florida, 2 University of Texas, Austin

NeuADC: Neural Network-Inspired RRAM-Based Synthesizable Analog-to-Digital Conversion with Reconfigurable Quantization Support *Weidong Cao, Xin He, Ayan Chakrabarti, Xuan Zhang* Washington University in St Louis

A Track

Laelaps: An Energy-Efficient Seizure Detection Algorithm from Long-term Human iEEG Recordings without False Alarms Alessio Burrello¹, Lukas Cavigelli¹, Kaspar Schindler², Luca Benini¹, Abbas Rahimi¹ 1 ETH Zurich, 2 University Bern

Block-Flushing: A Block-based Washing Algorithm for Programmable Microfluidic Devices Yu-Huei Lin¹, Tsung-Yi Ho¹, Bing Li², Ulf Schlichtmann² 1 National Tsing Hua University, 2 Technical University of Munich

> When Capacitors Attack: Formal Method Driven Design and Detection of Charge-Domain Trojans
> *Xiaolong Guo¹, Huifeng Zhu², Yier Jin¹, Xuan Zhang²* 1 University of Florida, 2 Washington University in St. Louis

T Track

New method for the automated massive characterization of Bias Temperature Instability in CMOS transistors Pablo Saraza-Canflanca¹, Javier Diaz-Fortuny², Rafael Castro-Lopez¹, Elisenda Roca¹, Javier Martin-Martinez², Rosana Rodriguez², Montserrat Nafria², Francisco Vidal Fernandez² 1 Universidad de Sevilla, 2 Universidad Autonoma de Barcelona

Error-Shielded Register Renaming Subsystem for a Dynamically Scheduled Out-of-Order Core Ron Gabor¹, Yiannakis Sazeides², Arkady Bramnik¹, Alexandros Andreou², Chrysostomos Nicopoulos², Yanfeng Li², Karyofyllis Patsidis³, Dimitris Konstantinou³, Giorgos Dimitrakopoulos³ 1 Intel, 2 University of Cyprus, 3 Democritus University of Thrace

E Track

Better Late Than Never Verification of Embedded Systems After Deployment Martin Ring¹, Fritjof Bornebusch¹, Christoph Lüth², Robert Wille³, Rolf Drechsler² 1 DFKI, 2 DFKI and University of Bremen, 3 Johannes Kepler University Linz

Data Subsetting: A Data-Centric Approach to Approximate Computing Younghoon Kim¹, Swagath Venkataramani², Nitin Chandrachoodan³, Anand Raghunathan¹ 1 Purdue University, 2 IBM T. J. Watson Research Center, 3 Indian Institute of Technology Madras

Exploiting System Dynamics for Resource-Efficient Automotive CPS Design Leslie Maldonado¹, Wanli Chang², Debayan Roy³, Anuradha Annaswamy¹, Dip Goswami⁴, Samarjit Chakraborty³
1 Massachusetts Institute of Technology, 2 University of York,
3 Technical University of Munich, 4 Eindhoven University of Technology

Self-Supervised Quantization of Pre-Trained Neural Networks for Multiplierless Acceleration Sebastian Vogel¹, Jannik Springer¹, Andre Guntoro¹, Gerd Ascheid² 1 Robert Bosch GmbH, 2 RWTH Aachen University