AMS Verification Methodology regarding Supply Modulation in RF SoCs induced by Digital Standard Cells

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***Abstract*—Nanoscale CMOS enables and forces the use of digital-centric RF architectures, where timing resolution is traded for analog resolution. Simultaneously, digital circuits act as aggressors endangering the performance of the time continuous digital and analog parts. The switching activities of logic cells result in power supply variations which lead to jitter in the digital signal paths and causes interferers coupling to the analog paths, appearing as e.g. phase noise, crosstalk, unwanted frequency conversion, etc. Since todays commonly used AMS simulation methods are limited to register-transfer level (RTL) models for the digital domain, the electrical behavior caused by digital switching is not considered. Here, a method for modeling logic cells with regard to power supply noise is presented using the available characterization data of a standard cell library. It covers the influence of switching on the supply voltage as well as influences of supply variations on the digital path delay and their feedthrough to blocks of the RF domain. A fast event-driven simulation of an entire AMS system regarding the mentioned aspects is enabled. The method is demonstrated on a digital-centric transmitter to detect the effects on system level.**

I. Introduction

Modern communication systems-on-chip (SoCs) are rising in complexity due to the support of multiple radio standards in one single chip. To reach this goal without an unreasonable increase of the chip area, the development of digital-centric nanoscale CMOS RF front-ends is currently subject of research activities. They perform most of their signal processing in the digital instead of the analog domain and therefore are accessible for shrinking with smaller CMOS technology nodes. Examples for components of such designs are huge DSP blocks, all-digital PLLs, or RF-DACs.

With the transition to complex AMS SoCs as digital-centric RF architectures new error sources occur, endangering the systems functionality. The digital components are very sensitive to jitter caused by supply modulations as described in [1], so these variations in the digital domain directly hit the performance of the analog signal. A major hazard regarding the quality of the signal is the generation of phase noise in digital paths or interferers, coupling through supply nets or the substrate into other components of the chip.

The prevention of these effects is an important task for pre-tapeout AMS system verification, but established mixed-signal simulation approaches for toplevel simulation usually do not consider the power supply of digital logic cells.

The drawback of todays verification simulations for AMS systems is that they either focus on pure digital or analog simulation methods. Digital RTL simulation only considers the functional behavior of the logic gates which makes them appropriate for simulation of complex digital parts in reasonable time, but neglects electrical impacts. Analog node-based simulation delivers accurate physical models which allow a sufficient simulation of electrical interaction with acceptable accuracy, but leads to a poor simulation performance.

Since there is no suitable method for fast and accurate verification simulation of test cases considering performance aspects and interaction between analog and digital domain, this work targets on a trade-off between analog and digital simulation approaches.

Some approaches like [2]–[4] enable methods to cover supply variations, but show drawbacks or neglects in different issues. The presented methods are only tailored for the digital domain instead of AMS systems and either abstract on a too high level, or require high efforts for prior characterization simulations. Also, they only regard the influence of supply variations on cell delays or switching behavior on the supply, but not the mutual relation of both, or the influence of switching behavior on neighboring analog blocks.

This work proposes an efficient method to model the current consumption from the supply net caused by the switching behavior of single digital logic cells and the retroactive effect of the resulting IR-drop on the switching delay of surrounding cells connected to the same supply. The simulation method is event-driven for both, analog and digital circuit blocks and therefore avoids costly solving of differential equations.

Since digital blocks are commonly created in an automated synthesis flow using digital standard cell libraries, the models for digital blocks are based on the characterization data provided through liberty files by the standard cell IP distributor.

In section II, the background of power supply modulation is discussed. Section III presents the developed methodology. In section IV, the application example and results of this work are presented. Section V gives a conclusion.

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II. Supply Modulation and Delay Variation

In logic cells, the current consumption depends on the input transition and the output load. With every switching event, the gate capacitances of subsequent logic cells are charged or uncharged, leading to an IR-drop on the supply or ground bouncing. A variation in supply voltage level leads to a deviating transition on the output so that the switching level for driven gates is reached earlier or later [5].

The resulting delay is proportional to the voltage drop and propagates through the signal paths, causing further switching events at different points in time. This leads to a dynamic time-variant state on the supply net, that can be described as power supply noise (PSN).

Depending on the circuit's distribution, periodicity, and activity, this leads to spurs on the supply net and jitter or phase noise on the digital signal paths.

III. Modeling Methodology

A. Liberty Data Extraction

The liberty standard characterization files, usually taken for static timing analysis in standard cell synthesis flows, contain the delay, transition time, and power consumption parameters for provided standard cell libraries. These parameters are formated as lookup tables sorted by the input transition and the load capacitance. The external power consumption, necessary to charge subsequent gate capacitances, is not given, but can easily be calculated knowing the supply voltage and total load capacitance (see sec. III-C). Usually, these datasets are created for different PVT (process, voltage, temperature) corners.

Since the liberty files already contain all relevant data for the modeling purpose of this work, no complex parameter extraction simulation for all used standard cells has to be done. The relevant characterization data from the discrete lookup table values can be loaded for the related model blocks in a preprocessing step and are linearly interpolated during simulation runtime.

B. Simulation Method

To simulate the developed models, the widely spread Cadence design framework is used. This has the advantage that the presented modeling methods can easily be included into the genuine toplevel design so that available schematics and netlists can be reused. To have a sufficient toolset for describing the standard cell functionality and to model the consumption and timing behavior, the cell descriptions are written in SystemVerilog HDL [6]. This enables user-defined data types, net types, and resolution functions to pass the data between circuit blocks. Also, a direct programming interface to C++ (C-DPI) is provided, which allows to expand the languages functionality by C function calls.

The available liberty timing and power consumption datasets for the according standard cell blocks are read in during the initialization step of the simulation.

Due to the event-driven character of SystemVerilog simulations, the standard cell blocks and their impact on the supply net are only evaluated when an input signal changes. Besides the mere evaluation of the internal logic function, for our modeling purpose the input transition time and the output load values are needed to calculate the current consumption, the propagation delay, and the output transition time. Here, the simulation benefits from the access of SystemVerilog to the C-DPI. C++ objects are created, which can be accessed through C++ function calls from the SystemVerilog domain during simulation runtime. Due to this, the needed data structures can be passed from one block to another as shown in Fig. 1, even against the flow direction of the digital signal.

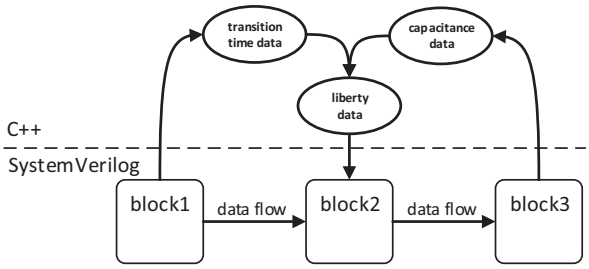


Fig. 1: Data propagation through SystemVerilog and C++ domain.

To model the supply net, a special shared C++ object was created, which is introduced to and can be accessed by all standard cell blocks. This configuration is shown in Fig. 2. When the activity of a standard cell is registered, the evaluation algorithm reads the transition times from the switched input, the summed output capacitances, and the voltage value on the supply net. Based on these parameters, the current consumption of the cell is derived from the prepared liberty lookup tables, and regarding the summed current of all cells, the offset in the voltage value is updated. The changed net voltage value can then be read by all standard cell blocks at the occurrence of the next switching event. The power estimation algorithm is explained more detailed in section III-C. Further, the transition time of the output signal is determined and passed to the subsequent cells.

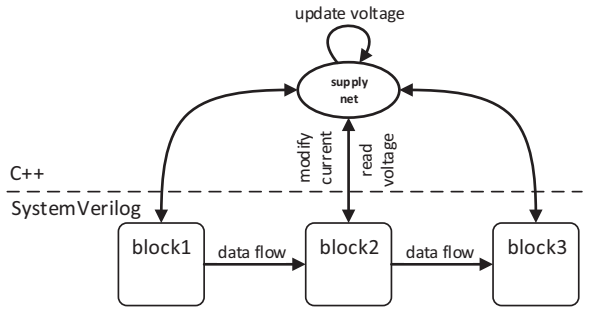


Fig. 2: Supply net object in C++ domain.

C. Supply Current Estimation

The key aspect of this work is the modeling of the supply voltage variations due to the current consumption of logic cells. According to the liberty format, we distinguish three

contributions in the current consumption: the leakage current, the switching current, and the internal current. The composition of the total consumption is depicted in Fig. 3. The active time of the cell is separated into the time spans input transition time (t_1), delay (t_2) and output transition time (t_3), where the current is assumed constant to reduce the number of generated events.

The leakage current is calculated from the given static leakage consumption depending on the supply voltage level.

The switching current is separated for changes of the input state during the input transition time t_1, and for changes at the output during the transition time t_3. The currents at inputs relate to the internal power consumption in the liberty file only concerning the affected pin. Changes at the output consider the current i_{VDD} to load the output capacitances $C_{L,i}$, calculated as

$$i_{VDD} = \frac{V_{DD} \cdot \sum C_{L,i}}{t_3}. \quad (1)$$

The internal current of the cell is based on the given liberty file's internal power consumption of the output caused by a state change on a certain input, which is considered to flow during the whole active time of the cell (t_1 till t_3).

For every step in current consumption i_x, a SystemVerilog event is created to increase or reduce the total current value in the supply net and the voltage level is updated so that the new values are available for all other cells when calculating their consumption, delay, and transition times.

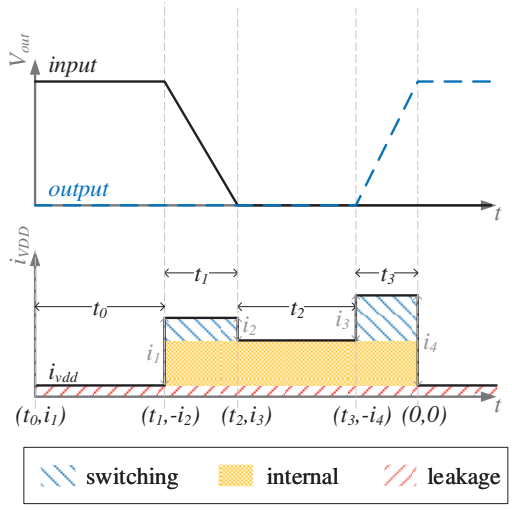


Fig. 3: Estimation of supply current contributions.

IV. Simulation Results

A radio-frequency digital-to-analog conversion (RF-DAC) transmitter is used to demonstrate the presented modeling approach. An RF-DAC transmitter performs a direct conversion from the digital baseband signals to the analog RF domain. The design investigated in this work has been introduced in [7]. It consists of a digital core, which receives the digital baseband signal over a serial interface for further preprocessing, and an analog RF front-end to generate an output signal by switching weighted power amplifier cells.

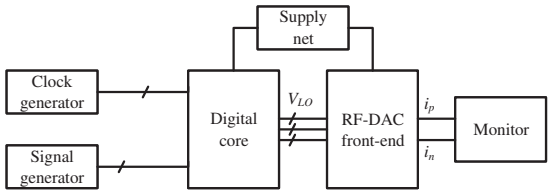
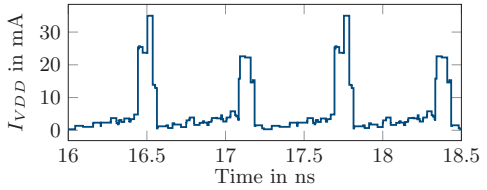
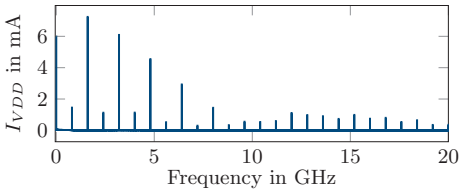


Fig. 4: Testbench for analysis of PSN effects on output current.



(a) Two sample periods of the supply current waveform.



(b) Frequency spectrum of supply current waveform.

Fig. 5: Simulated supply current generated by the chip's digital activity.

Fig. 4 shows the simulated test setup. The supply net was modeled as a simple resistive interconnection, but can be extended, for instance with the data of a parasitic extraction, through the adaptability of the used C++ objects. The signal generator creates the frames for the serial communication to transmit a sinusoidal signal of 3 MHz at the RF output. The sinus signal is sampled at 625 MHz with a 11 bit resolution. The clock generator creates the LO signals at 2.4 GHz needed in the RF front-end.

A. Supply Current caused by Digital Cells

Fig. 5 shows the supply current simulated in the test case described above. After an initial settling the current generates a periodic waveform caused by the cell activity for evaluating the frames of the transmission protocol. The serial interface runs at 800 MHz sampling the data at rising and falling edge. Looking at two sample periods in detail (Fig. 5a) two distinct peaks are identified approximately every 625 ns. As expected the frequency spectrum (Fig. 5b) has components at multiples of the clock frequency of 800 MHz with a major peak at 1.6 GHz.

B. Supply Noise induced Clock Jitter

To demonstrate the modeled effects of dynamic delay variation based on the supply noise generated by the digital core,

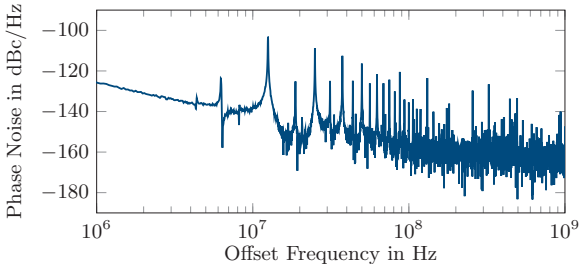


Fig. 6: Phase noise of V_{LO} at power amplifier cell input.

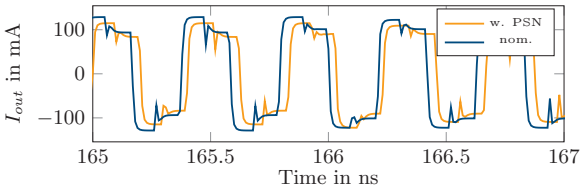


Fig. 7: Comparison output signal w and wo PSN.

the phase noise at the input V_{LO} of the power amplifier cells (Fig. 4) is simulated. Fig. 6 shows the results of the simulation with PSN.

A transient waveform of the generated RF-DAC output currents is shown in Fig. 7. A timing and thus supply noise dependent degeneration of the signal amplitude is clearly noticeable. Additionally, the direct influence of the clock jitter on the switching points in time is seen.

C. Direct PSN Feedthrough to the Output Signal

Fig. 8 shows the expected output spectrum of the RF-DAC front-end for the investigated test setup without induced PSN in blue. Two major frequency contributions at $2.4\,\mathrm{GHz}\pm3\,\mathrm{MHz}$ define the spectrum. Additional disturbances at multiples of approx. $\pm600\,\mathrm{MHz}$ are caused by the sampling of the sinusoidal input signal.

The output spectrum with PSN present is shown in orange. Besides the higher noise floor caused by jitter the additional interferer at $1.6\,\mathrm{GHz}$ and $3.2\,\mathrm{GHz}$ can be clearly identified. These frequency components at $\pm800\,\mathrm{MHz}$ deviation from the LO are the direct feedthrough of the supply noise components identified in section IV-A.

D. Simulation Time

To compare the efficiency of our developed methods to state-of-the-art approaches, we did a back-annotated simulation of a synthesized digital design considering the static timing data of the synthesis result. Table I shows the simulation speeds in simulated system time per simulation duration for the digital core of the presented RF-DAC.

TABLE I: Comparison of simulation speed.

	this work	back-annotated	slowdown
Digital Core	131.6 ns/s	30.3 µs/s	230.24

For the improved supply noise aware modeling achievements, a slowdown factor of only 230.24 can be observed.

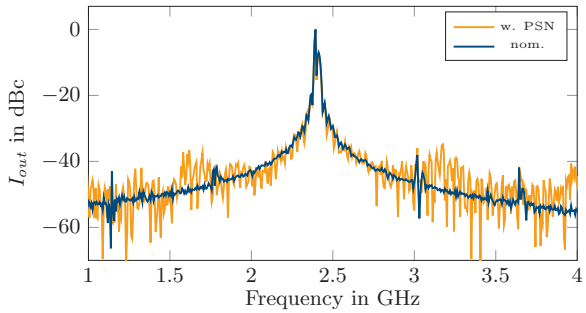


Fig. 8: Simulated output spectrum of RF-DAC transmitter with PSN.

V. Conclusion

A modeling method for simulation of power supply variations induced by digital circuit parts is proposed. This approach does not only consider the consumed current from the supply net and the resulting voltage variation, it also takes into account the voltage variation to recalculate the signal propagation delay of each logic cell. Beside this, a power estimation can be given for the digital parts. Since the common practice in designing complex digital circuits is the utilization of digital standard cell synthesis flows, the use of attached liberty files for timing and power data is proposed to avoid cumbersome characterization simulations.

An RF-DAC transmitter serves as an example to demonstrate the feasibility to diagnose the occurrence and impact of supply modulation in a genuine toplevel design. The simulation speed of the presented method is only slightly lower for the simulation of digital cells compared to commonly used back-annotated Verilog simulations. It is therefore a suitable approach for meaningful toplevel verification including supply noise effects on the design's performance.

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