Abax: 2D/3D Legaliser Supporting Look-Ahead Legalisation and Blockage Strategies

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***Abstract*—Abax is a modern version of the classical Abacus, minimum displacement, greedy legaliser. Abax supports single-tier 2D or 3D legalisation for multiple, logic-on-logic 3D-IC tiers, efficient look-ahead legalisation of intermediate Global Placement (GP) iterations, Hard Macros, Blockages, row density constraints and multiple local cell displacement functions and cell orderings. For 3D-IC, Abax can produce multi-tier 3D-IC placements by performing Legalisation-based Partitioning. For efficient Look-ahead Legalisation, Abax supports two new local displacement cost functions, multi-cell mean and multi-cell total. We show that the classical single-cell displacement and multi-cell total can result in artifacts when legalising early intermediate GPs, and that multi-cell mean is the best candidate for Look-ahead Legalisation. Obstructions, *i.e.* Hard Macros and Blockages are handled by using two strategies. We present legalisation results for the ISPD2014 and ISPD2015 benchmarks, by using GP generated from Eh?Placer, and HPWL measurement by using RippleDP. For 3D, two-tier legalisation we illustrate a ~30% reduction in HPWL for a set of ISPD2014 benchmarks. For 2D legalisation on the ISPD2015 benchmarks, our average HPWL increase over GP is 3.03%, compared to 7.21% of the Eh?Placer legaliser, and 43.16% of the RippleDP legaliser.**

***Index Terms*—EDA, 3D-IC, Placement, Legalisation, Blockages**

I. Introduction

Circuit Placement is a NP-Hard problem [1]. Conventionally confined to 2D, the evolution of 3D-ICs has created new opportunities for placement, promising reduction in Half Perimeter Wirelength (HPWL), and as a consequence power and performance improvements. Originally, 3D-ICs were based on packaging integration using TSVs (Through-Silicon Vias). TSVs provide limited inter-tier integration [2], as their pitch is limited between 5μm and 10μm. The emerging alternative 3D technology, Monolithic 3D, where multiple tiers are fabricated sequentially, offering very high inter-tier integration, with sub-micron MIV (Monolithic Inter-tier Vias) pitches [3]. In addition, recent advances in Wafer-to-Wafer bonding [4], for Stacked Die 3D-ICs, *i.e.* parallel integration, indeed provide high density connectivity, with Hybrid Bond pad pitches between 1.4μm and 1.8μm. Placement for 3D-ICs can provide new scaling opportunities beyond Moore's Law.

The Placement problem is typically subdivided into three steps: Global Placement (GP), Legalisation (LG) and Detailed Placement. Analytical algorithms are very efficient for GP. LG is responsible for moving cells to grid aligned and overlap-free locations, preserving the GP relative cell order, and minimising cell displacement from GP locations. The latter has been shown to provide good correlation between the LG total displacement and resultant post-LG HPWL. In modern Placement flows, look-ahead LG has been proposed [5], *i.e.* intermediate LG steps during GP, as it provides tighter integration between GP and LG and achieves better HPWL by reducing excessive GP component spreading. Look-ahead LG is however more challenging than conventional LG, as the intermediate GP state presents significantly higher density than the final GP state. A final key challenge for LG is handling Hard Macros or Blockages [6] effectively. In 3D Placement [7]–[10], multiple IC tiers are typically superimposed, in order to be able to use a 2D Placer, and a partitioning step is added, which distributes the 2D placed superimposed components across the tiers.

In this paper, we present a 2D/3D modern Legaliser, Abax, based on the classical Abacus [11], minimum displacement legalisation algorithm. Our contribution includes the extension of 2D Legalisation to multiple-tiers, based on minimum 3D displacement, allowing us to perform 3D partitioning legalisation. Our contribution also includes two new local displacement cost functions, multi-cell mean and multi-cell total, which take the movement of all affected cells into account. We show that effective Look-ahead LG is achievable by using the multi-cell mean displacement function, as it can handle a high congestion intermediate GP state better. We also present and evaluate two blockage handling approaches, Sub-Row Assign (SRA) and Sub-Row Re-assign (SRR). Abax supports three sorting orders as well as row density constraints.

II. Abax Legaliser

A. Displacement Cost Functions and Row Search Bound

In the original Abacus, only the displacement, *i.e.* the Euclidean distance from initial to legal position, of the currently legalised cell is considered. We refer to this as single-cell displacement. In the Abacus algorithm, legalised cells may be shifted to new locations, in order to be able to place the current cell to its minimum displacement, legal location. *However, single-cell displacement disregards the movement of already legalised cells.* Based on this observation, in Abax, we implement two additional displacement cost functions, multi-cell mean and multi-cell total [12], which correspond to the mean and total Euclidean distance of all moved cells, including the current one. The global total displacement function, is identical in all three cases, and is used to compare the post-legalisation result.

Displacement cost can be used to reduce the number of examined rows, because exploring a large number of chip rows, is prohibitive. Once a legal location is found, exploring locations with greater displacement cost is not necessary, so a current legalisation solution may be used directly as an upper bound for row search. However, we illustrate [12] that the original single-cell displacement function [11] may lead to suboptimal results, as the row search bound may be too small. On the other hand, multi-cell mean, which considers the mean displacement of all moved cells, produces the most efficient row search bound, as the multi-cell total bound is often too large, consuming execution time unnecessarily.

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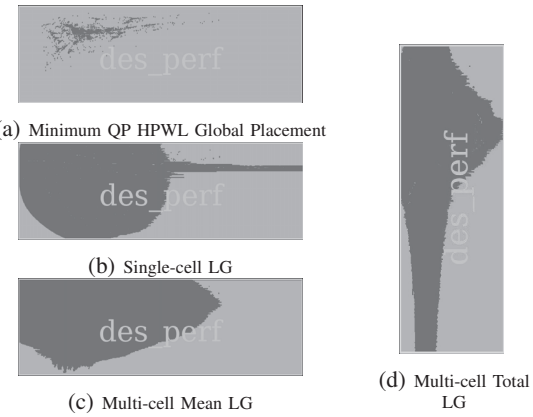
B. Look-Ahead Legalisation

GP cell spreading [13], [14], minimises cells' overlap helping LG to assign cells to legal positions, by influencing the GP result minimally. However, the intermediate GP input of Look-ahead LG (LALG) may not be spread much yet, therefore there will be high-congested areas. This effect will be even more pronounced when running LALG during the early GP iterations. In fact, our findings [12] indicate that early GP Look-Ahead LG may lead to significantly increased total displacement and HPWL, due to LG artifacts, which stem from particular displacement functions. Specifically, single-cell displacement LALG can lead to *horizontal stripe artifacts* (Fig. 1b), *i.e.* uneven row occupancy, with certain rows forming horizontal stripes, whereas multi-cell total displacement LALG may create *vertical stripe artifacts* (Fig. 1d), *i.e.* vertical stripes forming across rows. Such artifacts will lessen the significance of Look-ahead LG results, and its execution time will not be well spent. We have found that the multi-cell mean displacement function is the most suitable for LALG, as its averaging move effect is artifact free, Fig. 1c.



(a) Minimum QP HPWL Global Placement

(b) Single-cell LG

(c) Multi-cell Mean LG

(d) Multi-cell Total LG

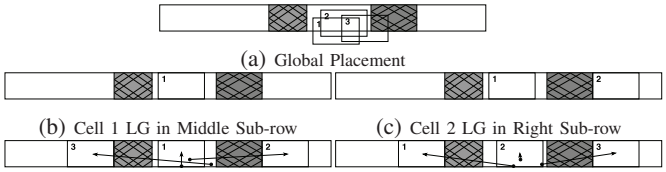
Fig. 1: Single-cell and Multi-cell total Displacement Functions Arifacts

C. Hard-Macro or Blockage Handling

Abax supports two approaches for handling blockages. The first, Sub-Row Assign (SRA), was proposed in [11], but not experimentally evaluated. In the SRA approach, blockage locations divide rows in row segments, called sub-rows, and LG is run on sub-rows, but the legalised cell move between sub-rows is not allowed. The key disadvantage of the SRA approach is that it will only preserve relative GP cell order within sub-rows.

We illustrate GP cell order violation with a contrived example. Fig. 2a shows GP with two blockages, in gray, and three cells, 1, 2 and 3. If we assume increasing x-coordinate order for LG, cells will be considered in the order 1, 2, 3. Figures 2b, 2c illustrate the legalised positions for cells 1 and 2. $Cell$ 1 is legalised in the middle sub-row, where its displacement cost is minimal. As $cell$ 2 cannot fit in the middle sub-row, it is placed in the right sub-row. The last cell, $cell$ 3 will have to be legalised in the left sub-row. Fig. 2d illustrates the SRA-based LG, with arrows representing GP cell displacement. GP cell order is not maintained.

We propose an alternative blockage handling approach, Sub-Row Re-assign (SRR), which allows recursive waves of cell moves between sub-rows when a sub-row becomes full, so as to preserve GP cell order, while ensuring no sub-row overflows. Further on, in contrast to SRA, SRR identifies the nearest, GP order preserving sub-row. This is achieved by observing the furthest legalised cell, depending on the legalisation order. We illustrate SRR operation in the same example, Fig. 2. After $cell$ 1 is legalised, SRR explores two possibilities for $cell$ 2, *i.e.* moving $cell$ 1 to the left sub-row, to make room for $cell$ 2 in the middle sub-row, and to simply place $cell$ 2 in the right sub-row. The latter will be selected, as it presents less displacement, resulting in Fig. 2c, the same as SRA. When $cell$ 3 is legalised by SRR, it will be assigned to its nearest sub-row, *i.e.* the right, shifting $cell$ 2 to the middle one, and $cell$ 1 to the left sub-row, Fig. 2e. The total displacement of the SRR solution is less than SRA. Note that without blockages present, the two approaches will produce the same result. More details about the top-level Abax algorithm are presented in [12].



(a) Global Placement

(b) Cell 1 LG in Middle Sub-row

(c) Cell 2 LG in Right Sub-row

(d) SRA - Cell 3 LG in Left Sub-row

(e) SRR - Cell 3 LG in Right Sub-row

Fig. 2: Row Search Bound Example

D. Abax 3D Partitioning Legalisation

In 3D mode, where multiple tiers are available, Abax effectively performs Partitioning legalisation, *i.e.* legalises and simultaneously partitions across the available tiers, by identifying the minimum 3D displacement position across all tiers, per cell. The row search bound, blockage handling, displacement function and HPWL calculation are all extended to 3D. For 3D displacement and HPWL calculations, the tier to tier spacing and tier index are used to incorporate the z-distance into cell displacement and net 3D HPWL.

In the process of 3D Partitioning legalisation, strongly connected cells may be legalised across tiers, when local tier cell displacement is large, thus the Legaliser will spread cells in all three dimensions. Cells connected across tiers will require vertical inter-tier connections. The total number of these connections, post 3D LG, represents the needed connectivity between tiers, and is similar to the notion of cutsize in classical graph partitioning. The available 3D-IC cutsize depends on both the 3D-IC technology used, *e.g.* TSV-based 3D-IC, Monolithic (sequential) or Stacked Die (parallel integration), as well as the relative size ratio between standard cells and tier to tier connections. In older technologies, *e.g.* 20nm, current Stacked Die capabilities achieve 1 Hybrid Bond pad every three minimum size inverters, thus vertical connectivity is not an issue. However, in recent technologies, *e.g.* 7nm and below, shrinking of standard-cells over Hybrid Bonds presents a new challenge, as available tier to tier connections will decrease.

3D Legalisation does not currently aim to minimise tier to tier connectivity, *i.e.* cutsize, yet focuses on achieving optimal 3D HPWL reduction, by minimising total 3D displacement. Thus, the 3D Legalisation HPWL result is an effective upper bound, and is strongly correlated to its resultant, required cutsize. It is indeed an upper bound, as any reduction in the required cutsize will increase the 3D HPWL, and consequently reduce 3D/2D HPWL gains. This upper bound may be used as a reference point, in a 3D Flow, to explore HPWL, cutsize trade-offs, and identify HPWL solutions with constrained cutsize, between the 2D HPWL and minimum 3D HPWL.

TABLE I: ISPD2015 Benchmarks ΔHPWL Results

Benchmark	GP HPWL (m)	% ΔHPWL Increase								Execution Time (s)							
		RippleDP *	Eh?Placer *	Abax (Ours)						RippleDP *	Eh?Placer *	Abax (Ours)					
				Single-cell		Multi-cell Mean		Multi-cell Total				Single-cell		Multi-cell Mean		Multi-cell Total	
				SRA	SRR	SRA	SRR	SRA	SRR			SRA	SRR	SRA	SRR	SRA	SRR
des_perf_1	1.25	61.57	18.41	4.97	4.97	6.83	6.83	8.35	8.35	16.4	15.3	7.4	13.7	7.2	15.2	160.8	200.6
des_perf_a	1.85	54.41	2.91	1.24	1.24	1.51	1.51	3.26	3.26	20.3	8.6	24.8	47.7	31.7	62.9	148.3	187.6
des_perf_b	1.73	19.12	3.12	1.40	1.40	1.55	1.55	3.54	3.54	11.3	5.5	20.1	38.7	24.3	48.1	123.6	142.8
edit_dist_a	4.72	20.01	1.48	0.74	0.74	0.87	0.87	2.30	2.30	15.0	11.0	20.2	46.7	22.9	59.0	158.3	168.3
fft_2	4.27	50.69	10.33	5.13	5.13	5.38	5.38	11.25	11.25	3.6	1.2	1.9	3.8	1.8	3.8	30.2	33.2
fft_a	8.29	37.81	2.73	1.33	1.33	1.40	1.40	3.58	3.58	10.1	2.1	1.5	3.8	1.7	4.1	13.6	15.3
matrix_mult_1	2.19	56.68	14.82	6.37	6.37	7.61	7.61	15.36	15.36	18.5	16.8	14.4	30.6	14.5	32.1	428.9	510.3
pci_bridge32_a	3.87	36.28	4.04	1.96	1.96	2.11	2.11	4.88	4.88	3.3	0.8	2.2	5.8	2.2	6.5	22.2	25.1
matrix_mult_2	2.25	51.88	13.32	5.44	5.44	6.57	6.57	15.36	15.36	13.5	15.7	15.8	32.8	15.2	32.5	209.9	267.2
superblue14	24.78	-	0.97	1.77	1.34	1.95	1.92	18.69	23.20	-	79.5	223.5	693.8	330.3	866.4	598.7	959.6
Average	-	43.16	7.21	3.03	3.99	3.58	3.57	8.66	9.11	12.44	15.6	33.2	91.7	45.2	113.1	189.5	251.0

TABLE II: ISPD2015 Benchmarks Augmented with Additional Blockages Pattern ΔHPWL Results

Benchmark	GP HPWL (m)	% ΔHPWL Increase								Execution Time (s)							
		RippleDP *	Eh?Placer *	Abax (Ours)						RippleDP *	Eh?Placer *	Abax (ours)					
				Single-cell		Multi-cell Mean		Multi-cell Total				Single-cell		Multi-cell Mean		Multi-cell Total	
				SRA	SRR	SRA	SRR	SRA	SRR			SRA	SRR	SRA	SRR	SRA	SRR
des_perf_1	1.42	45.58	7.33	3.23	3.23	4.57	4.52	8.30	8.30	5.6	4.9	4.9	20.3	9.8	20.3	260.8	348.5
des_perf_a	3.04	35.14	2.04	1.10	1.10	1.33	1.33	2.19	2.19	8.2	7.1	17.4	40.3	18.9	51.9	202.4	398.6
des_perf_b	1.97	12.10	1.59	0.93	0.93	1.00	1.00	1.85	1.12	6.0	4.8	20.2	41.0	28.8	59.8	168.8	301.5
edit_dist_a	6.44	16.62	1.18	0.64	0.62	0.80	0.80	1.23	1.23	11.6	9.0	16.6	39.4	17.7	43.5	195.0	399.3
fft_2	9.25	22.35	4.32	2.29	2.40	2.58	2.58	3.98	3.98	1.7	0.7	1.8	3.7	1.9	3.5	25.3	35.3
fft_a	2.82	7.28	0.37	0.28	0.29	0.29	0.29	0.48	0.48	1.3	1.1	1.5	3.6	1.8	4.0	11.0	21.8
matrix_mult_1	2.67	56.79	13.18	6.53	6.57	8.45	8.33	17.69	17.69	10.7	7.6	9.3	20.0	11.1	26.5	582.8	780.4
pci_bridge32_a	5.28	27.71	2.86	1.61	1.61	1.95	1.95	3.61	3.61	1.9	1.8	1.8	5.3	2.0	6.4	18.9	40.2
pci_bridge32_b	1.06	14.29	1.03	0.66	0.66	0.74	0.74	1.28	1.28	1.4	1.3	1.2	2.8	1.4	3.1	10.4	18.7
matrix_mult_2	2.72	77.61	11.77	5.59	5.68	7.28	7.24	16.05	16.05	8.5	7.6	10.0	20.7	10.7	23.3	531.5	707.0
matrix_mult_c	8.70	16.64	0.63	0.61	3.43	13.57	13.17	1.09	0.70	5.9	3.6	22.0	176.6	45.9	232.2	199.8	993.3
Average	-	30.19	4.21	2.13	2.41	3.87	3.81	5.25	5.15	5.7	4.5	9.7	34.0	13.6	43.1	200.6	367.7

III. Results

We present comparative results from both the ISPD2015 [15] and ISPD2014 [16] benchmarks, ignoring filler cells and regions. GP results are produced by Eh?Placer [14]. We compare the legalisation results of RippleDP [17], Eh?Placer and Abax. To avoid bias, we measure HPWL using RippleDP. There were cases where Eh?Placer was unable to produce a GP, or where RippleDP could not load the legalised result to measure HPWL. We do not present results for such cases. Table I presents the ISPD2015 comparative ΔHPWL results, as for Abax, we also illustrate variation in HPWL depending on the cell displacement function and blockage strategy. We see that although Abax does not directly minimise HPWL but displacement, it achieves, for all benchmarks, except `superblue14`, better HPWL results. Further on, single-cell displacement and SRA produce the best HPWL results. In terms of execution time, Abax is on average slower than the Eh?Placer legaliser. As for Abax, SRR is slower than SRA due to the subsequent re-assignments to sub-rows, and multi-cell total is the slowest local displacement cost function, due to its loose search row bound.

As the ISPD2015 Hard Macro patterns were relatively sparse, to stress the legaliser further, and exhibit a difference between our SRA and SRR blockage handling strategies, we augmented the ISPD2015 benchmarks with additional blockages, applied as a scalable size pattern, which stresses legalisation further. The pattern was applied so that blockages occupy a total of 24% of chip area, and GP and legalisation were performed again. Table II presents the comparative ΔHPWL results for the ISPD2015 benchmarks augmented with the scalable blockages pattern. In this case, we see that the SRA blockage strategy presents better HPWL results, yet the difference is small, despite the displacement difference.

Tables III and IV present the corresponding total displacement results for the ΔHPWL results presented in Tables I and II respectively. These allowing us to draw further conclusions. In Table III, SRA and SRR results are identical as the Hard Macros are sparse and the GP cells are spread out well, with little congestion. However, in Table IV the displacement of the SRR with Multi-cell mean is 7.6% better than SRA, for the same displacement cost function, and about 1.7% better for the average of all three displacement functions. In Table III, for `superblue14`, SRA and SRR present differences due to its large number of Hard Macros. Multi-cell total displacement exhibits the worst results.

Our 2D vs. 3D HPWL comparison results flow for the ISPD2014 benchmarks is the following. We use a flow similar to Shrunk2D [7], but 3D partitioning is performed solely by Abax. To produce the 3D Placement, we perform 2D GP on half the original chip area, and then run Abax on two tiers. We then measure the resultant 3D HPWL and 3D cutsize, *i.e.* number of inter-tier connections. Table V presents the 2D, 3D HPWL comparison. On average, 3D HPWL gains are close to 30%, which is a value claimed by many 3D flows. As discussed in Section II-D, the 3D solution represents an upper bound for HPWL gains and cutsize, obtained solely for minimum GP displacement.

*RippleDP, Eh?Placer results based on binaries provided by their authors.

TABLE III: Total Displacement Comparison for ISPD2015 Benchmarks

Benchmark	Single-cell (cm)		Multi-cell Mean (cm)		Multi-cell Total (cm)	
	SRA	SRR	SRA	SRR	SRA	SRR
des_perf_1	25.63	25.63	15.49	15.49	17.25	17.25
des_perf_a	7.72	7.72	8.33	8.33	10.35	10.35
des_perf_b	7.74	7.74	8.19	8.19	9.57	9.57
edit_dist_a	7.72	7.72	8.33	8.33	11.02	11.02
fft_2	2.74	2.74	2.98	2.98	3.58	3.58
fft_a	2.49	2.49	2.62	2.62	3.02	3.02
matrix_mult_1	18.41	18.41	19.30	19.30	21.25	21.25
matrix_mult_a	12.31	12.31	13.34	13.34	15.68	15.68
pci_bridge32_a	2.19	2.19	2.29	2.29	3.87	3.87
pci_bridge32_b	2.13	2.13	2.24	2.24	2.98	2.98
matrix_mult_2	17.22	17.22	18.48	18.48	20.35	20.35
superblue14	67.12	228.31	76.07	75.62	98.23	268.25
Average	14.45	27.89	14.80	14.77	18.10	32.27

TABLE IV: Total Displacement Comparison for ISPD2015 Benchmarks Augmented with Additional Blockages Pattern

Benchmark	Single-cell (cm)		Multi-cell Mean (cm)		Multi-cell Total (cm)	
	SRA	SRR	SRA	SRR	SRA	SRR
des_perf_1	11.70	11.70	12.51	12.48	14.40	14.40
des_perf_a	8.47	8.47	9.46	9.46	10.00	10.00
des_perf_b	7.29	7.29	7.55	7.55	7.90	7.60
edit_dist_a	10.96	11.03	12.29	12.29	13.24	13.24
fft_2	2.93	2.97	3.29	3.29	3.46	3.46
fft_a	2.18	2.18	2.24	2.24	2.28	2.28
matrix_mult_1	27.65	27.70	23.91	23.73	33.74	33.74
pci_bridge32_a	2.33	2.33	2.49	2.49	2.71	2.71
pci_bridge32_b	2.09	2.09	2.19	2.19	2.37	2.37
matrix_mult_2	27.11	27.26	22.80	22.73	32.61	32.61
matrix_mult_c	22.91	27.91	22.56	14.34	16.68	13.68
Average	11.42	11.90	11.03	10.25	12.67	12.37

TABLE V: Two-tier 3D HPWL vs. 2D HPWL Comparison

Benchmark	HPWL (m)				3D % HPWL Reduct.	Cutsize
	GP		LG			
	2D	3D	2D	3D		
des_perf_1	4.98	3.43	5.00	3.60	-27.97%	69085
des_perf_2	5.14	3.70	5.17	3.82	-26.14%	69062
edit_dist_1	7.36	6.09	8.40	6.38	-24.08%	80880
edit_dist_2	7.34	6.07	8.37	6.35	-24.13%	80672
fft	1.35	1.18	1.93	1.21	-37.44%	20867
matrix_mult	8.58	6.31	10.00	6.97	-30.58%	100831
pci_bridge32_1	1.24	0.94	1.25	0.96	-22.66%	17275
pci_bridge32_2	1.24	0.94	1.26	0.96	-23.25%	17383
Average	-	-	-	-	-27.03%	-

IV. Conclusions and Future Work

We presented a minimum displacement Legaliser, Abax, supporting single or multiple 3D-IC tiers, and a number of additional features, *i.e.* efficient look-ahead legalisation of densely congested, intermediate GP iterations, multiple local displacement cost functions, two blockage strategies, support for row density constraints and multiple cell orders. For 3D partitioning legalisation, we have demonstrated, on a set of ISPD2014 benchmarks, that a ~30% reduction in 3D HPWL is achievable, given no cutsize, *i.e.* tier-to-tier connectivity limits. 3D partitioning legalisation provides a 3D HPWL upper bound, and exposes the required cutsize in order to achieve it. We claim this is an interesting contribution and feature for 3D flows. For 2D legalisation, we have compared our post-legalisation HPWL increase with that of the Eh?Placer and RippleDP legalisers, for a set of the ISPD2015 benchmarks. We have found that our average HPWL increase over GP is 3.03%, compared to 7.21% and 43.16% for Eh?Placer and RippleDP respectively. Results in the two presented blockage strategies illustrate that the more complex strategy, SRR, will show benefits for designs with multiple, dense obstructions. The simpler strategy, SRA, will work very well on average. In terms of future improvements, we aim to improve execution time, by exploiting parallelism in the legalisation process. Futher on, we intent to address new technology node legalisation requirements, *e.g.* 7nm and below, *i.e.* large number of multi-track height cells, simultaneous cutsize and displacement or HPWL minimisation, as well as rendering legalisation aware of double, and multi-patterning metal layer issues.

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