

Co-Synthesis of Floorplanning and Powerplanning in 3D ICs for Multiple Supply Voltage Designs

Jai-Ming Lin and Chien-Yu Huang and Jih-Ying Yang

Department of Electrical Engineering, National Cheng Kung University, Tainan, Taiwan

Email: jmlin@ee.ncku.edu.tw, joy7160076@gmail.com, and jih830630@gmail.com

Abstract—This paper addresses a 3D floorplanning methodology, which considers floorplanning and powerplanning at the same time for Multiple Supply Voltage (MSV) circuits. Physical design becomes more complex for MSV designs since modules with the same power domain have to be placed at close locations in 3D space to facilitate powerplanning and reduce IR-drop, which would deteriorate wirelength. By properly partitioning modules of the same power domain into several voltage islands and increasing overlap area of the voltage islands in contiguous dies, we can reduce routing resource usage without increasing wirelength significantly. Further, unlike previous works, our approach not only can handle a netlist with soft modules and hard modules but also can meet the fixed-outline constraint. The experimental results show that our methodology gets better results than other approach in designs with single voltage domain and is also promising for MSV designs.

I. INTRODUCTION

As technology advances, two-dimensional integrated circuits (2D ICs) face more and more challenges. Many teams are expecting three-dimensional integrated circuits (3D ICs) to break through the bottleneck.

Conventional 3D ICs use through-silicon vias (TSVs) to achieve interconnections in different dies. Dies of a 3D IC are fabricated separately, and then they are aligned and bonded in a packaging house. Because integration density is greatly constrained by the alignment accuracy, this technique is more suitable to integrate off-chip elements. Recently, Monolithic 3D integration [1] has attracted more attention and is considered as a promising technique for 3D ICs. Because Monolithic 3D ICs are completely manufactured inside a foundry, a Monolithic Inter-tier Via (MIV) can be as small as a regular via ($< 100 \mu m$), which facilitates Monolithic 3D ICs to have better performance than TSV-based 3D ICs [22].

Low power has become one of the most important features in many electronic products. To reduce power consumption, Multiple Supply Voltages (MSVs) is a technique which is widely applied to 2D ICs. It divides a circuit into several parts according to different function modes such that voltages in different parts can be adjusted independently, or even be shut down; hence, dynamic power and/or leakage power are saved. Despite the benefit of MSVs, physical design for MSV circuits becomes more complex because power/ground networks in different voltage domains have to be planned, respectively. To reduce routing complexity and save routing resource, floorplanning plays a critical role. If modules with an identical voltage source can be placed at close locations to form a voltage island (VI for short), powerplanning or insertion of level shifters will become easier. However, because modules assigned to each voltage island cannot be packed tightly, the

This work was partially supported by the National Science Council of Taiwan ROC under Grant No. MOST 106-2221-E-006-236-MY2.

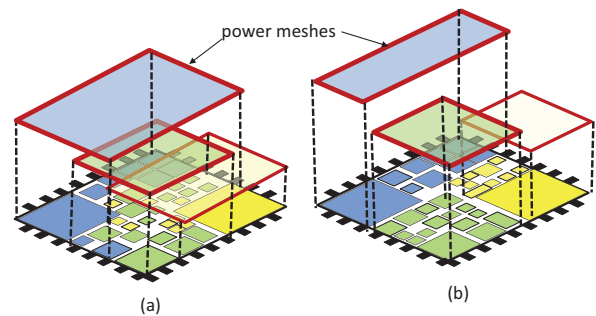


Fig. 1. Floorplans of an MSV design. (a) Worse floorplan due to overlaps of power meshes in different domains. (b) Better floorplan.

voltage island constraint may lead to additional overheads such as a larger chip area and longer signal delay. Fig. 1 shows a floorplan for an MSV design in a 2D plane. Rectangles with the same color denote modules in an identical power domain (PD for short). Since modules in different PDs interleave in the resulting floorplan of Fig. 1 (a), powerplanning is more complex and more routing resource is wasted. On the contrary, all modules in the same PD are placed together to form a complete voltage island (see Fig. 1 (b)). Thus, less routing length is required during powerplanning and better IR-drop may be obtained.

In the MSV-driven floorplanning, number of VIs in each PD has to be carefully determined since it has a lot to do with wirelength and powerplanning complexity. A design applying the MSV technique leads to longer wirelength than that without applying the technique. Besides, the fixed-outline constraint is more difficult to be satisfied. To reduce wirelength under the fixed-outline constraint, we have to generate more VIs to increase placement flexibility. But too many VIs will complicate powerplanning and the procedure of insertion of level shifters, and IR-drop may become worse due to a longer path from a device to a voltage source.

Because a 3D IC integrates more components in a single chip, it may have higher power densities [25]. Power injected from the package below the lowest die has to traverse through a resistive power network distributed in every die of a 3D IC before it can reach devices in upper dies. Hence, upper dies in 3D ICs usually have severe IR-drop problem than lower dies. This problem is more severe in Monolithic 3D ICs because MIVs are relatively small than TSVs and will induce larger resistance [14]. The structure of a power delivery network (PDN) in a 3D IC is shown in Fig. 2 (a). To simplify powerplanning and consider IR-drop for MSV-driven floorplanning in 3D ICs, modules in the same PD have better to be placed at close locations no matter whether they are in

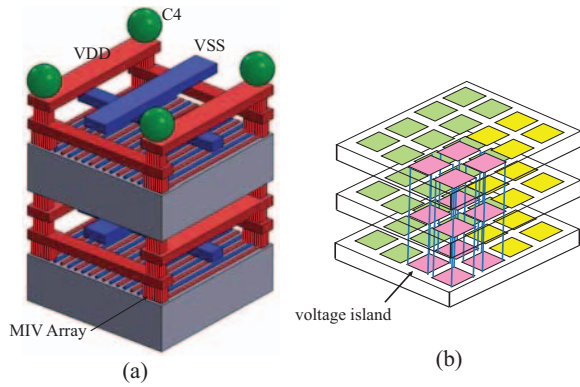


Fig. 2. (a) A power network structure in a 3D IC. (b) An ideal 3D floorplan for the MSV-driven floorplanning.

the same die or in contiguous dies. Fig. 2 (b) shows an example of an ideal 3D floorplan for a MSV design. The modules in an identical PD are grouped together to form a 3D VI such that power meshes in different dies can be connected easily. Hence, less routing resource is required and IR-drop problem in upper dies can be relieved.

Most works use the simulated annealing (SA) algorithm with a representation to handle 3D floorplanning [4], [5], [10], [13], [19], [26], [29], [30]. Only few researches use different approaches to deal with 3D floorplanning such as 3D-STAF [31], Co-place [15], and SAINT [17]. Because powerplanning is greatly impacted by floorplanning, Falkenstern *et al.* [6] propose to consider floorplanning and powerplanning at the same time for 3D ICs. But their approach takes longer runtime because a SA-based approach is adopted. In order to alleviate IR-drop, PDN resource usage, and power consumption in the top die, Panth *et al.* [23] propose a layer assignment approach to balance power distribution in each die of a Monolithic 3D IC.

This paper proposes the first work to handle MSV-driven floorplanning with the fixed-outline constraint for 3D ICs. Although there exist a lot of works targeting on MSV-driven floorplanning in 2D ICs [7], [8], [12], [16], [20], [24], there exists limited study for 3D ICs. Recently, Wang *et al.* [27] propose a methodology to handle MSV-driven floorplanning for 3D network-on-chip (NOC). However, when the number of power domains equals to the number of dies, they assign one power domain to each die to reduce routing resource consumed by a PDN, which may make their approach induce longer wirelength in this situation. Since we propose an iterative procedure to find proper VIs for modules in each PD by an analytical-based approach, our approach not only can reduce wirelength but also can save routing usage required by PDNs. Further, the optimized results are maintained by a two-stage legalization procedure. Unlike previous approaches adopt the SA-based approach to optimize floorplanning without considering the fixed-outline constraint and only handle hard modules, our methodology can meet the fixed-outline constraint and is applicable for a netlist with soft modules and hard modules. The experimental results have demonstrated our methodology can get better floorplans in term of wirelength and power resource usage.

II. PROBLEM FORMULATION

Let $M = \{m_i | i \in \mathbb{Z}^+, 1 \leq i \leq n\}$ denote a set of modules, where n is the number of modules. The width, height, and area of a module m_i are denoted by w_i , h_i , and

A_i , respectively. The aspect ratio of a module m_i is defined as h_i/w_i . Modules in M can be divided into hard modules and soft modules. Given a netlist for an MSV design, the modules in M are divided into p power domains (PDs), and the modules in each PD must be connected to respective power sources. While parts of modules in a PD are placed at contiguous locations, a voltage island is formed. To facilitate powerplanning, the area of the bounding box enclosing each voltage island should be larger than a given value τ , where τ is a user-specified parameter. This is considered as the voltage island constraint. The target is to determine dies, locations and shapes of modules while minimizing total wirelength and routing resource usage under the voltage drop constraint and the fixed-outline constraint.

A. Review of a Floorplanner

Before introducing our method, the section reviews a 3D fixed-outline floorplanner [18] since our approach is extended from the approach. It is composed of the layer assignment stage, global distribution stage, legalization stage, and TSV optimization stage. Layer assignment stage first assigns modules to dies of a 3D IC. Then, the global distribution and legalization stages determine locations and shapes of modules and TSVs in the associated dies. Finally, the locations of TSVs are optimized in the last stage. Due to limited of space, we only detail the global and legalization stages.

1) *Global Distribution Stage*: The global distribution stage divides each die into a set of bins, where the number of bins is determined by the number of modules. Then, a non-linear formulation (1) is solved:

$$\min W + \lambda \sum_b (D(b) - \bar{A}_b)^2, \quad (1)$$

where the first term represents the total wirelength while the second term estimates the utilization of all bins by modules. Let $D(b)$ denote the area covered by modules in a bin b . \bar{A}_b denotes the desirable area of modules in b , which is equal to the total area of modules in a die divided by the number of bins. The stable-log-sum-exp wirelength model [11] and the bell-shaped function [21] are applied to compute W and $D(b)$, respectively. λ is a user-specified weight, whose value is initialized as follows:

$$\lambda = \frac{\sum |\partial W|}{\sum |\partial D(b)|}. \quad (2)$$

(1) is solved by the conjugate gradient (CG for short) method with a dynamic step size [3]. During each iteration in the CG method, the value λ is doubled in order to spread components over a placement region.

2) *Legalization Stage*: To keep the geometric relation of modules in the first stage, the legalization stage first builds a slicing tree according to the distribution of modules in a die. Then, locations and shapes of modules are determined based on the slicing tree. The slicing tree is obtained by recursively bisecting modules and MIVs in a region. Each leaf in a slicing tree comprises a set of modules within a subregion while an internal node denotes the merging direction of its children. The shape curve of each leaf is generated first by the enumerative packing (EP for short) technique [28], where each point in the curve represents a feasible placement outline which can cover the associated modules. Then, the shape curve of an internal node is generated by merging the two shape curves of its child nodes in bottom-up manner until the shape curve of a root is obtained. Finally, the shape and position of each module are determined by top-down backtracing in the slicing tree.

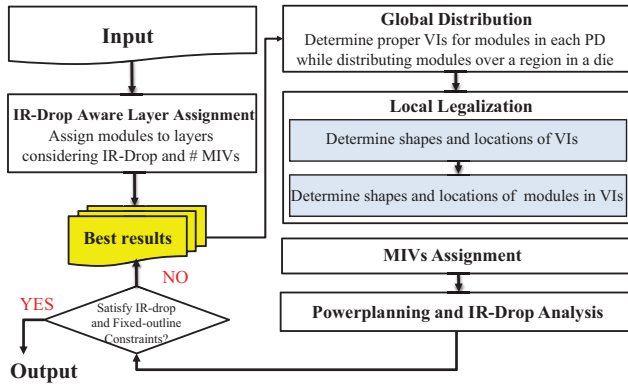


Fig. 3. Flow of our methodology.

III. OUR METHODOLOGY

Our floorplanning methodology includes five stages: (1) IR-drop aware layer assignment stage, (2) global distribution (GD) stage, (3) local legalization (LL) stage, (4) MIV optimization stage, and (5) Powerplanning and IR-drop Analysis stage. Fig. 3 shows the flowchart of our methodology.

The IR-drop aware layer assignment stage assigns modules to different dies in 3D ICs while minimizing the number of cuts under the area balance constraint. Since power distribution in dies of a 3D IC has a great impact on IR-drop, we gradually reduce total power consumption in a die from bottom to top by the SA-based approach. Moreover, because the number of MIVs in each die is determined after this stage, we can roughly determine their locations in the global distribution stage, which can avoid the problem that MIVs are placed at worse locations if they are only considered in the legalization stage. After modules are allocated to dies, the global distribution and legalization stages determine locations and shapes of modules and MIVs in 2D planes to minimize wirelength under the fixed-outline constraint. To facilitate powerplanning for modules in different PDs and minimize wirelength, we first determine the proper number of VIs for modules in a PD and then allocate the locations and shapes of VIs. Next, the locations and shapes of modules in each VI are determined. After the locations of modules are fixed, MIV optimization stage further optimizes locations of MIVs according to the minimum cost maximum flow algorithm. Since the approach has been mentioned in previous papers, we do not detail this stage. Finally, in order to estimate IR-drop of each module, powerplanning is performed which builds a power network to connect modules in each PD to the associated power sources. Then, the voltage of each module is calculated according to the actual power network and power consumption of modules. We will increase the density of power meshes until the IR-drop constraint is satisfied. A floorplan is considered as a bad solution if it requires longer wirelength to complete PDNs.

A. Layer Assignment

In the layer assignment stage, we first apply hMetis [9] to partition modules into K parts, where K is the number of dies in a 3D IC. hMetis minimizes the total number of cuts while balancing area of modules in each partition. Each cut represents a 3D net passing through neighboring partitions, which corresponds to an MIV in a 3D IC. Because hMetis only balances area of modules in each die without considering area occupied by MIVs, we further optimize the result by applying the simulated annealing based algorithm.

The operation of SA is to swap modules in two different dies. The cost function is as follows:

$$cost = N_{MIV} + \alpha \sqrt{\frac{1}{K} \sum_{i=1}^K (A_i - \bar{A}_i)^2} + \beta \sqrt{\frac{1}{K} \sum_{i=1}^K (P_i - P_i^T)^2}, \quad (3)$$

where N_{MIV} denotes the total number of MIVs in a 3D IC. A_i denotes the total area of modules and MIVs in the i -th die while \bar{A} denotes the average area of modules and MIVs in a die, which is equal to total area of modules and MIVs in all dies dividing by K . Similarly, P_i denotes the total power consumption of modules in the i -th die while P_i^T denotes the target power consumption of modules in the i -th die, which is specified by a user. The value of P_i^T is reduced from bottom die to top die to consider IR-drop problem.

B. Global Distribution

This section illustrates our global distribution method which distributes modules over placement regions in all dies. Moreover, modules in the same PD will be placed at as close locations as possible to reduce the number of VIs.

1) *Initial Distribution of Modules and MIVs*: After modules have been assigned to dies in the previous stage, each 3D net is first divided into subnets (i.e., 2D nets) based on the 3D wirelength model [15]. We assume two subnets of a 3D net in every two contiguous dies are connected by a MIV. Then, modules in each PD are clustered by applying the first choice (FC) algorithm to form several groups to ensure modules which are in the same PD and have strong connections will be placed at close locations in the following step. Next, groups and non-clustered modules in the same PD are connected together by an additional pseudo net. Finally, we distribute them over placement regions based on the modified netlist according to the analytical-based approach (see Section II-A1) as follows:

$$\min \{W + \gamma W_s + \lambda \sum_b (D(b) - \bar{A}_b)^2\}, \quad (4)$$

where W_s denotes the wirelength of pseudo nets. Minimizing W_s makes modules in the same PD placed at close locations. γ is a user-specified value. Wirelength of all subnets in a 3D net are estimated separately, and the values are summed up as wirelength W . The wirelength of a subnet on a die is computed by the half perimeter of the bounding box which encloses the terminals of the subnet in that die and any MIV of the subnet in the same die or the die below. The area of an MIV only affects the utilization of a die where it is placed to.

Fig. 4 (a) shows the flowchart to get an initial distribution of modules in all dies, and Fig. 4 (b) and (c) give an example. An initial distribution of modules is shown in Fig. 4 (b). The rectangles with an identical color denote modules in the same PD. Because of module clustering and addition of pseudo nets, modules in an identical PD will be distributed to closer locations as shown in Fig. 4 (c).

2) *Finding Voltage Islands*: In order to consider wirelength, we first distribute modules to placement regions without considering the voltage island constraint. Then, VIs are gradually formed according to the distribution of modules in all dies.

In the beginning, each module is considered as a super module (SM for short). Note that each SM may consist of VIs in different dies. A design with many small VIs may increase complexity in powerplanning and waste more routing resource while constructing PDNs. Hence, if the size of an SM S_1 is small than τ , we will form a large SM by combining it with the closest SM S_2 in an identical PD if it exists,

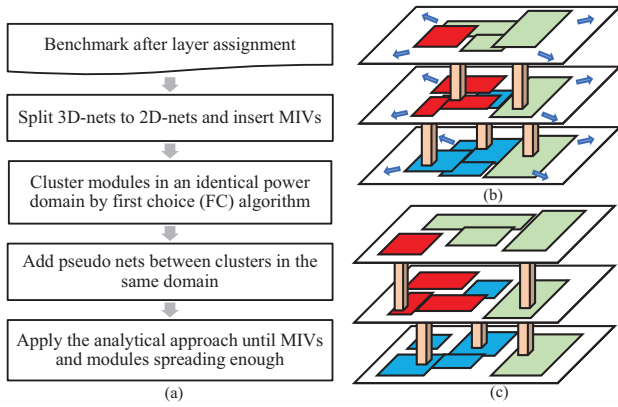


Fig. 4. (a) Flow to distribute modules and MIVs to placement regions in a 3D IC. (b) An initial distribution of modules. (c) Final distribution of modules.

where τ is a user-specified parameter. Note that S_1 and S_2 may be in the same die or in the contiguous dies. Modules in an SM are combined by a pseudo net. Next, all SMs are redistributed again by applying an analytical-based algorithm. The procedure is repeated until the size of each SM is larger than or equal to τ or it cannot find other SM to combine.

Next, we further combine any two SMs if they are in the same PD and their distance is small than δ unless the area of a new SM is too large, where δ is a user-specified parameter. An oversize SM may be difficult to be legalized. Then, all SMs are redistributed by the analytical-based algorithm. The procedure is repeated until we cannot combine any SMs.

C. Legalization

The legalization stage removes overlaps of modules without violating good result obtained in the previous stage. The previous stage has placed modules in an identical PD at close locations to form an SM under consideration of wirelength and powerplanning. Since modules in an SM may be in different dies, we have to place modules as close to their original locations as possible to keep the result during legalization.

Our legalization is composed of two steps. First, the locations and shapes of VIs in all dies are determined, simultaneously. Next, locations and shapes of modules in each VI are determined separately according to the outline of the VI. Although the two steps both try to solve the fixed-outline floorplanning problem, they are resolved by different approaches. All modules in an SM are separated into several VIs if they are in different dies. Each VI is considered as a soft block whose area is equal to the summation of areas of the modules in it. In order to keep the geometric relation of VIs in contiguous dies, we apply an ILP algorithm to determine locations and shapes of VIs. According to the distribution of VIs, we first build a horizontal and a vertical constraint graphs for each die, where each node denotes a VI in the die and each edge denotes the geometric relation of two VIs. Then, the shape and locations of VIs are determined by solving the ILP problem proposed by Lin *et al.* [17], where the objective function is the fixed-outline constraint and the constraints include the geometric relations of VIs and their shape constraints. After the outline of each VI is determined, we build a slicing tree according to the geometric relation of modules inside the VI. Then the locations and shapes of modules in the VI are determined by performing bottom-up curve merging and top-down backtracing operations in the tree (see Section II-A2).

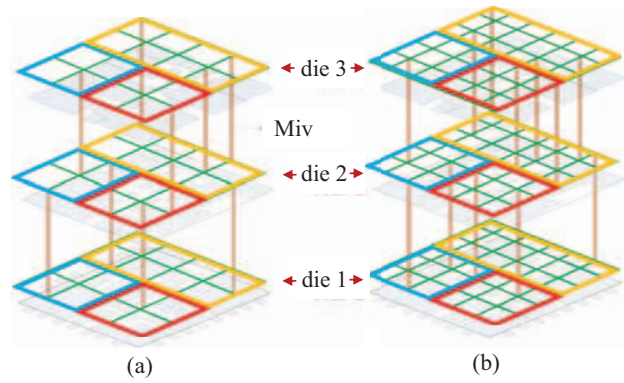


Fig. 5. Increase densities of a power mesh to satisfy IR-drop constraint. (a) Small density. (b) Larger density.

TABLE I
COMPARISON OF WIRELENGTH, PRA AND RUNTIME IN SINGLE POWER DOMAIN.

Cir.	Falkenstern <i>et al.</i> [6]			Ours w/o constraint		
	WL (μm)	PRA (μm^2)	CPU Time (s)	WL (μm)	PRA (μm^2)	CPU Time (s)
n100	194002	12560	9241	148472	10402	18.08
n200	402762	13487	22135	269157	10437	25.2
n300	610365	15614	32012	350092	12908	29.35
Nor.	1.57	1.23	872.75	1	1	1

D. Powerplanning and IR-drop Analysis

The subsection shows the procedure to analyze IR-drop of an MSV-driven floorplan. In order to estimate IR-drop of modules, we have to perform powerplanning which builds 3D power delivery networks (PDNs) to connect all modules in respective PDs to the associated power sources. A PDN is composed of a power ring and horizontal (vertical) power stripes. Every die in a 3D IC is divided into uniform grids with small size, and all segments in power rings and stripes line on grids. The procedure to build a PDN is as follows: first, we construct a power ring for each VI which uses the small bounding box to enclose the VI. Then, horizontal (vertical) power stripes inside each power ring are built. The spacing between every neighboring power stripes is ρ , where ρ is a user-specified value. To make sure that power stripes in different dies can be connected together by MIVs, power stripes in different dies have to line up. Then, voltage drop value in each PDN is estimated, respectively. If the worse voltage drop value in one PDN is larger than a given constraint, densities of all power meshes are increased by reducing the spacing from ρ to $\frac{\rho}{2}$. The procedure repeats until the IR-drop constraint is satisfied in all PDNs. Fig. 5 shows the procedure of increasing densities of power meshes.

To check the IR-drop constraint, a static IR-drop analyzer was implemented by us. It is based on the matrix equation $GV = I$ [14], where G denotes the conductance matrix for the resistors in a 3D PDN. $V(I)$ denotes the vector of voltages (current loads) for the nodes of the PDN.

IV. EXPERIMENTAL RESULTS

We implemented our algorithm in C++ programming language and ran it on Linux workstation with Intel Xeon E5500 2.27 GHz CPU and 90GB memory. In all experiments, the aspect ratio of a soft module is restricted between 1/3 and 3.

TABLE III
INFORMATION OF IBM BENCHMARKS.

Cir.	# of Tiers	# of TSVs	# Soft Modules	# Hard Modules
ibm01	2	568	665	246
ibm13	2	1494	530	424
ibm18	2	3121	658	285

The voltage values are 0.9 V, 1.0V, and 1.1V (0.9V and 1.0V) if a design has three (two) power domains, and a tolerable voltage drop is 5%. A 3D IC has maximum 15% whitespace in each die.

Our experiment can be divided into two parts. In the first part, we compare our methodology with Falkenstern *et al.* [6] which also handle floorplanning and powerplanning at the same time in 3D ICs. Since they do not handle multiple power domains, we restrict our methodology with single one power domain. Moreover, Falkenstern *et al.* [6] use the SA-based approach to handle hard modules without considering the fixed-outline constraint. For a fair comparison, we add an additional term into their cost function to ensure that modules can be placed inside an outline according to the approach proposed by [2]. The aspect ratio of a chip outline is set as 1:1. The voltage is 1V and 5% IR-drop is tolerable. Table I shows the comparison result. According to the table, our method is significantly faster than the SA-based approach. Besides, our wirelength is much shorter than their approach. Moreover, their approach requires a larger power routing area (PRA) than our result, which means that they require more routing resource in constructing a PDN in order to satisfy the IR-drop constraint. Note that PRA is computed by multiplying the wirelength of a PDN with a wire width.

Next, we show results of our MSV-driven 3D floorplanning methodology based on GSRC and IBM benchmarks, respectively. Table II exhibits the experimental results of GSRC circuits, which include three floorplanning styles for MSV circuits. In the first style, we only optimize wirelength without considering the voltage-island constraint. The second and third styles are based on our methodology except modules in the same PD are restricted to form an exact VI in the third style (i.e., we name it strict voltage island constraint). Columns 2-4, 5-7, 8-10 of the table respectively show the results of the three floorplanning styles, which include wirelength, power routing area (PRA), and runtime. The table shows floorplanning without considering the voltage-island constraint obtains the shortest wirelength, but it requires more routing resource in powerplanning in order to satisfy the IR-drop constraint. On the contrary, the strict voltage-island constraint requires the longest wirelength; however, it has the smallest PRA value. Hence, a flexible voltage island constraint gets compromised results in terms of wirelength and PRA. Fig. 6 (a), (b) and (c) respectively show the resulting 3D floorplans of n300 in the three floorplanning styles, where a 3D IC contains three dies.

In order to demonstrate the scalability of our methodology, we also ran our program on IBM benchmarks which have more modules than GSRC benchmarks. Besides, each benchmark contains soft modules as well as hard modules. The information of IBM benchmarks is shown in Table III. To reveal the impact of the voltage island constraint on wirelength, we also compare the MSV-driven floorplanning with those without the constraint, and the results are shown in Table IV. Fig. 7 (a), (b) and (c), respectively, show the resulting 3D floorplans for ibm01, ibm13, and ibm18 circuits, where each 3D IC contains

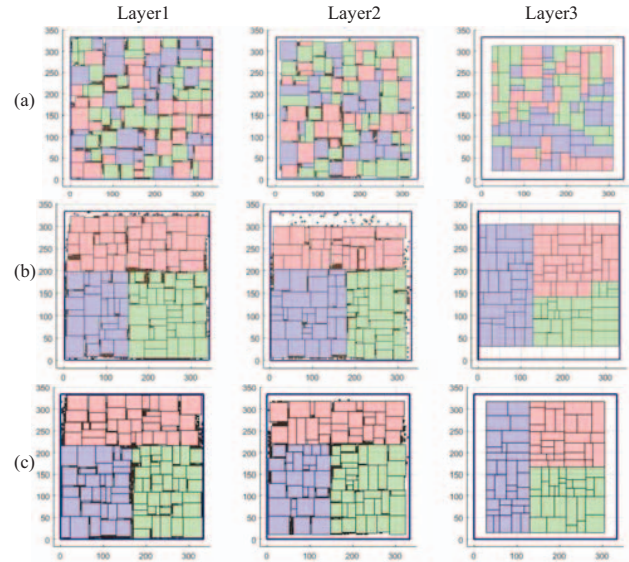


Fig. 6. Resulting floorplans of n300 in a three die 3D IC. (a) w/o voltage-island constraint, (b) ours, and (c) strict voltage-island constraint.

TABLE IV
COMPARISON OF WIRELENGTH AND PRA IN TWO FLOORPLANNING STYLES

Cir.	w/o Voltage-island constraint			Our methodology		
	WL (μm)	PRA (μm^2)	CPU Time (s)	WL (μm)	PRA (μm^2)	CPU Time (s)
ibm01	2755950	140712	35.0	4043670	123669	36.32
ibm13	33480800	8336150	111	42651300	8008950	126.3
ibm18	71331200	9470520	359	91663500	9205370	283.8
Nor.	0.78	1.035	1.13	1	1	1

two dies.

V. CONCLUSION

In this paper, we have presented a methodology to handle MSV-driven floorplanning and powerplanning for 3D ICs. Our approach is able to get the balance between wirelength and power resource usage while satisfying the fixed-outline constraint. The experimental results have demonstrated the effectiveness and efficiency of our methodology.

REFERENCES

- [1] P. Batude *et al.*, "Advances in 3D CMOS sequential integration." *In Proc. IEEE Int. Electron Devices Meeting*, pages 1-4, Dec 2009.
- [2] T.-C. Chen and Y.-W. Chang, "Modern Floorplanning Based on Fast Simulated Annealing." *In Proc. ISPD*, pages 104-112, 2005.
- [3] T.-C. Chen, Z.-W. Jiang, T.-C. Hsu, H.-C. Chen, and Y.-W. Chang, Member. "NTUplace3: An Analytical Placer for Large-Scale Mixed-Size Designs With Preplaced Blocks and Density Constraints." *IEEE TCAD*, Vol. 27, No. 9, pages 1228-1240, July 2008.
- [4] L. Cheng, L. Deng, and D. F. Wong. "Floorplanning for 3-D VLSI Design." *In Proc. ASP-DAC*, pages 405-411, 2005.
- [5] J. Cong, J. Wei, and Y. Zhang. "A Thermal-driven Floorplanning Algorithm for 3D ICs." *In Proc. ICCAD*, pages 306-313, 2004.
- [6] P. Falkenstern, Y. Xie, Y.-W. Chang, Y. Wang, "Three-Dimensional Integrated Circuits (3D IC) Floorplan and Power/Ground Network Co-synthesis." *In Proc. ASP-DAC*, pages 169-174, 2010.
- [7] J. Hu, Y. Shin, N. Dhanwada, and R. Marculescu, "Architecting Voltage Islands in Core-based System-n-a-chip Designs," *In Proc. ISLPED*, pages 180-185, Aug 2004.

TABLE II
COMPARISON OF WIRELENGTH AND PRA IN THREE FLOORPLANNING STYLES.

Cir.	w/o Voltage-island constraint			Our methodology					
	WL (μm)	PRA (μm^2)	CPU Time (s)	Flexible voltage-island constraint			Strict voltage-island constraint		
				WL (μm)	PRA (μm^2)	CPU Time (s)	WL (μm)	PRA (μm^2)	CPU Time (s)
n100	154221	39876	3.53	172466	39750	2.67	201866	31584	2.86
n200	272791	62151	5.79	327482	56721	6.54	367897	56688	6.98
n300	446390	135018	8.73	447608	134082	9.18	487098	132798	9.21
Nor.	0.77	1.03	0.98	1	1	1	1.12	0.96	1.03

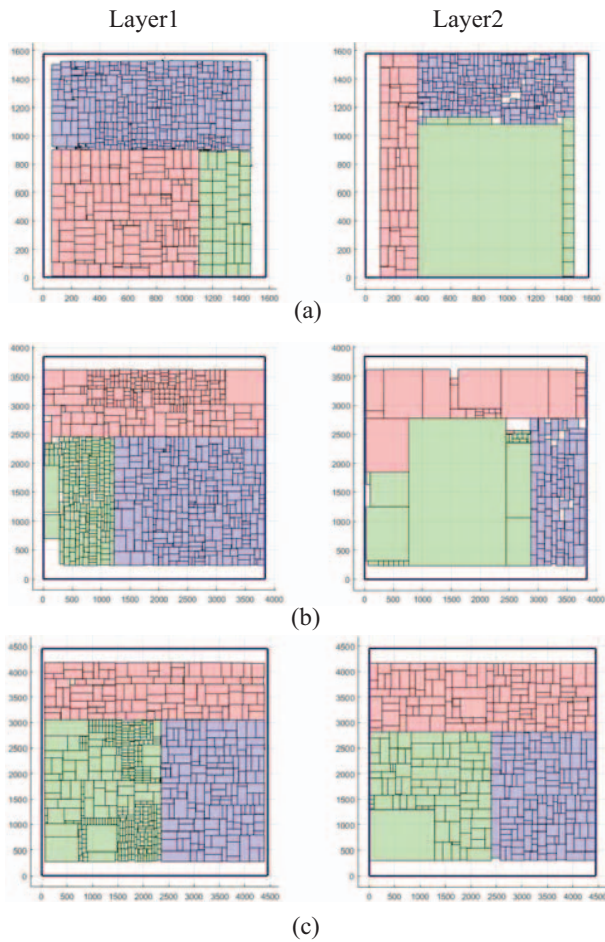


Fig. 7. Resulting floorplans in a two die 3D IC for (a) ibm01, (b) ibm13, and (c) ibm18.

[8] W.-L. Hung et al., "Temperature-aware Voltage Islands Architecting in System-on-chip Design," *In Proc. IEEE ICCD*, pages 689-696, 2005.
 [9] G. Karypis, R. Aggarwal, V. Kumar, and S. Shekhar, "Multilevel hypergraph partitioning: Application in VLSI domain," *In Proc. DAC*, pp. 526-529, 1997.
 [10] J. Knechtel, F. Y. Young, J. Lienig, "Planning Massive Interconnects in 3D Chips," *IEEE TCAD*, Vol. 34, No. 11, pages 1808-1821, Nov 2015
 [11] M. Kuwano and Y. Takashima, "Stable-LSE Based Analytical Placement with Overlap Removable Length," *In Proc. SASIMI*, pages 115-120, 2010.

[12] W.-P. Lee, H.-Y. Liu, and Y.-W. Chang, "Voltage Island Aware Floorplanning For Power and Timing Optimization," *In Proc. ICCAD*, pages 389-394, 2006.
 [13] Z. Li, X. Hong, Q. Zhou, Y. Cai, J. Bian, H. H. Yang, V. Pitchumani, and C.-K. Cheng, "Hierarchical 3-D Floorplanning Algorithm for Wirelength Optimization," *IEEE TCAS-I*, Vol. 53, No. 12, pages 2637-2646, Dec 2006.
 [14] Z. Li, Y. Ma, Q. Zhou, Y. Cai, Y. Wang, T. Huang, and Y. Xie, "Thermal-aware Power Network Design for IR drop Reduction in 3D ICs," *In Proc. ASP-DAC*, pages 47-52, 2012.
 [15] C.-R. Li, W.-K. Mak, and T.-C. Wang, "Fast Fixed-outline 3-D IC Floorplanning with TSV Co-placement," *IEEE TVLSI*, Vol.21, No. 3, pages 523-532, Mar 2013.
 [16] J.-M. Lin and Z.-X. Hung, "SKB-tree: A fixed-outline Driven Representation for Modern Floorplanning Problems," *IEEE TVLSI*, Vol. 20, No. 3, pages 473-484, Mar 2012.
 [17] J.-M. Lin, B.-Y. Chiu and Y.-F. Chang, "SAINT: Handling Module Folding and Alignment in Fixed-outline Floorplans for 3D ICs," *In Proc. ICCAD*, 2016.
 [18] Remove for blind review, to be appeared in *IEEE TCAD*.
 [19] Y. Ma, X. Hong, S. Dong, and C.-K. Cheng, "3D CBL: An Efficient Algorithm for General 3-Dimensional Packing Problems," *In Proc. MWSCAS*, pages 1079-1082, 2005.
 [20] Q. Ma and E. F. Y. Young, "Multivoltage floorplan design," *IEEE TCAD*, Vol. 29, No. 4, pages 607-617, Apr 2010.
 [21] W. Naylor, R. Donnelly, and L. Sha, "Non-linear Optimization System and Method for Wire Length and Delay Optimization for and Automatic Electric Circuit Placer," US Patent 6 301 693, 2001.
 [22] S. Panth, K. Samadi, Y. Du, and S. K. Lim, "High-density Integration of Functional Modules using Monolithic 3D-IC Technology," *In Proc. ASP-DAC*, pages 681-686, Jan 2013.
 [23] S. Panth, K. SamadP, Y. Du, and S. K. Lim, "Tier-Partitioning for Power Delivery vs Cooling Tradeoff in 3D VLSI for Mobile Applications," *In Proc. DAC*, pages 8-12, June 2015.
 [24] Z. Qian and E. F. Y. Young, "Multi-voltage floorplan design with optimal voltage assignment," *In Proc. ISPD*, pages 13-18, 2009.
 [25] T Song, S Panth, Y.-J. Chae, and S. K. Lim, "Three-Tier 3D ICs for More Power Reduction: Strategies in CAD, Design, and Bonding Selection," *In Proc. ICCAD*, pages 752-757, 2015.
 [26] M.-C. Tsai, T.-C. Wang, and T. Hwang, "Through-Silicon Via Planning in 3-D Floorplanning," *IEEE TVLSI*, Vol. 19, No. 8, pages 1448-1457, Aug 2011.
 [27] K. Wang, S.Dong, and F. Jiao, "TSF3D: MSV-Driven Power Optimization for Application-Specific 3D Network-on-Chip," *IEEE TCAD*, Vol. 36, No. 7, pages 1089-1102, July 2017.
 [28] J. Yan and C. Chu, "DeFer: Deferred Decision Making Enabled Fixed-outline Floorplanning Algorithm," *IEEE TCAD*, Vol. 29, No. 3, pages 367-381, Mar 2010.
 [29] P.-H. Yuh, C.-L. Yang, Y.-W. Chang, and H.-L. Chen, "Temporal Floorplanning Using 3D-subTCG," *In Proc. ASP-DAC*, pages 725-730, Jan 2004.
 [30] P.-H. Yuh, C.-L. Yang, and Y. Chang, "Temporal floorplanning using the T-tree formulation," *In Proc. ICCAD*, pages 300-305, 2004.
 [31] P. Zhou, Y. Ma, Z. Li, R. P. Dick, L. Shang, H. Zhou, X. Hong, and Q. Zhou, "3D-STAF: Scalable Temperature and Leakage Aware Floorplanning for Three-Dimensional Integrated Circuits," *In Proc. ICCAD*, pages 590-597, 2007.