Fast Chip-Package-PCB Coanalysis Methodology for Power Integrity of Multi-Domain High-Speed Memory: A Case Study

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***Abstract*— The power integrity of high-speed interfaces is an increasingly important issue in mobile memory systems. However, because of complicated design variations such as adjacent VDD domain coupling, conventional case-specific modeling is limited in analyzing trends in results from parametric variations. Moreover, conventional industrial methods can be simulated only after the design layout is completed and it requires a lot of back-annotation processes, which result in delayed delays time to market. In this paper, we propose a chip-package-PCB coanalysis methodology applied to our multi-domain high-speed memory system model with a current generation method. Our proposed parametric simulation model can analyze the tendency of power integrity results from variable sweeps and Monte Carlo simulations, and it shows a significantly reduced runtime compared to the conventional EDA methodology under JEDEC LPPDR4 environment.**

I. Introduction

The packaging structure causes static and dynamic power loss. Therefore, from a low-power perspective, it is necessary to consider the power integrity (PI) without securing the on-die termination (ODT) and equalizer while reducing power loss. Moreover, because of the IR drop in the power distribution network (PDN), it is also necessary to analyze the effect of additional decoupling capacitors on the dynamic losses to ensure power integrity [1]. Recently, multiple power domains are applied in low-power memory systems to deliver power with an adequate VDD level, and each power domain has its own noise and switching activity [2]. However, the previous multi-domain research has focused only on analysis in the package, and there has not been sufficient system-level analysis, or has focused on case-specific analysis parametric analysis [3]–[5].

In industry, due to the difficulties of this power integrity analysis, chip-package-PCB are designed through many back-annotations rather than efficient co-design. An conventional method obtains results from simulations using a EDA tool with the realistic package-PCB design. Therefore, if it is possible to estimate how design and environment parameters affect the PI through a analysis method, this can effectively reduce the back-annotation process.

In accordance with this recent design trend, we propose a design methodology for PI that considers the effects of electrical and structural parameters on the multi-voltage domain PCB-package-chip system. For the PI analysis, we construct a parametric link model that can quickly and accurately predict electrical performance characteristics according to various design variables of a high-speed link. In addition, it is necessary to develop a statistical analysis of the performance data derived from the link model that provides design guidelines. Thus, we also propose a link simulation environment considering the electrical characteristics of the high-speed memory current profile and physical effects of PCB and packaging in multiple domains. In this paper, we introduce a fast chip-package-PCB coanalysis methodology for multi-domain power integrity as shown in Figure 1. We define the parameters that include characteristics of power delivery system, then our script parses parameters to base simulation files with S-parameter of PDN. Finally results of test case and analyzed data are obtained.

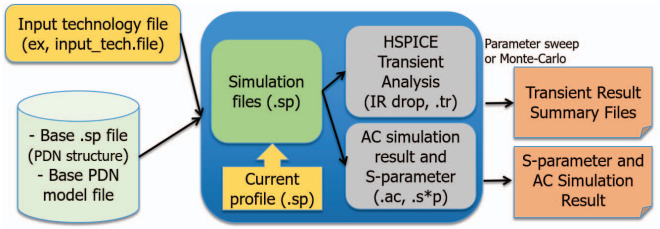

Fig. 1. Process of package-channel analysis with power integrity script.

The main contributions of our work are summarized as follows.

- We analyze power integrity with sweep or Monte Carlo simulation of design parameters under a multi-domain JEDEC 800MHz LPDDR4 memory environment.
- Our package-channel analysis tool can make PI simulations according to various design parameters of chip-package-PCB and supply power noise with a short runtime.
- Our proposed pseudo-random current profile characterize the realistic on-chip current profiles with desired design constraints.

The remainder of this paper is organized as follows. Section II describes our package-channel analysis model which consists of the chip-package-PCB, supply power source, and current profile generation method. Section III presents procedure of proposed methodology, and section IV the experimental simulation result and analysis. Section V summarizes and concludes the paper.

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II. Power Delivery System Analysis Model

To make power analysis of the low-power package design, we implement a package-on-package (PoP) model of the power delivery system (PDS) using *Synopsys HSPICE* [6]. Figure 2 shows an overview of the PDS analysis model. The power is transfered from VRM to memory chip through PCB board, SoC package and memory package. The PCB and packages have decoupling capacitors. In addition, memory package and chip are wire bonded. Instead of modeling the realistic signal channel, we generate a pseudo-random current profile with real channel characteristics.

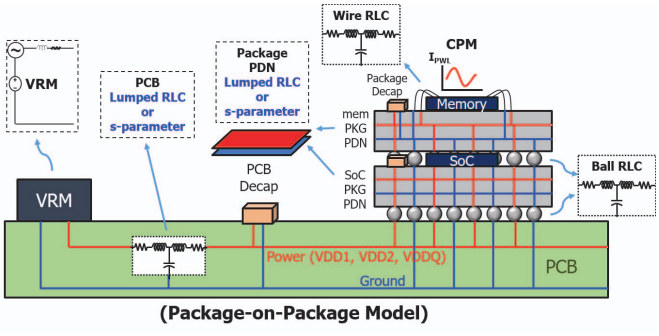

Fig. 2. Overview of the power delivery system for package-on-package (PoP) model.

A. Multi-Domain Power Distribution Network

Analysis of power domain coupling is needed to prevent unwanted distortion of PI. In order to prevent coupling between power domains, a ground plane is placed between them in general. We use a PDN structure with two power domains as shown in Figure 3. This PDN structure has two power domains and ground planes. Two power domains are surrounded by a ring ground, and separately placed by center ground plane. Each ground planes are connected to the bottom ground plane by vias. A detailed design parameters are described in a preliminary analysis [7]. This PDN structure is electrically small and simple compared with the realistic PDN geometry, and the location of port in same power plane are not dominant. Therefore, we have chosen the input/output ports of two domains as shown in Figure 3. We mainly consider three design parameters to analyze the domain coupling effect. First, we change the existence of the center (CGND) and the ring (RGND) grounds. Second, we vary the width of edges around of the power domain planes (MARGIN_WIDTH), and the other dimensions are fixed.

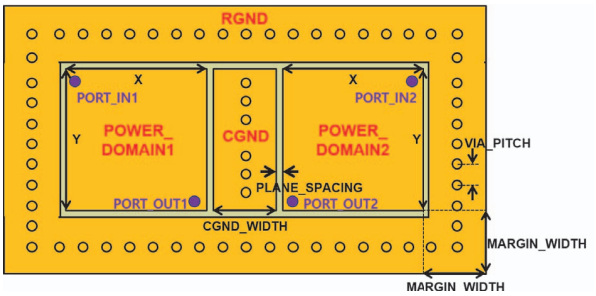

Fig. 3. Structure and parameters of a simple multi-domain PDN.

B. Input Power Source

The voltage regulator module (VRM) consists of a DC-DC converter and a feedback control circuit, which supplies the reference voltage required by the system to the output stage. The VRM is basically a nonlinear system. However, when the nonlinear model is implemented as it is in the power transfer model, the simulation runtime becomes longer, and it is difficult to set the parameters that determine the characteristics of each element in the VRM. Therefore, when the power transfer model is constructed to analyze the power integrity, the VRM is simplified to a linear model. The buck switching regulator is a widely used nonlinear VRM model [8], and we simplified it to a linear model for simulations in *HSPICE*. For the VRM, four-element linear model can be used as shown in Figure 4(a).

However, L_{slew} and R_{flat} do not significantly affect the output response in the low switching noise frequency range below 10 MHz [9]. Thus, we have modeled VRM based on the two-element linear model as shown in Figure 4(b).

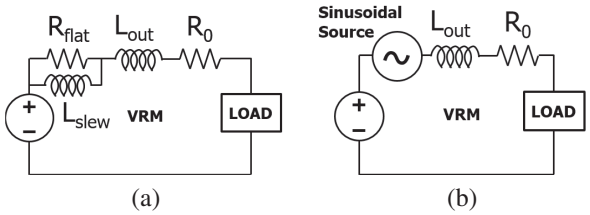

Fig. 4. (a) Four-element linear VRM model and (b) proposed two-element linear input power source model with a sinusoidal source as a noise.

Based on the two-element linear model, we have added the sinusoidal noise source and the VDD offset. L_{out} is the inductance value of the cable between the VRM and the system board, and it affects the maximum effective frequency. R_0 represents the resistance between the VRM sense point and the actual load. R_0 of VRM can be calculated as follows $R_0 = \rho \frac{l}{A}$, where ρ is the resistivity (assuming copper in this model), A is the cross-sectional area of the die, and l is the maximum path length.

We have modeled the input noise itself as a sinusoidal source to make it easier to use in EDA analysis. The noise ripple and frequency of the VRM can be set in the sinusoidal source, and the DC voltage level is determined by setting the VDD offset. In this way, the input of the PDS can be adjusted as an environment similar to the VDD source output from the actual VRM.

C. On-Chip Current Profile Generation

In general, when modeling a PDS and analyzing power loss and PI, the chip power model (CPM) [10] is used instead of the realistic channel model to reduce design complexity and simulation time. In the CPM, it is easy to change the model of the package at once, but it is unsuitable for swapping the components of the package. In addition, the CPM already contains on-chip capacitance, metal resistance, and an RDL. Thus, it has less flexibility in design simulation from the perspective of the package designer. Therefore, in our methodology, we propose a pseudo-random current profile generation algorithm.

The on-chip current profile is designed to be pseudo-randomized with several characterized parameters as shown in

Figure 5(b). We set the parameters to have an important effect on the power transfer characteristics during actual operation to achieve a current demand similar to a real memory operating environment. As the input parameters, we take the min/max current constraint, and the min/max *slope_step* value. In addition, we generate a randomized piecewise linear waveform to satisfy the input condition. The *slope_step* determines the time between current slope (di/dt) changes as one step. A random current value between the min/max *current constraint* is arbitrarily set for each *slope_step*, and then the waveform is generated by increasing/decreasing based on the random current value. The *delay* parameter is the initial delay time at which the current profile starts. The *interval* time that the current profile repeats is also an input parameter, and the *time_length* is a repeated period for the generated current profile. Note that the above parameters are not intended to imitate realistic waveforms, but are intended to facilitate analysis through parametric simulation by characterizing factors that affect the PI.

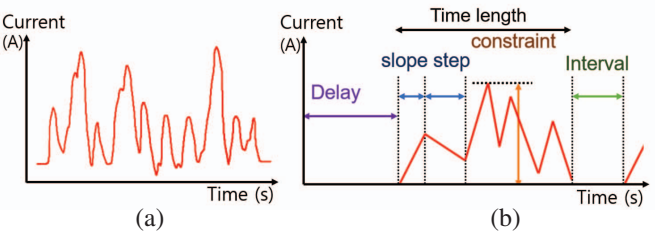

Fig. 5. (a) Realistic on-chip current profile. (b) Overview of characterized pseudo-random current profile parameters.

III. Procedure of Proposed Methodology

This section describes the procedure of package-channel analysis with our proposed power integrity script in detail. As shown in Figure 6, we first read the PDN and simulation parameters, and internally computes the RLC values through the calculation process. The PDN model is simulated with the S-parameter. If we input the lumped RLC value of the PDN directly, the generated lumped RLC PDN model and the remaining parameters are parsed. In addition, an on-chip current profile is generated based on the input parameters. All the results of simulations are automatically summarized in the output file.

For the analysis of PI in transient simulation, there are two methods to change design and process parameters – sweep simulation and Monte Carlo simulation. In a sweep simulation, we can observe how each parameter affects the PI characteristics. The variation in the IR-drop of the on-chip can be observed by sweeping one parameter. This allows us to analyze the relative impact of different parameters and the trends of linear and nonlinear effects. On the other hand, Monte Carlo simulation is mainly carried out to investigate how the errors in the process affect the entire PDS. For example, when the geometric dimension of the memory package PDN varies, the Monte Carlo simulation can be used for PI analysis. In addition, it is not easy to analyze whether process/voltage/temperature (PVT) variation occurs at the same time, our proposed methodology can quickly statistically analyze through the Monte Carlo simulation.

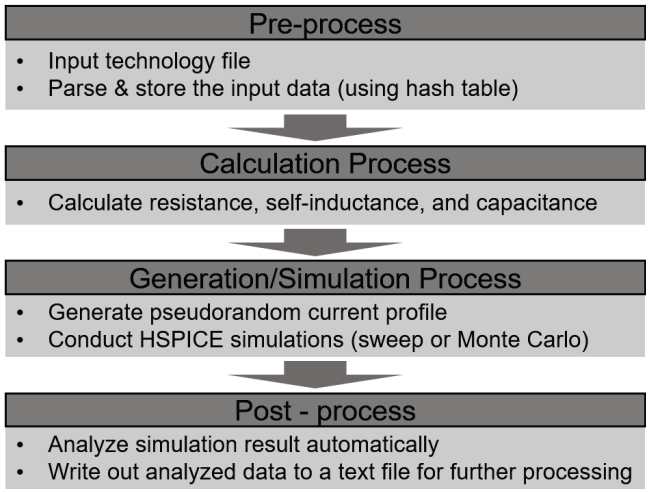

Fig. 6. Procedure of proposed fast analysis methodology for PI.

IV. Simulation and Analysis

Our proposed fast methodology script is written in *Perl* and *HSPICE*, and validated on a 2.4GHz Intel Xeon E5-2620V3 Linux workstation with single core for HSPICE simulation. We perform several case-based sweep and Monte Carlo simulation for PI analysis. Figure 7 shows the simplified schematic of VDDQ and VDD2 of the PoP PDS model. Our multi-domain PDN model is adopted to SoC and memory package, and we use PCB board PDN as lumped RLC element with actual parameter values. All the simulations are measured at the pad of on-chip to analyze power transfer from VRM to memory chip as shown in Figure 7. Note that we set the parameters based on real 800MHz LPDDR4 memory.

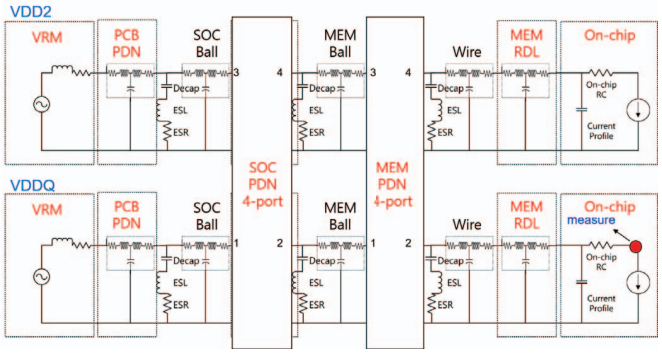

Fig. 7. Schematic of PoP PDS model and measurement point for analyzing of on-chip PI.

A. Domain Coupling

To investigate the domain coupling effect of the ring and center ground plane, we simulate two methods. First, we analyze effect of existence of center and ring ground. We change the PDN of package by three cases: RGND=1 and CGND=1, RGND=1 and CGND=0, RGND=0 and CGND=1. Figure 8(a) is a generated current profile, and as shown in Figure 8(b), center and ring ground can reduce the domain coupling effect by reducing mutual capacitance between two

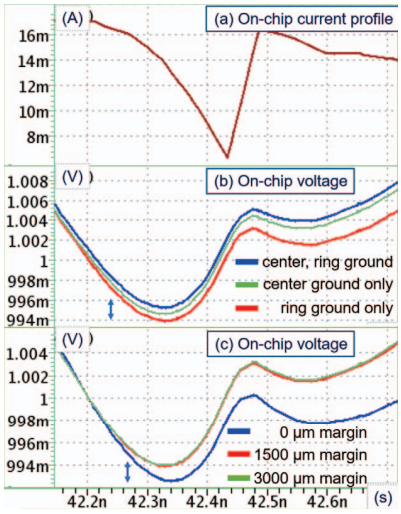

Fig. 8. Transient result of (a) generated current profile and corresponding voltage fluctuations in two method (b) voltage with three different PDN structure (with both of center/ring, without ring, without center ground) and (c) three different ground margins (0, 1500, 3000 μm) of package PDN on pad of on-chip VDDQ.

domains. In this case, the center ground plane improve PI more effectively than ring ground plane. Second, we vary the width of ground plane margin from 0 μm to 3,000 μm with the other fixed parameters: CGND=1, RGND=0. As shown in Figure 8(c), we observe that larger margin width can reduce IR drop. Note that our multi-domain PDN model is relatively small than actual package PDN structure, thus, the effect of domain coupling is also less than the actual environment.

B. Input Noise Effect

To analyze the effect of input VDDQ noise frequency, we have made a simulation with out proposed methodology. Although the magnitude of the input noise is the same, the PI depends on the frequency. As shown in Figure 9, the input noise affects according to the frequency on VDDQ of the on-chip pad. In addition, we could analyze the tendency of relationship between IR drop and input VDDQ noise frequency as shown in Figure 10(a). Moreover, we have analyzed how critical noise frequency range (red circle in Figure 10(a)) affects PI. We perform 1,000 Monte Carlo simulations with 10% 1-sigma variation as shown in Figure 10. The runtime of the simulation is about 120 minutes, which is significantly faster compared to the conventional simulation method which takes approximately 1,000 times longer.

V. Conclusion

In this paper, we propose a PDS analysis methodology in high-speed low power memory environment. First, we suggest a simple multi-domain PDN model to analyze domain coupling effects. We integrate VRM, PDN (PCB, SoC and memory package), decap, wire and ball model. In addition, on-chip current profiles are configured to improve simulation flexibility and runtime. Our proposed parametric simulation methodology can analyze the tendency of results from variable sweeps and Monte Carlo simulations. Moreover, the runtime of entire process is significantly faster than conventional simulation method. Thus, our proposed methodology makes it possible to design considering PI by applying parametric simulation and optimization technique. Our ongoing work seeks to analyze the power integrity with on-chip dynamic operation modes and to compare with a commercial EDA tool.

Note that one simulation takes about two hours by *HSPICE* tool with actual layout in the referenced environment.

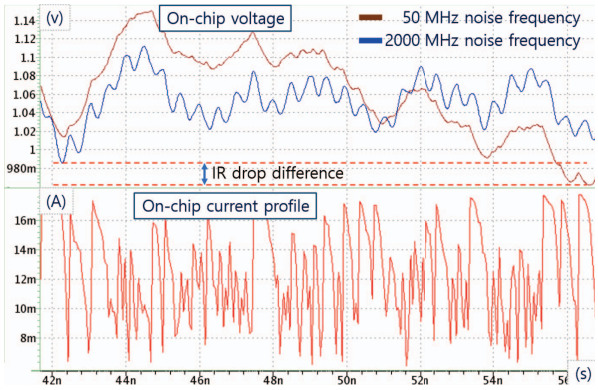

Fig. 9. Transient result of voltage (above) and current profile (below) on pad of on-chip VDDQ.

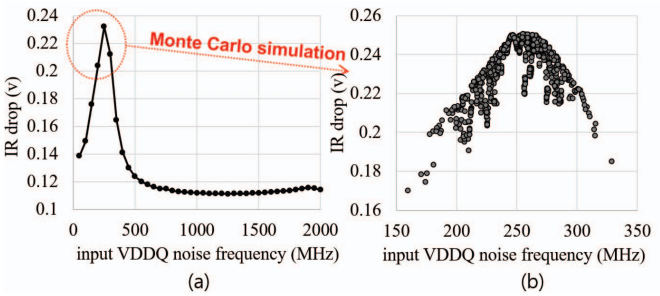

Fig. 10. IR drop on pad of on-chip with various input noise frequency.

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