Pre-Assembly Testing of Interconnects in Embedded Multi-Die Interconnect Bridge (EMIB) Dies

Sudipta Mondal and Krishnendu Chakrabarty
Department of Electrical and Computer Engineering
Duke University, Durham, NC 27708, USA

***Abstract*—The embedded multi-die interconnect bridge (EMIB) is an advanced packaging technology for 2.5D integration. This paper presents a bridge test architecture based on the proposed IEEE Std. P1838. The proposed test method enables access to interconnects at a pre-assembly stage by pairing the interconnects using metal shorts and probing on coarse-pitch C4 bumps. It can efficiently detect resistive-open and resistive-short defects in the bridge interconnects and micro-bumps. Simulation results are presented to evaluate the range of defects that can be detected by the proposed method.**

I. Introduction

Three-dimensional (3D) ICs use through-silicon-vias (TSVs) to stack multiple dies [1]. Even though 3D integration overcomes the problems of large footprint and long global interconnects, challenges related to cost, yield, and testing are yet to be adequately addressed. These problems have paved the way for the adoption of interposer-based 2.5-D ICs [2].

However, interposers also introduce design and test challenges. An interposer must be large in size to accommodate the dies on it. In addition, the large number of TSVs in 2.5D ICs may result in reduced yield, degraded signal integrity, and IR drop in power-delivery nets [3].

Embedded multi-die interconnect bridge ICs (EMIB ICs) offer several advantages over interposers, e.g., higher bandwidth, flexibility of die placement, and increased scalability [3]. In this technology, the interposer is replaced by a thin silicon chip (also called a bridge), with multiple routing layers that eliminate the need for TSVs [4]. Intel recently announced the 8th-generation Core H-Series chip with integrated AMD Radeon graphics [5]. This H-Series CPU uses EMIB technology to interconnect the various Intel and AMD components, as well as high-bandwidth on-chip memory. Resistive opens and shorts can, however, occur in the bridge interconnect due to incomplete metal fill, misalignment of micro-bumps, and deformation. These defects lead to excessive interconnect delay and anomalous electrical characteristics. In [4], a test vehicle was proposed to evaluate the signal integrity of EMIB interconnects. RF probing was performed to measure the S-parameters of the interconnects. However, direct RF probing of micro-bumps is expensive using standard test equipment in high-volume manufacturing. Moreover, the test-application time for RF probing can be prohibitively high and it is difficult to evaluate test quality for shorts and opens.

We propose a new test method for detecting opens and shorts in EMIB interconnects. We perform testing after a logic die is attached to the bridge. This die is utilized for both applying test patterns and observing test responses. In this way, direct probing is not required and test cost is reduced.

In an EMIB chip reported in the literature [6], one side of the EMIB die is connected to a transceiver die and other side is connected to an FPGA. If testing is performed with both sides of bridge attached to functional dies, then in case of a faulty bridge, we will need to discard both the dies. As the processing cost of an FPGA is higher than that of a transceiver die [6], it is more economical to perform the test with the transceiver die and attach the FPGA later. On the other hand, direct probing of the bridge die with no functional die is difficult due to the localized high density of interconnects. Thus, this paper is aimed at testing of the EMIB with one functional die attached to it. This testing step can ensure the screening of defective EMIB dies, whereby good functional dies do not have to be discarded after assembly due to a defective EMIB. While pre-assembly EMIB testing without any functional die and post-assembly testing where functional dies are connected to both sides of the EMIB are also desirable, we leave this problem for future work.

The IEEE 1149.1 test-access port (TAP) has been used to test interposer interconnects [7], [8]. In these methods, two dies are used to launch tests and capture responses, respectively. We have to, however, implement a new test architecture in which the same functional die is used to apply test patterns and capture test responses. The key difference between interposers and EMIBs is that interposers use vertical and horizontal interconnects for inter-die communication [8]. The vertical interconnects are connected to C4 bumps by TSVs. Hence, these interconnects can be utilized to apply test patterns and observe test responses. EMIB-based 2.5D ICs do not have TSVs that can be leveraged for testing and this imposes a new challenge in EMIB interconnect testing. The IEEE 1149.1 boundary scan architecture is not suitable for this purpose as it provides only one test data input pin (TDI) and one test data output pin (TDO). Hence, the TDO pin of another functional die must be used to shift out the test responses from interconnect test. On the other hand, the proposed IEEE Std. P1838 [9] facilitates TAPs, (primary and secondary) on a functional die, which can be concatenated to form a single test path. Thus, we present a test technique that is compatible with P1838.

Since EMIB-based 2.5D IC prototypes have been reported in industry [4], [6], [3], it is likely that test methods have also been developed for these prototypes. However, these methods are proprietary and not fully disclosed in the literature. This

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paper describes a test solution based on open standards that can be leveraged and extended, and can facilitate collaborative advances for the next generation of EMIB-based 2.5D ICs.

The rest of the paper is organized as follows. Section II presents an overview of EMIB technology. The proposed test method and test architecture are presented in Section III. Section IV presents simulation results. Finally, Section VI concludes the paper.

II. Overview of EMIB technology

The bridge substrate is composed of glass, ceramic, or semiconductor material. Electrical routing features (through-hole-vias, traces, and pads) through the substrate are first created. A sacrificial layer is added on the surface of the substrate. Openings are formed in the sacrificial layer to facilitate the connections between interconnects and micro-bumps. After the formation of interconnect pads and traces, the sacrificial layer is etched away [10]. The organic package substrate is formed with a cavity to attach the bridge fabricated in the previous step. After the bridge is attached to the package cavity, the final dielectric layers are formed, and coarse-pitch and fine-pitch vias are etched for power-delivery nets and inter-die interconnects, respectively. The bridge is then embedded into the cavity using an adhesive [4].

There are two types of micro-bumps in an EMIB: 1) fine-pitch micro-bumps; 2) coarse-pitch micro-bumps. Fine-pitch micro-bumps are used to connect dies to the interconnects. They enable localized interconnects and high density. Coarse-pitch micro-bumps provide power and ground connections to functional dies. One end of a coarse-pitch micro-bump is connected to a functional die, and the other end is connected to the back of the package substrate through a C4 bump. Interconnects are formed between coarse-pitch micro-bumps and the C4 bumps to provide power and ground connections [10].

III. Proposed Test Architecture

The proposed test-architecture design adds controllability and observability to the bridge interconnects through the package C4 bumps. A new die-wrapper cell is added to the inputs and outputs of the functional die. This design is based on minimal changes to P1838.

A. Overview of P1838

P1838 envisions a primary and a secondary test interface inserted on the bottom side of each functional die. These interfaces are placed in such a way that the secondary interface of a die is connected to the primary interface of another die as shown in Fig. 1(a).

In the pre-assembly stage, there is only one functional die on the EMIB. Hence, one primary and one secondary interface are necessary for testing. The primary interface can be placed on the bottom side of the die where the coarse-pitch micro-bumps are located. The secondary interface can be placed at the location of the fine-pitch micro-bumps, as shown in Fig. 1(b).

Both the primary and secondary interfaces are equipped with test access ports (TAPs); these are referred to as primary and secondary TAPs, respectively (Fig. 2). Each TAP has four

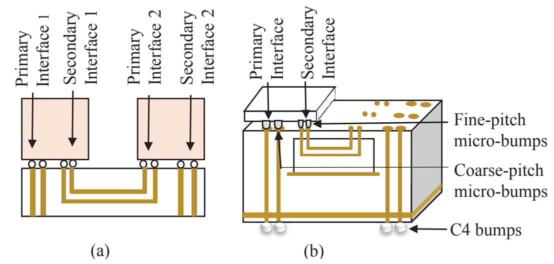

Fig. 1: P1838-compliant test interfaces for: (a) Interposer-based IC; (b) EMIB die.

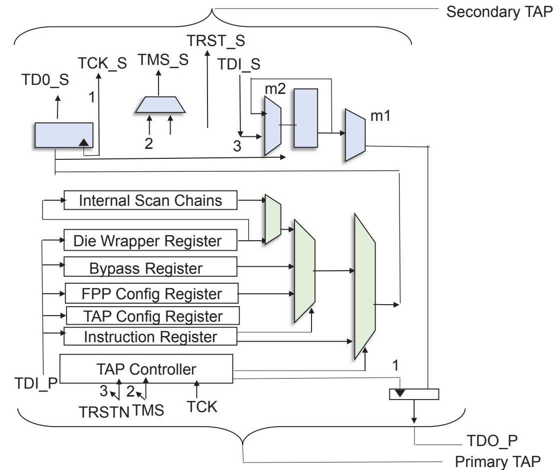

Fig. 2: Primary and secondary TAPs.

input ports and one output port. The ports at the primary interface are labeled as TDI_P (Test Data Input), TCK_P (Test Clock), TMS_P (Test Mode Select), TRSTN_P (Test Reset Not), and TDO_P (Test Data Output). The ports at the secondary interface are denoted as TDI_S (Test Data Input), TCK_S (Test Clock), TMS_S (Test Mode Select), TRSTN_S (Test Reset Not) and TDO_S (Test Data Output). The 16-state finite-state machine of 1149.1 is utilized in the primary TAP controller. It includes:

1) Instruction Register: This register selects the test mode for the die. It also selects the test data register (TDR) that is connected to the serial path of the scan chain.
2) Configuration Register: It selects the secondary interface to be included in the serial scan path of the die. Multiple secondary interfaces can be activated simultaneously.
3) Bypass Register: It is used to bypass the serial scan path.
4) Die Wrapper Register (DWR): This register is used during EXTEST (testing of interconnect between dies) and INTEST (testing of die-internal logic) modes.

B. Details of the Proposed Test Method

In order to overcome the difficulty of direct probing of micro-bumps, dummy metal interconnects were placed in [11] to create test loops between pairs of micro-bumps. We similarly propose the use of dummy metal to create interconnect pairs. After the bridge substrate is embedded in the package substrate, a logic die is connected to one side of the EMIB and dummy metal wires are placed on the interconnect traces that are located on the other side of the EMIB. The dummy

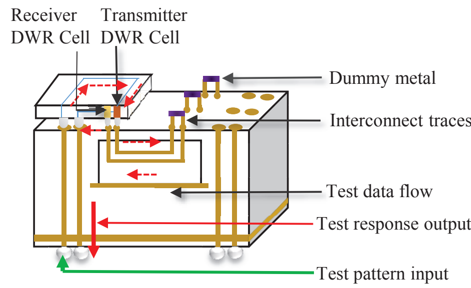

Fig. 3: Test architecture for bridge interconnects.

metal can be subsequently removed using specific processing steps as in [12].

Suppose there are N interconnects in the bridge denoted by 1, 2,...., N. First, we assume that N is even. We divide the interconnects into two groups. The first group includes interconnects 1 to $N/2$ and the second group includes $N/2+1$ and the interconnects up to N. The group of interconnects that are closer to the coarse-pitch micro-bumps are called *receiver interconnects*, and the interconnects that are on the other side of the bridge are called *transmitter interconnects*; see Fig. 3. The micro-bumps attached to the transmitter and receiver interconnects are called the transmitter and receiver micro-bumps, respectively.

Next, we short (using dummy metal) one transmitter and one receiver interconnect to make a pair. The pairing of the interconnects is done in the following manner. Interconnect 1 is paired with interconnect $N/2+1$, interconnect 2 with interconnect $N/2+2$, and so on. The last pair is made by shorting interconnect $N/2$ with interconnect N. On the other hand, if N is odd, the first group includes interconnects 1 to $(N\text{-}1)/2$ and the second group includes $(N+1)/2+1$ and the interconnects up to N. In this case, the first pair consists of interconnect 1 and interconnect $(N+1)/2+1$, the second interconnect pair consists of interconnect 1 and interconnect $(N+1)/2+2$, and so on. The last pair is made by shorting interconnect $(N\text{-}1)/2$ with interconnect N. If N is odd, interconnect $(N+1)/2$ cannot be included in any pair. After testing all of the remaining interconnects, one of the dummy metal shorts can be removed and interconnect $(N+1)/2$ can be paired with the disconnected interconnect of the second group.

A dedicated DWR cell is shown in Fig. 4. DWR cells are attached to transmitter and receiver micro-bumps; these are referred to as transmitter and receiver DWR cells, respectively. In the proposed method, we do not consider connecting a transmitter and receiver DWR cell at every interconnect because this solution is associated with increased area overheard. The transmitter DWR cells are used to shift in and apply test patterns. The receiver DWR cells capture and shift out test responses. The transmitter and receiver DWR cells (Fig. 5-6) are different due to their difference in functionality. Several modifications are made to the P1838-complaint DWR cells in order to implement the transmitter and receiver DWR cells. A multiplexer is added to the transmitter DWR cell. The TEST_ENABLE_S1 signal determines whether the transmitter DWR cell operates in functional mode or test mode, and the

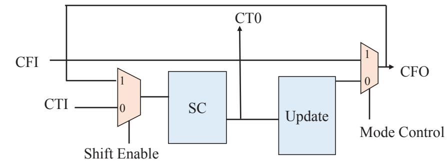

Fig. 4: A dedicated DWR cell [9].

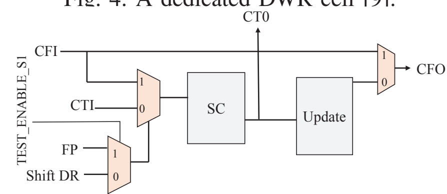

Fig. 5: Design of the proposed transmitter DWR cell.

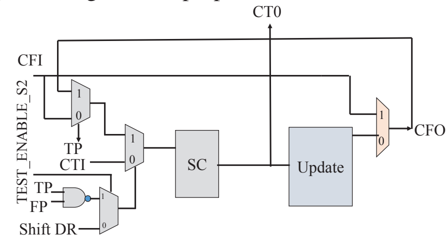

Fig. 6: Design of the proposed receiver DWR cell.

FP signal is used to shift in the test patterns. In the receiver DWR cell, we add two multiplexers and a NAND gate. One of the multiplexers is added to the feedback path from CFO to CTI. This feedback path is important in the proposed test method to ensure that receiver cells can receive test data from transmitter cells. As the boundary scan cells used in IEEE 1149.1 do not have a feedback connection from the parallel output pin (CFO) to the serial input pin (CTI), they are not suitable for the proposed method.

We insert one primary test interface and two secondary test interfaces on the bottom-side of a die. The primary interface is connected to the bottom side of the die that has the coarse-pitch micro-bumps. The test data pins of the primary interface are connected to two coarse-pitch micro-bumps.

The secondary interfaces are inserted on the side of the die that has the transmitter and receiver fine-pitch micro-bumps. The transmitter and receiver test interfaces are denoted as Secondary Interfaces SI_1 and SI_2, respectively. The test data input and output pins of the secondary interface at the transmitter side are TD1_S1 and TDO_S1, respectively. The test data input and output pins of the secondary interface at the receiver side are TD1_S2 and TDO_S2, respectively. Instructions, configuration data and test data are fed to the primary TAP controller through TDI_P. When the test mode is initiated, the value in the configuration register selects the secondary test interface (transmitter or receiver) to be included in the serial scan path of the die. The TCK_P pin is connected to TCK_S1 and TCK_S2. Similarly, TRSTN_P is connected to TRSTN_S1 and TRSTN_S2. The data at the primary interface TMS_P is fed in to TMS_S1 and TMS_S2 through multiplexers. For instance, if TAP_S1 is selected by the configuration register in the TDI_P and TDO_P path, then TMS_S1 will receive the values in TMS_P. When it is deselected, TMS_S1 receives a user-programmable value.

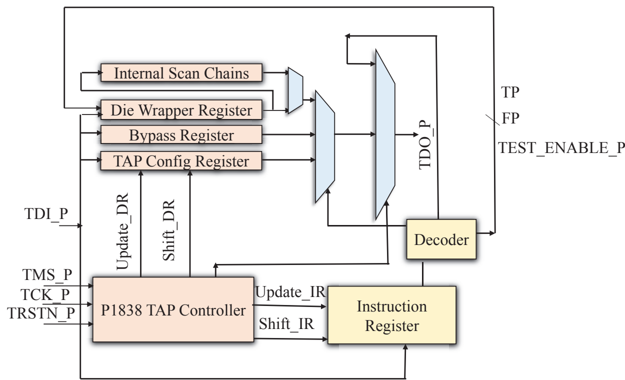

Fig. 7: Design of the primary TAP controller.

Similarly, TEST_ENABLE_P is fed into TEST_ENABLE_S1 and TEST_ENABLE_S2 to select between the functional mode and the test mode at the secondary TAPs.

In order to implement the proposed test method two private instructions (SHIFTIN and SHIFTOUT) need to be inserted, in addition to the public instructions in IEEE P1838 (BYPASS, IDCODE, and EXTEST). In SHIFTIN, the configuration register value is set to 1, and the secondary interface at the transmitter side is included in the serial scan path of the die. The die-wrapper register in connected between TDI_S1 and TDO_S1, and test patterns are shifted into the transmitter DWR cells. The test patterns are applied to the interconnects and captured by the receiver DWR cells. When SHIFTOUT is asserted, the configuration register value is set to 0, and the secondary interface at the receiver side is included in the TDI-TDO path of the die. The die-wrapper register is connected between TDI_S1 and TDO_S1, and test responses captured in the receiver DWR cells are shifted out through TDO_P.

The primary TAP controller remains in the Run-Test/Idle controller state for the duration required for the completion of the execution of SHIFTIN. The scan chain between TDI_S and TDO_S is utilized to shift in a test pattern into the DWR cells. Similarly, when the SHIFTOUT mode is selected, the captured test response in the scan chain between TDI_S and TDO_S is shifted out through TDO_P.

The block diagram of the primary TAP controller is shown in Fig. 7. It has four inputs TCK_P, TMS_P, TRST_P and TDI_P. The signal TEST_ENABLE_P is internally generated from the decoder, and set to 1 when the opcode output of the instruction register matches SHIFTIN or SHIFTOUT. Otherwise, it is set to 0.

Several outputs are generated by the primary TAP controller. The Shift_IR and Update_IR signals are fed into the instruction register during the IR cycle. The Shift_DR and Update_DR signals are generated during the DR cycle and fed to the DWR register and the bypass register. The modified TAP controller generates the additional outputs TP, FP, and TEST_ENABLE_P to implement the proposed test method. These signals are used to select between the functional and the test mode of the TAP. The values of these output signals during different modes of operation are listed in Table I.

Table I: Control signal values in the newly defined test modes.

Instruction	SHIFTIN	SHIFTOUT
TP	1	0
FP	0	1
TEST_ENABLE_P	1	1

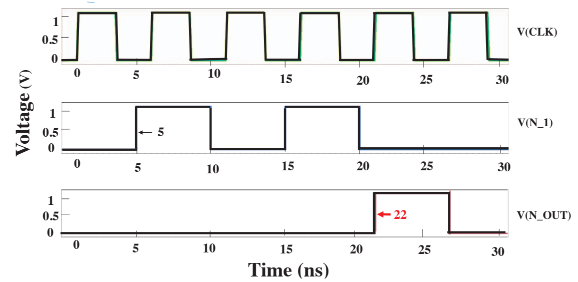

Fig. 8: Results obtained by simulating a resistive-open defect.

IV. Simulation Results

In this section, we present HSPICE and ModelSim simulation results, and, DfT hardware overhead. In a representative EMIB IC, the interconnects are 0.8 μm in diameter, with a pitch of 0.8 μm and thickness of 0.6 μm [13]. Based on this data, we calculated the resistance and capacitance of the bridge interconnect to be 3.5 Ω per 100 μm and 7.73 fF per 100 μm, respectively. The transistors were modeled using a low-power 45 nm technology [14]. Transmission-gate transistor widths were set to 360 nm (270 nm) for PMOS (NMOS). Inverters were composed of 270 nm (180 nm) wide NMOS (PMOS) devices. The supply voltage was set to 1 V.

A. Open-defect detection

For the analysis of resistive-open defects, a 2000 μm-long interconnect is used to connect a transmitter and a receiver micro-bump. A high resistance (60 kΩ) is inserted in the interconnect to model a resistive-open defect. The test patterns for the detection of an open defect are shifted in at a frequency of 200 MHz and six clock periods are shown in Fig. 8. During the first two clock cycles, test patterns are shifted into the transmitter DWR cells. Test responses are captured by the receiver DWR cells in the third clock cycle. The remaining three clock cycles are used to shift out the test response from the receiver cells through TDO_P. As shown in Fig. 8, a test sequence of 1010 is shifted into the transmitter cells (V(N_1)), but due to the delay introduced by the resistive-open defect, the receiver cell cannot capture the correct value (V(N_OUT)). As a result, the incorrect value 0001 is shifted out.

Next, we determine the smallest resistive-open defect that can be detected. Fig. 9(a) shows the smallest detectable resistance when the shift frequency is varied from 50 MHz to 200 MHz. As the frequency decreases, the value of the smallest detectable resistance increases. This happens because the capacitance of the interconnect has sufficient time to charge and discharge as the shift frequency is decreased. At a shift frequency of 50 MHz (200 MHz), the smallest detectable open resistance is 90 kΩ (16 kΩ).

In addition to the shift frequency, the location of the open defect also affects detectability. We modeled a long interconnect using 2, 5, 10, and 20 RC segments. It can be seen

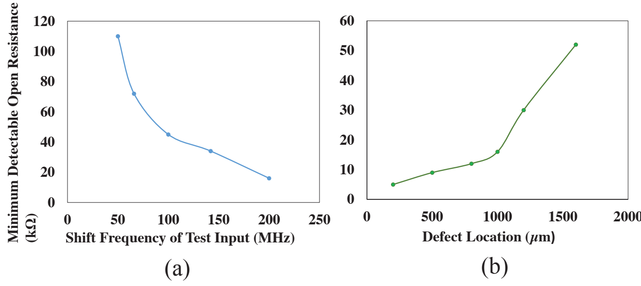

Fig. 9: Detectability of open defect: (a) Minimum detectable resistance versus shift frequency of the test input; (b) Minimum detectable resistance versus the defect location.

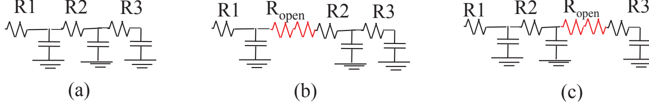

Fig. 10: Elmore delay model for an EMIB interconnect: (a) A fault-free interconnect with three RC segments; (b) A resistive-open between Segment 1 and Segment 2; (c) A resistive-open defect between Segment 2 and Segment 3.

from Fig. 9(b) that the smallest detectable resistance increases as the open is moved closer to the end of the interconnect. This is because the capacitance associated with the open is reduced when the defect is closer to the end.

This simulation results can be explained using the Elmore delay model. Let us assume that the interconnect under consideration is modeled using three RC segments as shown in Fig. 10. According to the Elmore delay model, the RC delay is $R_1(C_1+C_2+C_3)+R_2(C_2+C_3)+R_3C_3$. Now, we insert a resistive-open defect (R_{open}) between Segment 1 and Segment 2. In this case, the delay of the interconnect is calculated to be $R_1(C_1+C_2+C_3)+R_2(C_2+C_3)+R_{open}(C_2+C_3)+R_3C_3$, and the additional RC delay due to the defect is $R_{open}(C_2+C_3)$. Next, we place the open-defect resistance between Segment 2 and Segment 3. In this case, the RC delay of the interconnect is $R_1(C_1+C_2+C_3)+R_2(C_2+C_3)+R_{open}C_3+R_3C_3$ and the additional RC delay due to the defect is $R_{open}C_3$. Hence, it is evident that as the defect is shifted towards the end of the interconnect, the RC delay decreases because the capacitance in the “RC” product term decreases.

Next, we consider the occurrence of multiple open defects at different locations of an interconnect. For instance, we insert open defects in two different locations; the first at a distance of 500 μm from the transmitting end and another 1500 μm away from the transmitting end. Without loss of generality, we use a shift frequency of 200 MHz for analysis. We fix the first open defect at 500 μm (R1) with a magnitude of 10 kΩ and perform HSPICE simulation to determine the smallest detectable open defect at 1500 μm (R2). At a shift frequency of 200 MHz, R2 is 166 kΩ. As we decrease the shift frequency to 100 MHz, R2 increases from 166 kΩ to 200 kΩ.

The smallest detectable value of R2 also depends on the relative distance between R1 and R2. To analyze this relationship, we fixed the location of R1 and the shift frequency to 200 MHz as before, and varied the location of R2. The smallest detectable value of R2 with varying distance between R1 and R2 is given in Table II. As R2 is moved further away from

Table II: Distance between open defects affects detectability.

Distance between R1 and R2	Smallest detectable value of R2
500 μm	85 kΩ
1000 μm	166 kΩ
1500 μm	8 MΩ

Table III: Largest detectable short resistance for different combinations of inputs.

Interconnect 1	Interconnect 2	Interconnect 3	R_{short}
0	0	1	5 kΩ
0	1	0	7 kΩ
0	1	1	450 Ω
1	0	0	4.5 kΩ
1	0	1	1 kΩ
1	1	0	450 Ω

R1, the smallest detectable value of R2 increases rapidly. For a distance of 1500 μm, the smallest detectable value of R2 is high as 8 MΩ. This happens because when R2 is moved further away from the transmitting end, the capacitance associated with it decrease.

B. *Detection of short defects*

Fig. 12 shows simulation results for the detection of bridge defects. Two interconnects are shorted by a resistance of 1 Ω. The signal values applied to the interconnects are opposite to each other. Hence, the fault-free logic values of V(O1) and V(O2) are opposite to each other. However, due to the short, the logic values on the interconnects are incorrect.

Next, we analyze the largest detectable short resistance. As the value of the largest detectable short resistance decreases, the effectiveness of the detection method increases. We use a lumped model for analyzing shorts. Fig. 12 shows the results for the detection of shorts. The voltage level of V(O1) at 9 ns is analyzed when the short resistance is increased from 0 to 1.8 kΩ with a step size of 100 Ω. The voltage switches to 1.1 V when the bridge resistance is 1.8 kΩ. Thus, the largest detectable short resistance is 1.8 kΩ. As the shift frequency and the location of the short are varied, the largest detectable short resistance remains 1.8 kΩ. This is because the delay on the shorted path remains negligible even when different shift frequencies and short locations are taken into account.

Next, we consider shorts that involve more than two interconnects. For instance, we consider three interconnects shorted by two resistances. In order to determine the largest detectable short defect, we consider all possible combinations of signals on the three interconnects. The signal combinations and the corresponding value of the largest detectable short resistance are listed in Table III. We use ‘1’ to denote a high signal level and ‘0’ to denote a low signal level. The largest detectable short resistance for each combination is indicated as R_{short} in Table III. We exclude the ‘111’ and ‘000’ combinations as they do not lead to any observable error.

Table III shows that the largest detectable short resistance for input combinations (001, 010, and 100) is higher than that for the input combinations (001, 101, 110). We next consider two interconnects as aggressors and the third interconnect as the victim. When aggressors are low and victim interconnect is high (001, 010, and 100), the largest detectable short resistance

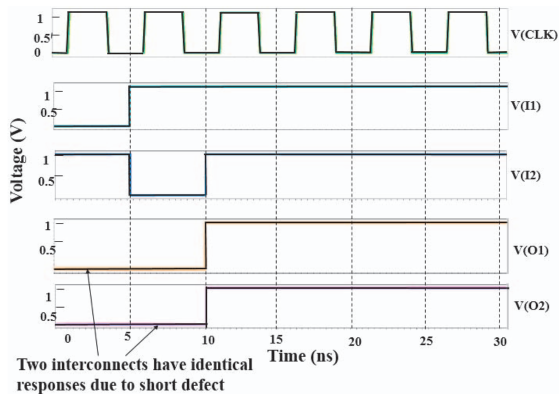

Fig. 12: Simulation results for short defects.

is larger. On the other hand, when aggressors are high and the victim is low (001, 101, 110), the largest detectable short resistance is small.

C. DfT Architecture Simulation

To perform RTL synthesis, the proposed architecture was first described in Verilog. Test benches were written in Verilog and simulated using ModelSim. In Fig. 11, we present the I/O signals of the TAP when it operates in test mode. Two IR-DR cycles are presented. In the first IR-DR cycle, the TAP is configured to select the secondary interface in the serial scan path. In this mode, the opcode value in the instruction register is '0001'. In the second IR-DR cycle, we program the TAP to be in SHIFTIN mode and the opcode value in the instruction register is '0000'. In the SHIFTIN mode, the send_select signal is set to high (Fig. 11).

D. Area Overhead

The hardware overhead due to the modified primary TAP controller and decoder is referred to as the control overhead, and the overhead caused by the changes in the DWR cells is denoted as the die-wrapper overhead. The proposed DfT architecture and the P1838 architecture were synthesized using Cadence Encounter RTL Compiler and PTM 45 nm standard-cell library. Table IV lists the area overhead of the transmitter DWR cell, the receiver DWR cell, and the TAP controller. The overheads of the transmitter DWR cell and receiver DWR cell were calculated with respect to a dedicated DWR cell. The area overhead of the proposed primary TAP controller was calculated with respect to the P1838-compliant primary TAP controller. The transmitter DWR cell and receiver DWR cell overheads are 10.9% and 18.2%, respectively.

Table IV: (a) Synthesis results; (b) Area overhead.

Cell name	Layout area
Standard DWR cell	14.09 μm^2
Transmitter DWR cell	15.69 μm^2
Receiver DWR cell	16.85 μm^2
Standard primary TAP controller	490.34 μm^2
Proposed primary TAP controller	497.02 μm^2

(a)

Type of Overhead	Overhead
Transmitter DWR cell overhead	10.9%
Receiver DWR cell overhead	18.2%
DWR cell (averaged)	14.55%
Proposed primary TAP controller overhead	1.4%

(b)

V. Conclusion

We have presented a DfT solution that enables pre-assembly testing of interconnects in an EMIB die. The proposed solution can detect open and short defects in the EMIB interconnects along with any defects that may occur in micro-bumps. We have presented HSPICE and ModelSim simulation results to demonstrate the effectiveness of the proposed approach.

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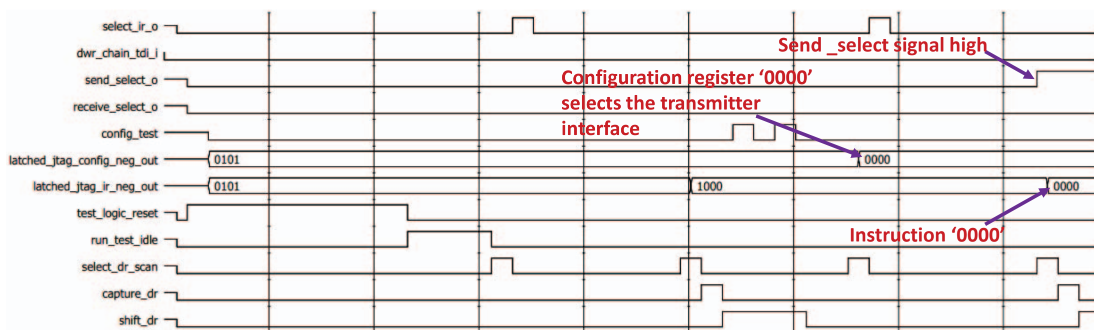

Fig. 11: Results for DfT architecture simulation.