Ultra low power microelectronics for wearable and medical devices

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***Abstract*— The requirements for wearables and portable medical devices present a number of challenges in terms of integration, autonomy and connectivity, and demand a careful co-design of hardware and software to reach optimum performance. This paper addresses these challenges by way of some recent examples of ASICs designed for ECG, EIT (Electrical Impedance Tomography) and PPG (Photoplethysmography) sensors as well as for non-invasive blood pressure monitoring.**

Keywords—ECG, EMG, EIT, PPG, subthreshold

I. Introduction

The constraints for wearable, battery powered medical devices are numerous. Such devices should offer a long autonomy to enable continuous monitoring for a long time. They should deliver reliable measurements even in the presence of motion artefacts or sudden ambient light changes. An additional challenge in the development of such systems is the size and weight reduction of its element and the integration (in particular the cabling) of the sensors in a wearable monitoring device which should be simple from a manufacturing and usage point of view. These challenges have been addressed separately in different ASICs developed for vital sign monitoring in the recent years. Ease of integration has been addressed by developing cooperative sensors interconnected by a single wire. Reliability of measurements while minimizing power consumption was addressed in a photoplethysmography (PPG) monitoring device which combines analog and digital processing to minimize power, while delivering highly reliable measurements. Power minimization has been addressed by the development of a complex System on Chip (SoC) combining on the same substrate analog amplification and filtering, digital processing and RF transmission to enable portable electrocardiogram (ECG) monitoring. The rest of the paper will describe in more details these 3 ASICs and show future developments.

II. Cooperative sensors

Cooperative sensors are a disruptive new approach that allows the simultaneous measurement of large sets of physiological signals during daily activities [1]. As shown in Fig. 1, the cooperative-sensor technology allows easy and effective integration of physiological-signal monitoring in smart garments because they require only one unshielded (possibly even non-insulated) conductive electrical connection without compromising with signal quality [2]. Therefore, the cooperative sensors can be easily integrated and connected by a conductive textile featuring bendability, elasticity, and breathability. The sensor size depends only on the integration level and autonomy requirements. This contrasts with state-of-the-art solution where the electronics is centralized with miniaturization largely depending on cumbersome connectors used to connect several shielded cables. The cooperative sensors are standalone, i.e., each with its own electronics and power supply (battery). A battery per sensor offers an additional degree of freedom allowing simpler yet better electronics. Finally, the battery weight and volume is spread over the sensing area resulting in a more 'seamless' system since there is no need for a big centralized electronics box. However, cooperative sensors must communicate to be synchronized and to centralize the data as illustrated in Fig. 2. They need only one electrical connection between the sensors, since the current returns via the body. Such strategy is well suited for cooperative sensors because it is simpler than the fully wired strategy and such electrical connection is anyway required for the measurement of biopotential and/or bioimpedance. The communication should use frequency bands that do not interfere with the measured signals. A current source *j* is used for the emitter driven according to the emitted signals (a voltage source could also be used) and for the receiver a load with voltage drop *u* as received signal.

An ASIC, which will be used in a system to measure ECG and body impedance at a certain frequency (50kHz) has been integrated in a 180 nm process. After processing, those signals can be used for impedance tomography, or extraction of non-occlusive blood pressure (NOBP). For the later case, 4 cooperative sensors are used (see Figure 1 right). The ASIC is used in each of the sensors, but is configured for the specific function of the sensor.

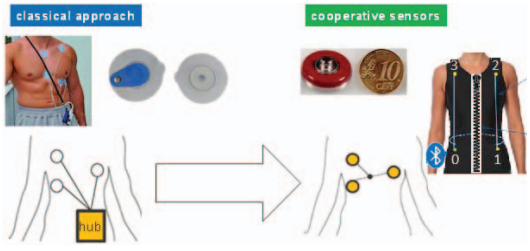

Fig. 1: Classical approach and cooperative sensors

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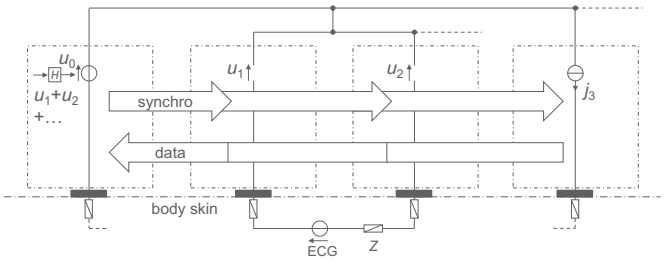

Fig. 2: Typical biopotential and bioimpedance sensing system using cooperative sensors linked with a single and simple electrical connection

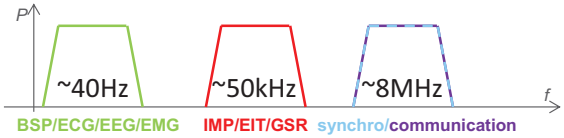

Fig. 3: Frequency band for BSP, IMP and communication

Sensor 0 acts as master, and thus generates a synchronization stream and collects the data from all other sensors prior to transmission through Bluetooth low energy (BTLE). Furthermore a current is injected in order to control the reference node (sensor 1) to ground potential. Sensors 1 and 2 measure the body surface potential (BSP) and impedance (IMP) signal, and send the data to the master through the communication channel. Sensor 3 injects a current and also sends digitized BSP measurement data to the master. The entire system is running on a single wire. The body is used as the return path. This is possible as the BSP, IMP and communication signals are located in different frequency bands (see Fig. 3).

The ASIC contains two main blocks: communication and sensing. The communication block (see Fig. 4) can be configured as either master or slave. In the first case, a synchronization data stream is sent out, that consists of pulses that are generated using an internal clock source. In the latter case, a dual-loop clock and data recovery (CDR) block extracts the sampling clock from the incoming data pulses (sent by the master). In the digital TX part, data semi-randomizing for uniform spectrum is applied prior to Manchester encoding. For every 1000th bit, the start of a new frame is indicated by a violation in the Manchester code ("code break"). Finally the data is pulse-modulated, i.e. data '1' is transformed into a positive pulse followed by a negative pulse. Data '0' is transformed into a negative pulse followed by a positive pulse. In the digital RX part, the detected pulses are demodulated, Manchester-decoded and finally descrambled. Code breaks are used to synchronize to the data frame.

The sensing part of the SoC is shown in Fig. 5. The BSP measurement chain consists of a pre-amplifier, a passive low-pass filter, an instrumentation amplifier, and an ADC. The signal gain (26 dB to 40 dB) and hi/low pass cutoff frequency (0.67 Hz resp. 40 Hz) of the pre-amplifier are set by external components.

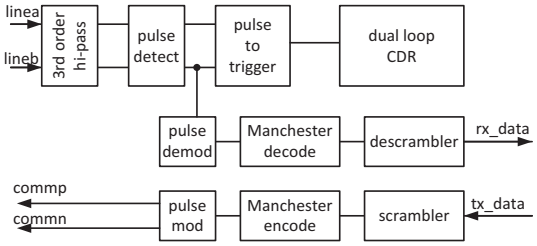

Fig. 4: Block diagram communication part

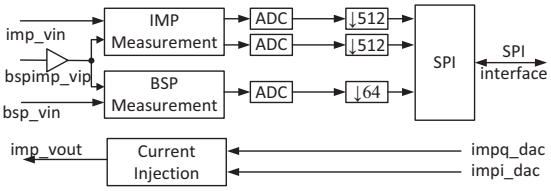

Fig. 5: Block diagram of the sensing part

The IMP measurement incorporates two functions: stimuli and measurement. For stimuli, current injection block delivers a modulated current in the 50 kHz band. It consists of a modulator, a filter and a voltage-to-current converter by means of an external resistor. The measurement chain consists of a pre-amplifier with filter, a de-modulator, a passive filter, and an ADC. First the in-band signal (49 kHz to 51 kHz) is amplified and out-of-band signals are suppressed..

In order to guarantee that measured results of ECG and impedance will not be sensitive to motion artifacts, or temporary changes of the skin conditions, the impedance between body and garment electrode had to be kept as high as possible posing a tough challenge on the front-end part of the sensing block. Another challenge was to guarantee that the DC current between electrodes will be close to zero, to minimize electrolysis below body electrode. For high dynamic range of measured signals, care had to be taken to limit noise feed-through from communication band into ECG / IMP band by demodulation. Fig. 6 shows a microphotograph of the ASIC. Its performance is summarized in Table 1.

III. Low-power PPG monitoring system

While sports watches with an integrated optical heart rate sensor technology (OHR), based on photoplethysmography (PPG) have been commercialized for several years now, the market has seen recently a widespread use of such functionality within the smartwatch products of the microelectronic and smartphone giants such as Apple, Samsung, Huawei, LG and Sony. Unsurprisingly, not all of these smartwatch products reach the same accuracy and reliability, especially during the presence of motion.

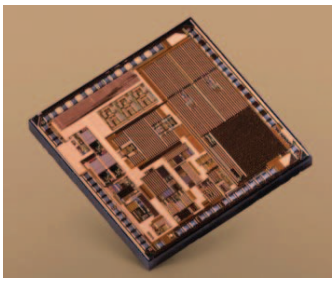

Fig. 6: Microphotograph of the chip

Table 1: Performances

Internal Supply	2.5V / 1.6V
Technology	180nm
ECG Noise (0.05Hz .. 150Hz)	1.6uV rms
ECG Immunity to IMP	< 1uV
ECG ADC	16b ΣΔ (8kS/s + 1kS/s)
Current injection	< 800uApp (50kHz)
IMP Noise	62 nV/ √ Hz
IMP ADC	16b ΣΔ (4kS/s)
Communication Data Rate	2Mb/sec

Actually, a comprehensive system approach is required to achieve the best heart rate measurement quality, and is even more critical to be able to measure additional parameters like RR intervals, heart rate variability (HRV) or perfusion, using a PPG sensor. PPG is based on the measurement of the changes in light absorption of the subcutaneous tissue of the skin, typically illuminated with an LED. The light is actually modulated by capillary blood flow, which is used to monitor heart rate. However, even with well-designed sensor interfaces, there are two major sources of error: ambient light and movement artefacts. Ambient light fast variations can become a major issue when its fluctuations show a high amplitude above the sampling frequency, which can occur with bright indoor lighting or when moving in sunny conditions. Today's available state-of-the-art solutions do not prevent the saturation of the input stage in every use case.

The HR extraction uses the PPG. An InfraRed (IR) Light-Emitting Diode (LED) lights up the skin while a photodiode detects the variations of the emitted light. As this light is disturbed by blood volume changes, electrical variations in the photodiode are related to the heartbeat.

The SPO2 extraction uses the absorption spectroscopy of the blood. An IR LED and a Red LED are used alternatively while a photodiode analyses the incoming light. When blood is saturated with oxygen, IR light is absorbed whereas Red light is reflected and reversely. The ratio between the reflected amount of light coming from the Red LED and the IR LED into the photodiode is proportional to the blood oxygen saturation.

The system developed optimally combines analog amplification, filtering and A/D conversion in an ASIC to pre-process the signal and enable an easy post-processing in a low-power micro-controller to extract a high quality measurement of the heart rate. The developed ASIC incorporates three measurement channels. Fig. 7 shows the analog amplification and filtering chain composed of Trans-Impedance Amplification (TIA), Ambient Light Removal (ALR) which substract a current at the TIA input to avoid saturation, Low-Pass Filtering (LPF), Sample-and-Hold (S&H) and Voltage Gain Amplification (VGA). LED drivers and Analog-to-Digital Converter (ADC) are also included as well as a sequencer for synchronization and an SPI interface. The ASIC allows a high level of miniaturization with few external components and is optimized in term of power consumption.

The analog chain described in Fig. 7 is copied three times. Two chains are needed to measure separately the Red and IR light from the related LEDs in the SPO_2 mode. All of them are used to add redundancy and increase reliability in the HR mode. In order to reduce current consumption, the LEDs are sampled with a very low duty cycle and synchronized with the S&H. The ALR circuit is implemented in such a way that there is no need for a specific phase of ambient light acquisition and removal. Furthermore, the chosen topology relaxes flicker noise constraints that might be significant in MOS technology. The signal is recovered at the end of the chain with a simple LPF and digitized with a suitable ADC.

From this scheme, two points are critical for the ASIC:

- The noise of the LED drivers and the TIA;
- The implementation of the LPF at the end of the chain.

During the LED switching-on phase, the photodiode current is the sum of the pulse rate signal (LED passing through the skin vessels), the ambient light (coming through the tissues directly to the photodiode), and the direct LED light (to the photodiode without passing through the skin vessels). Artifacts created by movements can saturate the chain and swamp the useful signal. To guarantee the needed dynamic, noise is a critical point, especially in front of the gain that is on the LED drivers and the TIA. A good trade-off between silicon area and current consumption has to be found to well balance flicker and thermal noise within the useful bandwidth.

The second critical point is the very low cutoff frequency required for the LPF. This implies a high RC time constant and, in turns, a huge silicon area. Resistance values are realized by switched capacitors, but increasing their values too much also increases thermal noise. Again, a trade-off should be done between noise, area and the need for external components. In this implementation, two external capacitors are needed, one after the S&H and one at the very end of the chain intended to prevent aliasing in the ADC.

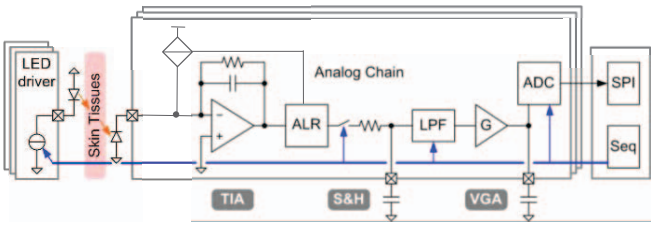

Fig. 7: Schematic principle of one analog chain and LED driver

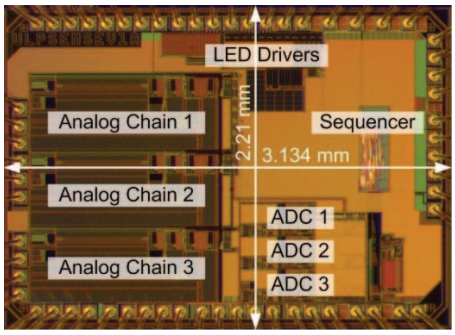

Fig. 8: Die photograph of the ASIC with dimensions

The circuit has been integrated in TSMC 0.18 µm, standard CMOS process. Two supply voltages are needed, 3 V for the input TIA and the LED driver, 1.8 V for the rest of the system.

The measured analogue front-end shows a consumption of 235 µA for each of the three analog chains and an output integrated noise lower than 10 μV_{RMS} within the 5 Hz signal bandwidth. The three ADCs consume 530 µA for an input referred noise of 18 μV_{RMS} within a 250 Hz bandwidth and a resolution of 15 bits. The ADC results are ready after 4 ms from the switching-on which allows duty cycling also on the ADCs. LED drivers can bias the IR and Red LED from a 200 µA PTAT current reference to respectively 20 mA and 120 mA in less than 30 µs, with noise level comparable to that of the TIA (good balance of noise along the chain). With a 0.6 % LED duty cycling and a 10 % ADC duty cycling, the total consumption of the ASIC including LED current is 390 µA . The on-chip analog filtering enables a very low data sampling, thus reducing considerably the power requirements for digital processing, so that the total system power consumption compares very favorably to commercial systems.

IV. SoC for ECG monitoring

An approach to minimize power consumption consists in integrating all processing (analog conditioning, digital processing, communication, power management) in a single chip called an SoC. An example of such a circuit is an SoC developed for multi-lead ECG monitoring [3, 4] with standard electrodes. It integrates on a single chip an ultra-low-power signal acquisition front-end with analog-to-digital converter (ADC) for 3-lead ECG, a low-power digital signal processor (DSP) and a low-energy radio frequency (RF) transceiver. The SoC runs from a 1 V supply, compatible with a single alkaline cell, and is optimized for long battery life.

The analog front-end is illustrated in Figure 1. It consists of 3 ECG leads capacitively coupled, each followed by an amplification chain with a gain programmable up to 46 dB and an adjustable cut-off frequency from 100 to 480 Hz. It features a measured total harmonic distortion (THD) of 54 dB with the nominal gain setting of 35 dB and an input referred noise of 1 µV for a current consumption of 27 µA (biasing, second stage of amplification and buffer to the ADC included). For a maximal input voltage of 4 mV, the achievable resolution of the amplification chain is 12 bits.

The sensor interface also incorporates an active ground control to cancel large common voltage variations. It probes the common mode voltage of the three leads through a simple star connected resistors network and feeds back a signal corresponding to the inverted value of the common mode. Finally, the sensor interface also implements a lead-off detection by injecting an AC square signal via the active ground connection and detecting it on the 3 ECG leads.

A low power and low voltage sigma delta ADC was specifically designed to digitize the signals out of the 3 amplification chains. Measurements show that it achieves a resolution of 14 bits and a THD of 52 dB for an input signal of 300 mV.

The digital core of the Icyheart SoC is built around the **icy*flex*** DSP, a 32 bit low-power microcontroller with DSP functions (parallel dual MAC) [5], which is used to analyse in real-time the ECG data provided by the analog front-end. This enables to extract high level information such as heart rate, ECG fiducial points or detect special events such as arrhythmia on-chip and therefore strongly decrease the amount of data to be transferred off-chip and the power consumption associated to data transmission.

The low-power RF [6] transceiver operates in the ISM863-928 MHz range. The receiver part consumes 3 mW in receive mode at 105 dBm, and 4.5 mW in transmit mode at -5 dBm. It is not only optimized for continuous operation but also for RF channel power sampling. This allows efficient implementation of low-power protocols minimizing the receiver activity.

Additional peripherals such as a voltage-divider to also address lithium batteries, SPI, I2C, UART, I2S are all included on the same chip, resulting in a compact system solution. Fig. 10 shows a picture of the SoC with area distribution.

The design of an optimized low power analog front-end requires a deep knowledge of Integrated Circuit (IC) tradeoffs. Reducing power consumption increases thermal noise whereas decreasing input capacitance increases flicker noise, and increasing input impedance increases non-linearity and power.

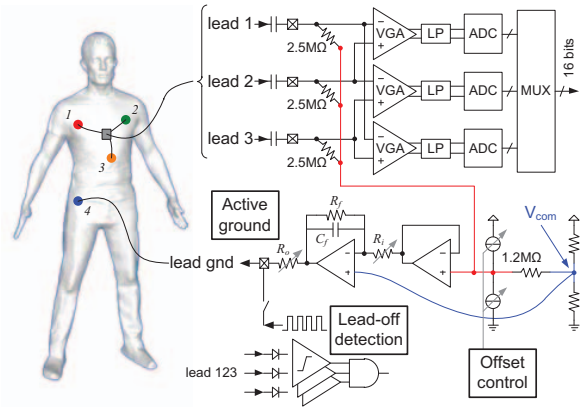

Fig. 9: Analog front-end

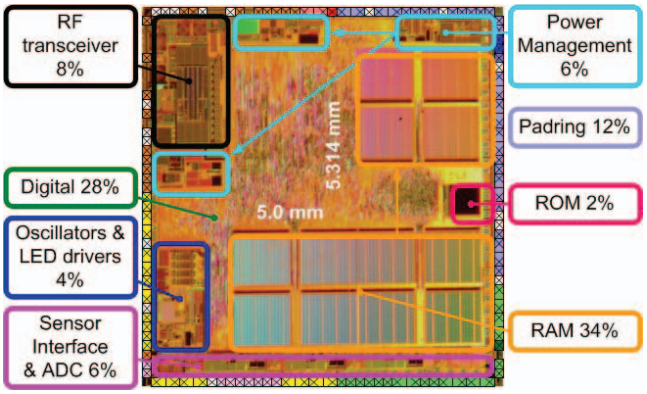

Fig. 10: Microphotograph of the IcyHeart chip with surface distribution

In term of noise, the most critical part of a front-end is the first stage of amplification. The implemented circuit is an open-loop g_mR amplifier whose gain is a function of the transconductance (g_m) and the resistor load (R_L). It is followed by a Differential OPerational Amplifier (DOPA) and an RC passive filter. A detailed schematic of the amplification stage is given in Fig. 11.

The g_m transconductance of first stage is made with a classical differential pair of PMOS transistors in weak inversion without degeneration and loaded with the resistors. The input differential pair is supplied by the internal high voltage (3V generated on-chip by a low power step-up) to allow sufficient headroom on the common mode ECG signal whereas the other parts of the circuit are all 1 V compatible. For small signals, the voltage gain A_V can be written as (1):

$$A_V = g_m \cdot R_L = I_D/(nU_T) \cdot R_L \quad (1)$$

I_D is the drain current of the transistors in the differential pair, R_L the load resistor, U_T the thermodynamic voltage and n the slope factor. As the I_D current comes from a PTAT current (Proportional To Absolute Temperature), this gain does not depends on resistance corner or temperature variations and can be tuned either with current biasing or with resistors load.

In term of noise, the g_mR gain is the best trade-off for low power consumption. Indeed, the number of transistors contributing to noise is minimal and all of the current is used for the gain. By selecting a proper biasing scheme, it can be guaranteed that the $g_m \cdot R$ gain value A_V is constant and independent of the temperature and technology parameters [7].

The whole SoC has been tested in real conditions. The global power consumption is 850 uW for a 1 % power sampling (duty cycling) of the RF part. The analog front-end including A/D conversion consumes 100 µW per channel, which compares very well to commercially available ECG frontends with digital output, In sleep mode with a real-time clock running the whole SoC consumes only 1 µW.

V. SUBTHRESHOLD DIGITAL DESIGN

Low power applications (such as body area networks, portable health monitoring equipment, implants, etc…) are demanding solutions to go always lower in power consumption and simultaneously to support always more features. One possibility to reduce the power consumption is reducing the supply voltage (Vdd) of the circuit.

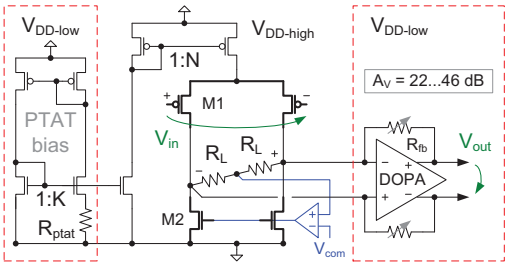

Fig. 11: Voltage gain amplifier

Two major benefits can be achieved by reducing the supply voltage:

- Power budget reduction: Dynamic (Pdyn) and static (Pstat) power both depend on Vdd. Therefore, reducing Vdd reduces both power components. For Pdyn, the reduction is quadratic. For Pstat the reduction is linear (see Fig. 12)

- Enabling energy harvesting: Power budget reduction can allow the development of autonomous ultra-low power devices that can be completely supplied by energy harvesting techniques. The target is to spend less power than what can be harvested from the user or from the environment; a typical application developed at CSEM is an artificial retina powered solely by the light entering the eye.

When Vdd is lower than the threshold voltage of the transistors (Vt), the transistors are in so called sub-threshold operation and the power consumption is drastically reduced.

It can be easily shown that the total energy (dynamic + static) experiences a minimum at a supply level that is usually near or slightly below the threshold voltage of the transistors: this point of operation is called the Minimum Energy Point (MEP) and is illustrated in Fig. 12.

However, ensuring the correct operation of sub-threshold designs is challenging as the ratio between active (Ion) and leakage (Ioff) currents is reduced. CSEM has developed a methodology to adapt existing design flows for sub threshold design, thus allowing operation at the Minimum Energy Point.

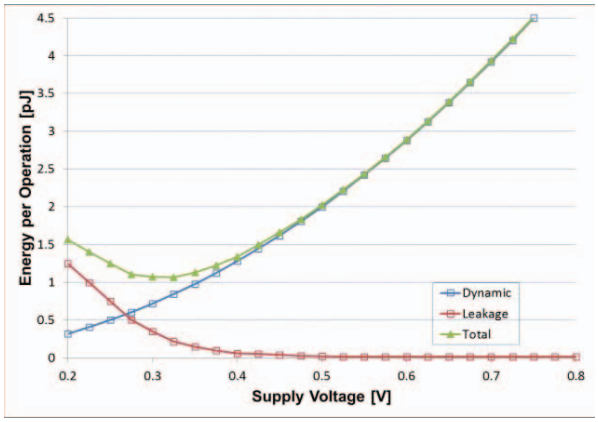

Fig. 12: Energy per operation scaling

Application Specific Integrated Circuits (ASICs) have to be designed not only to satisfy their requirements in terms of energy consumption, but they also have to fulfill their specified functionality and therefore need to work at a given minimum frequency. CSEM has developed several IPs and techniques allowing to dynamically adjust the power consumption depending on the workload and the conditions of operation what allows to find the optimum operating point of the circuit in all conditions: typically, it is possible to temporarily boost the frequency of operation when more processing power is needed (at the cost of extra power consumption) before going back to a low power mode with minimum power consumption. Those techniques are generally described as Adaptive Dynamic Voltage and Frequency Scaling (ADVFS); on top of those techniques, CSEM added automatic body bias control to go even one step further in the optimization of the power consumption.

VI. Toward ultra-low power EMG SoC

The H2020 DeTop project addresses the scientific, technological and clinical problem of recovery of hand function after amputation. The actual active prosthesis are known for their poor functionality, controllability and sensory feedback, mainly due to the use of surface electrodes. The goal of the project is to develop a novel prosthetic hand with improved functionality, smart mechatronic devices for safe implantable technology as illustrated on Fig. 13. Targeting ultimately implantable devices, the power consumption of the sensing chip is of utmost importance to facilitate powering and minimize heating. Within the DeTop project, CSEM is developing a low-power SoC, illustrated on Fig. 14, which is used for both control of the actuators and collecting sensory feedback data, exploiting the subthreshold approach described above. The SoC is based on CSEM's low-power icyflex2 processor combined with its icyTRX ultra-low-power transceiver and a real-time communication protocol, also developed by CSEM. The SoC enables removal of the cabling to the control unit; increasing the flexibility of the hand and the versatility of the stump measurements. A low-power optimized integrated EMG analog front end is also being designed by CSEM for the interface with the sensors.

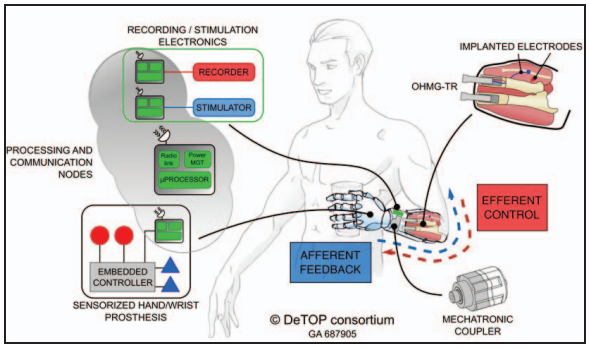

Fig. 13: Goal of the DeTop H2020 project

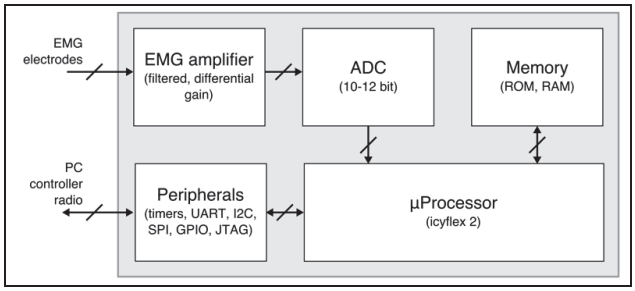

Fig. 14: SoC for artificial limb control

VII. Conclusion

Wearable medical devices face several challenges to be comfortable, offer a sufficient autonomy and deliver reliable results. The cooperative sensors represent a new promising approach to ease integration in wearable systems while maximizing signal reliability. On-chip analog processing to reduce the sampling rate decrease subsequent processing requirements and enable to optimize the system power. Finally, the SoC approach in combination with subthreshold enables drastic power reduction.

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