Reconfigurable Embedded Systems Applications for Versatile Biomedical Measurements

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***Abstract*—Nowadays, the majority of the monitoring devices used in clinical settings is limited to specific applications and powered by highly specialized microcontrollers and pre-programmed DSP systems. Moreover, these kind of devices are usually connected to a high capacity battery to operate in case of power blackout. Nevertheless, considering that all the measured bio-signals depends from an amperometric or potentiometric transducer, it should be viable to integrate them on a single device with multiple probes, reprogrammable sensor-fusion capabilities and on-board signal processing. Within this context, in this paper, we present a design concept for such a device. Exploiting FPGA reconfigurability, various analog front-ends can be connected to the device and configured to return the measured signal or the output of the desired signal processing to the user. Multiple case studies with different sensors and end-user applications are described. The high degree of parallelism and the reduced frequency of the embedded FPGA coprocessor make it suitable for all the applications that are subject to medium/low power and cost constraints such as portable Point-of-Care devices or emergency medical centers.**

I. Introduction

Commercial devices for multi-parametric physiological measurements are generally focused on the analog front-end of input channels, while additional computations are off-loaded to companion software or pre-programmed Digital Signal Processors (DSP)[1]. Whereas the entire processing is self-contained in the hardware device, as in Intensive Care Unit (ICU) monitors, it is generally bounded to a fixed behaviour and presents limited space for hardware or firmware improvements. In this scenario, the realization of multi-purpose and connected biomedical devices is driven by economical reasons. A General Electric study of 2012 [2] pointed out that, although modern devices integrate multiple functions, the number of devices per bed increased of 62% (with a +90% in maintenance costs), and the inventory utilization remained under 50%. The usage of connected devices along with indoor positioning techniques could reduce the time needed to locate the inventory, limit over-provisioning and optimize the staff workflow. In addition, Internet of Things (IoT) enabled healthcare technologies are expected to cover 41% of the IoT market share by 2025, with $1.1 trillion annual growth [3].

More in general, the usage of *smart* portable devices represents the major driver of Point of Care Testing (PoC or PoCT) paradigm, where various medical diagnostic tests are conducted at/near the point of care instead of relying on laboratory analysis i.e. portable ultrasonography, non-invasive blood oxygenation estimation, biochemical diagnostics and advanced techniques for diabetes, nerve conduction disorders and coronary diseases.

These kind of devices is always bound to power consumption constraints: while the standard ICU monitors are plugged to power wall and contain a capacitor battery in case of short power outages, portable monitors are more limited with a battery time from 3 to 6 hours for screen connected monitors (source *Heyer medical*), up to 1-2 days for simplified Holter ECG recorders. These requirements pose major issues in all the scenarios where the access to electricity is unreliable or subjected to intermittent supply, i.e. in medical centres for rural developing communities. For all these reasons we believe that the development of a device which is low-power, versatile, connected, and rechargeable with multiple power sources would represent a breakthrough in the field of smart medical devices.

Modern programmable devices, like FPGAs (Field Programmable Gate Arrays), provide an interesting alternative for the implementation of biomedical signal processors. Compared to standard microcontroller-based solutions, FPGAs can be used to gather data from the sensors in parallel to avoid multiplexing techniques and delays in the data processing cause by single instruction operations. From a sensor point of view, the FPGA connections can be configured to directly acquire digital data, connect analog inputs to the internal ADCs, and use port outputs to emit signals or control actuators. In this way, the low level reconfigurability of the FPGA can be used by programmers to keep the clock frequency and the dynamic power consumption low, while maintaining a high throughput for the most common biomedical signal processing algorithms. Moreover, System-On-Chip (SoC) FPGA platforms merges the architectural capabilities of programmable logic with the high-level coordination and versatility given by general purpose CPUs and full-stacked operative systems.

The aim of this paper is to present the various possibilities offered by FPGA SoC regarding biomedical measurements, more specifically a Proof of Concept of a portable device with:

- low power consumption, and independent from the type of power source available.
- reprogrammable I/O connections to manage multiple sensor probes.
- a application-wise HW/SW library to process the signals without external DSP processors.
- the possibility to be programmed both at HW and SW level, depending from the desired application.

The rest of this paper is organized as follows. Section II de-

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scribes the current studies on FPGA-based physiological data acquisition. In Section III, the key aspects of the proposed device's architecture and methodological aspects are introduced. In Section IV Three case studies regarding a multi-channel EMG sensor, a remote ECG monitor and a heterogeneous sensors system are presented. Finally, in Section V, is descibed a comparison of the results obtained in terms of processing speed and power consumption.

II. Related works

To the extent of our knowledge, one of the earlier application of reconfigurable hardware for wearable technology can be found in [4]: the study proposed a body area network composed by multiple hybrid CPU-FPGA nodes where every node took advantage of the FPGA reconfigurability to acquire different signals and reduce power consumption. The case studies proposed were voice recording compression and voice context recognition by means of neural networks.

In recent years various FPGA solutions were presented, although the majority of the studies is dedicated to electrocardiographic (ECG) acquisition and signal processing. In [5] a flexible three lead ECG recorder was implemented using a combination of a FPAA (Field Programmable Analog Array) for ECG conditioning and a FPGA to detect QRS complexes in the signal, and the same architecture was used in [6] to implement an adaptive denoising filter for fetal heart rate extraction. Conversely, in [7], a single SoC included both ECG conditioning and R-peaks detection, using the ARM processor to transmit data over ethernet.

Other studies exploited the FPGA versatility to diagnose pathologies in real-time from ECG traces. In [8] is described the implementation on FPGA of a block-based Neural Network for arrhythmia identification, which employed evolutionary algorithms to reconfigure the network and the classifier. In [9] a particular type of neural network called Self-Organizing Maps (SOM) was implemented on the fabric logic along with the QRS detector and a discrete Fourier transform block. A fuzzy clustering classifier for ECG is described in [10], in this particular case, the algorithm was not implemented as hardware block but on a Xilinx MicroBlaze soft-processor running on the FPGA. Nevertheless, the data reduction provided by fuzzy clustering and the low frequency of the soft-processor (50 MHz, maximum) allowed a rough increase in the power efficiency of the system.

With regard to the power efficiency of FPGA-based systems, various studies exploited different circuital aspects. In [11] is modeled the dataflow from a set of wearable inertial units (IMU) and fixed point arithmetic to limit the number of floating point operations (which are known to be *costly* on FPGAs) obtaining an efficiency increase of 13% and 95.7% compared to an ARM Cortex 9 and an Atmel32 microcontroller. In [12] a system combining data from EEG and EMG sensors controlled a neural stimulator for mice, exploiting sensor multiplexing and the reuse of digital filters; the entire system needed only 44.3 μW with a control loop latency of 39μs. More advanced techniques can be used to design the electrical properties of the system, in [13] a HW Burg's autoregressive (AR) estimator was simulated with circuit buffers optimized for sub-threshold region (supply voltage < 0.65V) and the lowest clock frequency possible (2 MHz for a 20 kHz bandwidth signal), obtaining an *estimated* decrease of power consumption of *197.7*x

Concerning the PoC paradigm presented in Section I, the studies found can be divided in single-purpose and multi-purpose devices: in the first one the devices that take the most advantages from FPGAs are portable ultrasonographs (US). In [14] a B-mode color flow US scanner was implemented, and the Processing Logic (PL) was used to control the US pulser, the receiving channels, and the data processing necessary to generate the color image; moreover, it included a Bluetooth module to be connected with other medical systems. In [15] is implemented a similar device, and the FPGA look-up tables (LUTs) were exploited to store sinusoidal waves for quadrature demodulation and log-compression values in an efficient manner. In both the cases, a fast and efficient control was necessary to comply with the US pulsers high frequencies (30-40MHz) and high voltage drivers ($\pm$ 60-70V).

A multi-purpose PoC was studied in [16] for emergency medical services: the acquisition of a 2-lead ECG was managed by a 8 channel reconfigurable analog front-end (with multiple I/Os for system expansion), the signal was stored and transmitted through IEEE 802.11 protocol, and the power supply system was designed to be interoperable with solar panels, standard lithium cells batteries and even vehicle batteries. In this case a Xilinx Spartan-3E FPGA was used to filter the signal and to reproduce a plot on a small LCD panel.

Starting from these studies, our proposal is to design a Proof of Concept device for PoC versatile measurements, with multiple I/O probes, low power, and a library of functions and applications that can be loaded as necessity.

III. Proposed architecture

In this section is described the general structure of the FPGA board used in the experiments, and its key functionalities such as the power management block, and the wireless communication model.

Device structure

The different case studies were implemented on a Xilinx Pynq-Z1 development board (`www.pynq.io`) which comprises a SoC with ARM Cortex A9 CPU and a Zynq XC7Z020 PL, USB host and programmable GPIO connectors both with PMod and Arduino Shield layout. The board includes a 16bit ADC with 500 KS/s maximum sampling frequency. The base design integrates all the connectors including HDMI and audio I/O, but the reconfigurability of the FPGAs allow the application designers to remove undesired components, or viceversa to extend its capabilities, without the need to modify the physical design or to manage the power consumption of multiple discrete components. All the case studies presented here are implemented on the MicroBlaze soft-processor (or

with minimal variations on the base HW design) to demonstrate how the final user can exploit FPGA capabilities and implement power-*wise* solutions even without the extensive knowledge of the underlying hardware and the steep learning curve required by pure FPGA programming.

Key functionalities

The connectors on the board are configured for programmable data transfer, the protocols currently supported are GPIO, I2C, UART serial, and SPI for data I/O, analog input on the PL ADC and Pulse Width Modulation (PWM) outputs controlled by precise PL timers. This versatility allow the creation of both pure sensing applications or control loop applications with input and outputs such as [12] or [15].
As stated in Section I, a versatile device should be independent from the power supply. Thanks to the board characteristics, the system can be powered through 5V USB port or any 7-15V source. However, to keep the device portable and to handle power shortages, we have included a backup battery between the processing system and the power plugs. The chosen battery is a 2300 mAh @11.1V Li-PO battery with a energy capacity of 25.53 Wh. A scheme of the power management is depicted in Fig. 1.

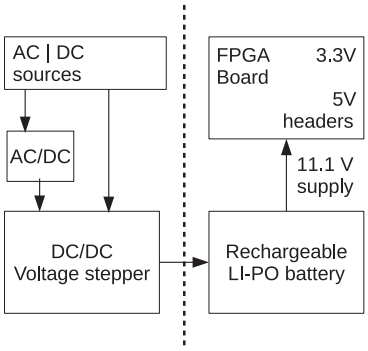

Fig. 1. Block description of the device power management. The central line divides the independent power supply circuit from the proposed portable device.

The power supply circuit can be connected to AC sources i.e. wall plugs or DC sources i.e. batteries, solar panels. A DC/DC regulator boost or step-down the input to recharge the battery. At the other end, the battery is connected to the DC input of the device; the ports on the board provides 3.33V and 5V references for sensors power supply and voltage reference. All the metrics relative to power consumption and estimated battery life are presented in Section V.
The communication between the device and other systems is made available using wired (Ethernet cable) and wireless (IEEE 802.11 and 802.15) connections. The device networking allows advanced end-applications such as remote monitoring, integration inside hospitals' IT networks or data transmission to PoC caregivers devices. Moreover, the board's FPGA can be configured to provide to off-load the CPU in data encryption/decryption, and to be compliant with the level of security and privacy required for specific applications. The desired communication protocol can be implemented using the OS software stack abstraction, or connecting the communication ports directly to the PL fabric.

IV. Case studies

In this section, 3 case studies are presented to highlight the different possibilities made available by the proposed device: a multichannel EMG sensor with digital signal pre-processing, a remote ECG monitor with noise reduction and wireless communication and the central node that receives the signal and extract various parameters, and a heterogeneous sensor to acquire different signals in an efficient manner. All the results and signal representations are found in Section V.

A. Multichannel EMG sensor

Multi-channel surface EMG sensors recently became interesting for motion recognition (8-10 channels), and for motor fiber conduction studies (high density 64-128 channels). EMG signal sensors can benefit from the high parallelism of FPGAs because every channel is generally subject to the same pre-processing stages.
In this study, two commercial Grove differential EMG sensors with 2^{th} order amplifiers, were connected directly to the board ADC. The electrodes placement followed the [17] system for the *flexor digitorum* and the *extensori carpi ulnaris*. On the MicroBlaze soft-processor that manages the ADC acquisition we implemented a Mean Absolute Value (MAV) function, a feature commonly used for EMG diagnostics or hand gesture recognition systems. The sensor used in this case uses a 0 - 3.33V reference and the rest value is placed at 1.5V. Given that, the algorithm is implemented right after the ADC read and employ integer arithmetic to boost performances directly on the soft-processor.
The MAV formula is the following:

$$MAV = \frac{1}{N}\sum_{i=1}^{N}|X_i| \tag{1}$$

and it is often used in EMG protocols to study the activation of muscles, along with the ratio between different MAV's channels [18][19]. Although it presents a SNR slightly lower compared to the Root Mean Square (RMS) [20], it is faster to compute in very low-power processors or direct HW blocks because it does not need the *costly* square root and both the sums and the divisions necessary can be simplified exploiting unsigned integer ADC representation and time windows with $N = 2^n$ samples. Acquisition examples and performances are in Section V.

B. Remote ECG monitoring

In this case, a 2 stage differential amplifier was re-purposed to work as a ECG bipolar 1-lead amplifier directly connected to the analog input. The FPGA is configured for typical AC noise filtering and low frequency drift removal. In addition, the device is configured on the software side to communicate with a central manager over TCP/IP local connection. The system functions as *record* and *live* mode.

In live mode the device connects to a central node, which runs a tool for signal visualization and monitoring. The wireless port uses a Ralink RT5370 802.11 WiFi device controlled by the board OS. Both the boards use queued buffer sockets to manage possible delays in the data transfer.
Given that the sampling frequency of the signal (250Hz in this case) is far lower than the PL clock frequency (100MHz), we can observe how most of the processor time is spent waiting for the next sample. In the best case scenario, such as dataflow polynomial filters, the processing time is known and fixed, and the sampling delay can be stretched to increase the sampling frequency or to fit other signal processing functions. Exploiting the tight control on the sampling interval permitted by the PL timers, an IIR Butterworth notch filter has been implemented directly in code, decreasing the time delay between samples accordingly.
An example of stretched time intervals is represented in Fig. 2.

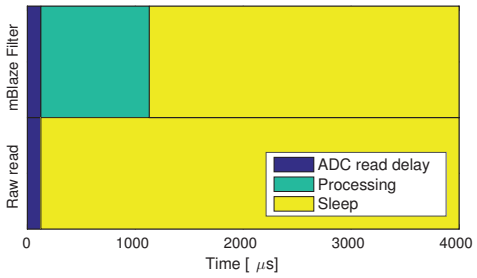

Fig. 2. Acquisition process of an ECG sample @ 200Hz. *Raw Read* is the acquisition of a single sample without further processing, *mBlaze Filter* includes a 50Hz noise IIR filter.

The sample delay is exploited also to manage remote monitoring, while the PL unit is waiting in the sleep cycle, the PS reads the sample from the shared memory and send it to the monitoring central node. On the central node (in this case another Pynq board) a monitoring software receives the data, plots the ECG trace and detect QRS complexes (using the algorithms described in [21]) and calculate subject's N-N intervals for Heart Rate Variability (HRV) studies. The ECG graph can be visualized on screen using the HDMI out port.
In record mode, signal acquisition and processing are performed on the ECG node. The ECG recording stops after an hour and the PS automatically switch to signal analysis mode, where multiple HRV parameters are estimated on 5 minutes intervals (with 1 minute overlap). After the computation, a report file is generated and the device is shut down to limit battery consumption. The HRV parameters considered were: Interbeat Intervals (IBI) mean and deviation, RMSSD, Pnn50, and spectral power density with LF and HF segmentation; all the formulas and meanings can be found in [22].

C. Heterogeneous signals recording

The techniques presented before converge when different signals with different bandwidths need to be acquired together. Here an ECG signal is acquired at 250 Hz, while the signal of a Galvanic Skin Response (GSR) sensor is recorded in parallel from a second soft-processor. The GSR is widely used as a rough estimator of the activity of the autonomous nervous system and it shows correlates with the HRV intervals. The GSR bandwidth contains a high frequency *phasic* component, which is related to transient stimuli, and a *tonic* component under 0.15Hz which measures overall autonomic activation. For this reason, the sampling frequency was kept at 2Hz and the clock frequency of both the soft processors was reduced accordingly to minimize dynamic power consumption.
The *naive* parallelism allowed by multiple soft cores differentiate FPGA-based devices from regular microcontrollers, that generally rely on multiple ADCs stages or time multiplexing techniques to acquire multiple signals with mixed sampling frequencies.

Remarks: Independently from the case studies presented here, the memory-map *Mailbox* protocol used for the PS-PL communication can be re-purposed to control and orchestrate the different cores available on the PS and the PL fabric i.e. the Mailbox *CMD* value used as a timing token which moves through the cores and regulate their execution.

V. Results

In this section are presented the measurements metrics for power consumption, and a characterization of different parameters for all the case studies mentioned in the preceding Section.
The measured bootstrap time of the device is 3.12 seconds (PL fabric) and 23.30 seconds with full software stack; the device can be configured to boot PL-only applications for specific purposes and emergency response scenarios, although this modality can limit the connectivity options.
The power consumption was measured using a commercial energy logger connected to the AC power supply. If not stated differently, the device uses base configuration with ARM core running at 650 MHz and 3 MicroBlaze cores at 100 MHz. The current absorbed by the device and the wattage are described in Table I.

Table I
Device modes with required power, along with the estimated battery life. Battery characteristics in Section III

Mode	Current [mA]	Voltage [V]	Power [W]	*Est.* battery life [hours]
PS Sleep, PL Off	20	4.8	1.9	13:25
PS On, PL Off	20	5.8	2.4	10:40
PS On, PL On	30	7.6	3.3	7:40
EMG (A)	30	8.2	3.5	7:20
WiFi On (B)	40	8.8-9.0	4.1	6:15
PL downClk (C)	30	6.7	2.8	9:10

It is visible that the wireless transmission and the MicroBlaze PL contribute to most of the power needed by the device. Less power hungry solutions will be advocated in Section VI. The down-clock of the PS from 650MHz to 325MHz has been tested, although its contribution was marginal with respect to

the other components.
In general, the measured power requirements are consistent with analogous commercial solutions, plus, it is important to state that this study is focused on medical appliances that have loose power constraints compared to wearable or implantable devices. In addition, we can observe that for all the case studies presented, power and current absorption are low enough to fuel the device with portable solar or wind generators, and guarantee its usage in power constrained environments.

A. Multichannel EMG Sensor

In Table 2 are described the maximum sampling frequencies for the sensors' structure in Section IV-A. The floating-point conversion from ADC level to Voltage has a cost in processor time near to the calculation of a 32 points MAV. Alternatively, the simple structure of the MAV function make it suitable for fast implementation on HW using high level synthesis tools. Whilst above-kHz sampling rate are present in literature (i.e. in [23]) for SNR or machine learning purposes, a $f_s = 1kHz$ is enough for most of the EMG applications. The Fig. 3 depicts the activation of the measure muscles during a combined movement of wrist extension and finger closure, and the MAV signal gives a clear representation of the muscle activation during the movement. Since the base architecture employs 32bit unsigned integers blocks in the DDR memory to communicate between the PS and the PL, the performances can be increased with the number of EMG channels by packing two channels read (with 16bits each) inside a single block and reducing the number of operations on the memory bus.

Table II
MAXIMUM SAMPLING FREQUENCY AND READ DELAY FOR VARIOUS EMG SENSING MODALITIES.

Method	max f_{sample} [Hz]	Read delay [μs]
Raw ADC	5691.26	175.71
Voltage	4281.23	233.58
MAV (N=2)	5489.89	182.153
MAV (N=8)	5431.92	184.10
MAV (N=32)	4367.67	228.95

B. Remote ECG monitoring

In Fig. 4 are visible to ECG traces read from the sensor with and without the IIR filter enabled. The improvement in the quality of the signal was measured using spectral Signal-To-Noise ratio (SNR) and the average improvement was 21.47 dB (or 7x) compared to the noisy signal. The time necessary to send a sample from the ECG board and to receive the ACK back was measured to assess the wireless network performances: the obtained average delay was $227 \pm 42\mu s$ which is far lower the $4ms$ necessary to acquire a sample at 250Hz. Nevertheless, a queue buffer is present on both the transmitter and the receiver to be compliant with faulty connections or re-send requests.

In Table III are represented the performances for HRV analysis on the board and on a laptop equipped with Intel i5-2520M CPU running the same algorithm. For testing purposes

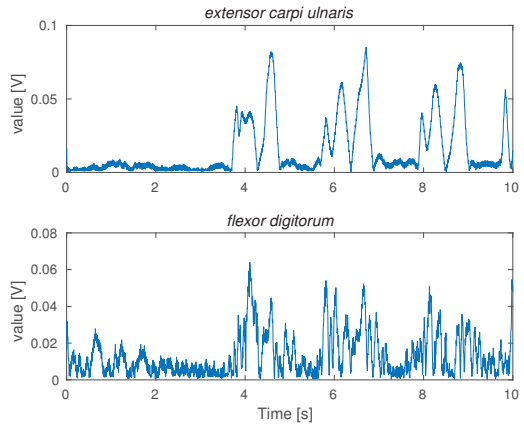

Fig. 3. Example of the acquired EMG MAV signal during wrist extension and finger closure movements.

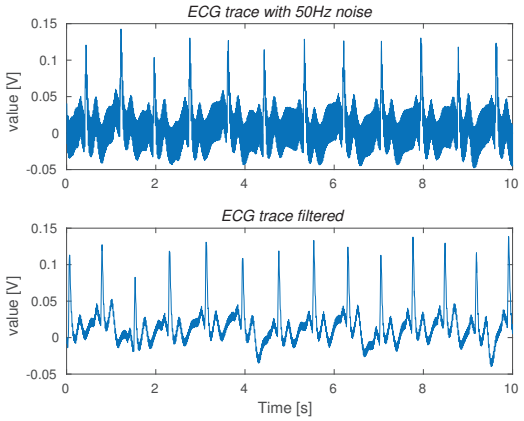

Fig. 4. different ECG traces acquired w/out signal processing (50Hz interference visible), and with IIR digital filtering.

both the systems run the same Python code with minimal optimizations (i.e. array pre-allocation). The peak detect function can be found in [21], while the Lomb-Scargle periodogram algorithm is based on [24]. Both the devices were connected directly to the power outlet, hence no power was absorbed to recharge the batteries.

Table III
COMPARISON OF CPU VS BOARD PS FOR 5 MINUTES HRV PARAMETERS CALCULATION. AT THE BOTTOM: POWER REQUIRED BY THE TWO DEVICES

Routine	CPU [s]	Board PS [s]
Peak detect	0.735	1.735
Peak diff	4.63e-05	4.13e-04
IBI mean/std	2.06e-04	1.2e-03
RMSSD	8.32e-05	7.24e-04
PNN50	7.59e-05	6.64e-04
Lomb-Scargle	7.98e-01	7.61
LF, HF, LF/HF	6.64e-05	3.65e-04
Total	**1.534**	**9.34**
Power	32.6 W	2.4 W

Although the board executes the code *6.1x* slower, it com-

pensate with a power consumption of 2.4W (30 mA) against the 32.6W (340 mA) of the laptop, resulting in an increase in power efficiency of 2.23x and 11.33x in current absorption. Nevertheless, we can observe that on the board, 81.5% of the time is spent for the Lomb-Scargle computation of the power spectrum, and for this reason it represents the operational bottleneck and a good candidate for HW implementations.

VI. Conclusions

In this paper, different applications for biomedical measurements were presented. All the case studies were implemented using a SoC FPGA development board by Xilinx. The results shown that *relatively* low power biomedical devices with good performances can be rapidly implemented on FPGA-based SoC using high-level languages and minimal code optimizations. We have also shown that power supply *agnostic* devices are a valuable option for particular environments.

To reduce the power needed by the device, multiple solutions are possible:

- HW designs targeted for the specific application with reduced area and stripped of all the unnecessary elements.
- HW designs with low-power / reduced area soft processors to substitute the MicroBlaze.
- Communication systems based on already available low-power technologies such as Bluetooth Low Energy (IEEE 802.15.4) or GSM LTE, valuable for outdoor applications.

Regarding the power spectrum computation presented in Section V, the possible candidates for an hardware implementation are *Townsend* [24], *Leroy* [25], and *Press & Rybicki* [26]. Alternative estimators relies on the autoregressive (AR) form of the HRV.

Since many commercial sensors are connected through I2C connection, a service discovery system based on I2C address dictionary will be created.Lastly, to detect the device when is not used, a indoor positioning system based on a ultra low-power wireless node mounted on the board is under development; to minimize power consumption, the node control PS deep sleep functions and de-activate the PL fabric.

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