Rapid Growth of IP Traffic Is Driving Adoption of Silicon Photonics in Data Centers

(Invited Paper)

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Abstract: **With the dramatic growth in consumers using Mobile plus Video data and the corresponding increase in IP traffic, more Data Centers are required together with a need to scale the capacity within the Data Centers. Moore's law continues to push advances in CMOS technology enabling the design of larger higher capacity ASICs used to build Switches and Routers in the Data Centers. The cost, power dissipation and face plate optical density challenges are being solved by Silicon Photonics deployed in smaller form factor pluggable optics with a longer term transition to embedded optics. This march towards higher data rates, lower cost and lower power dissipation requires major advances in the cost, volume wafer manufacturing, optical packaging and test for Silicon Photonics based products. The focus of this talk will be on how Cisco is addressing these multiple development and manufacturing challenges as Silicon Photonics based products are released in the market.**

I. Introduction – Traffic Growth

The combination of more mobile users, more mobile connections, faster mobile speeds combined with more voice, data and video consumption is driving a dramatic need for larger and larger Data Centers to support this growth (Fig 1) [1].

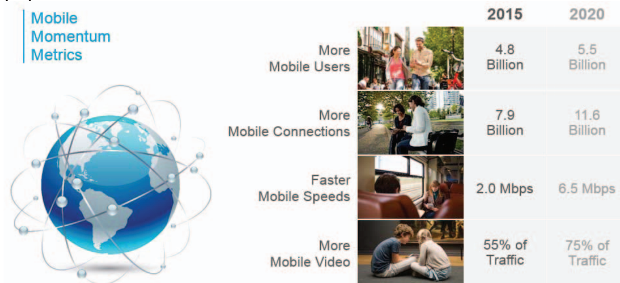

Fig 1: Global Mobile Data Traffic Drivers

The number of mobile users has quintupled since 2000. In 2015, more people had mobile phones than bank accounts, running water, cars, and landlines (Fig 2) [1].

Cisco's Visual Networking Index (VNI) is projecting global IP traffic increase of 3X from 2014 to 2019 (Fig 3) [1]. In the Data Centers, this traffic growth is driving pluggable Optics transitions to higher and higher speeds: 10G → 40G → 100G.

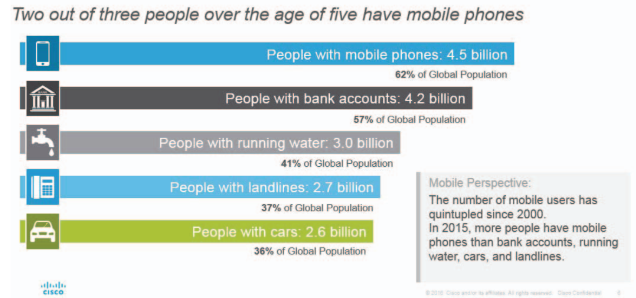

Fig 2: The Pervasiveness of Mobile in 2015

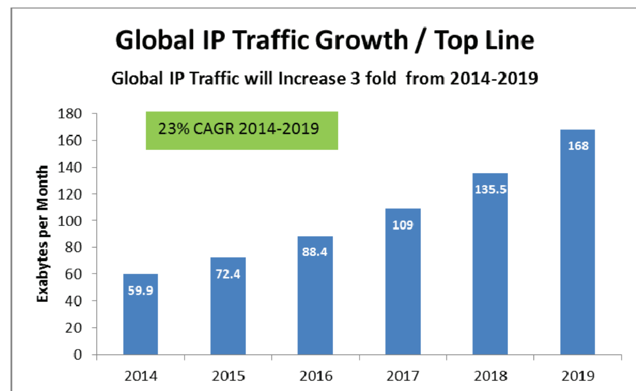

Fig 3: Global IP Traffic Growth

The higher speed ports are driving lower bandwidth cost per Gb/s e.g. $ per Gb/s in Dell O'ro chart is the aggregated cost of port bandwidth in the data switch market shown in Fig 4 [2]. The growth in port volume will continue to drive scale and costs. The cost of bandwidth per Gb is trending to <$1 by 2020. To support this tsunami in traffic growth, highest volume optics deployment will be in the Data Center which is also the most cost sensitive. Another trend in the Data Center is the transition to Single Mode fiber connectivity which is much better aligned to Silicon Photonics capability.

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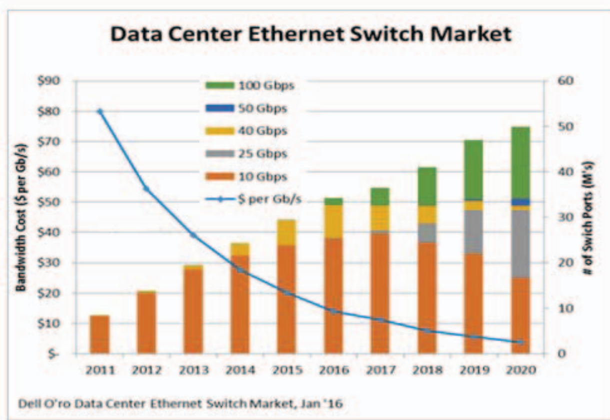

Fig 4: Data Center Bandwidth Cost Trend

The acceleration in traffic growth demands higher port speed as well as higher switch and router bandwidth. Higher SERDES IO and port speeds are being adopted at faster rates to enable efficiencies (Fig 5) [3].

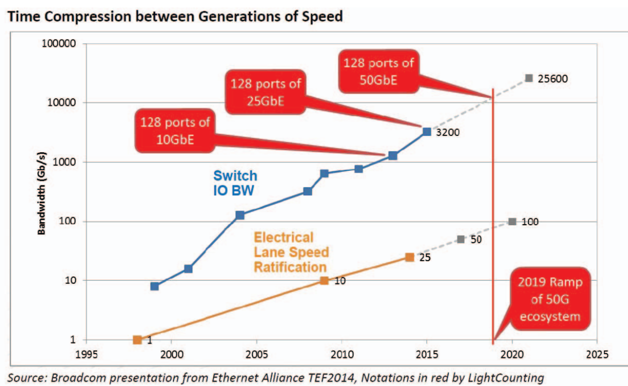

Fig 5: Acceleration in electrical SERDES

To keep pace with electrical SERDES speeds, pluggable optics transition to higher speeds and higher densities is increasing rapidly as shown in Fig 6.

In summary, optical face-plate density must increase to keep up with electrical port bandwidth. Moore's law continues to drive electrical port bandwidth as CMOS scales from: 28nm → 16nm → 7nm. For Optics, pluggable size, power and thermals drive the architecture and design of Data Centers. For example:

- ✓ SFP+ enabled 400G line card in 2008
- ✓ CPAK enabled 1Tb line card in 2013
- ✓ QSFP28 enabled 3.6Tb line card in 2016
- ✓ QSFP-DD will enable >12Tb line card in 2019

With its inherent advantages in the areas of low power dissipation, size and cost, Silicon Photonics has a key role to play here and will drive higher optical density. At some point in the future, it will also enable Embedded Optics to become a reality.

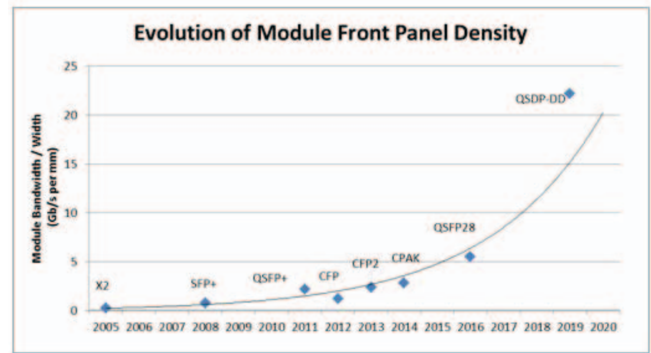

Fig 6: Acceleration in Face Plate Density

II. Cost Drivers for Silicon Photonics

A. Levels of Optical Integration and Packaging

The levels of integration possible for critical optical building blocks is key to lower parts count, performance and cost. Significant progress has been made here and some of the more advanced Optical PDKs provide Modulators, Splitters, Mux/De-Mux functions, Integrated Detectors and Optical Polarization controllers. Fig 7 is an example of a MZI modulator based Silicon Photonics IC with 4 integrated MZIs, Muxes, Splitters and Detectors [4]. This IC is used in Cisco's 100G CPAK IEEE standards compliant LR4 pluggable module currently in volume production. A key and necessary block is the source of photons or laser and the manner in which the photons are coupled both into and out of the waveguides on the Silicon Photonics IC. Fig 7 shows 4 lasers, each a different wavelength, directly attached to the Silicon Photonics die and aligned to the input waveguides for good coupling efficiency. The number of lasers, the alignment cost and coupling efficiency are key cost divers for the overall solution. Availability of heterogeneous integration of III-V material in volume production is expected to reduce the cost of the laser solution. Longer term, epitaxially grown laser technology (QD) with acceptable performance and reliability on the Silicon Photonics platform will drive the cost even lower.

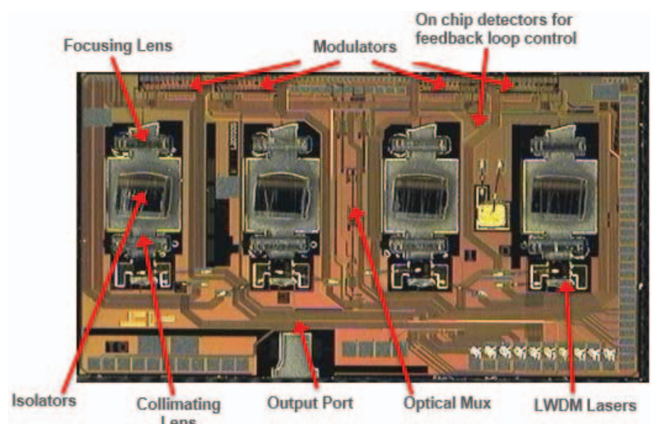

Fig 7: Silicon Photonics IC in CPAK 100G LR4

B. *Fibers, Alignment and Density*

Duplex fiber connectivity offers the lowest cost. Although fiber arrays offer a more dense optical connectivity solution, they are generally higher cost. From an alignment perspective, fiber arrays have an advantage in that you can potentially get multiple channels aligned with fewer active or passive alignment operations. The cost target per alignment needs to be <$1 per alignment to support Data Center cost requirements. Whether you use active or passive alignment does not matter, what counts is your alignment throughput and overall cost per alignment. Higher optical density, higher bandwidth solutions can be achieved by using more lasers (multiple wavelengths) and more parallel fibers or increasingly, with advanced modulation solutions such as PAM4 shown in Fig 8 [5].

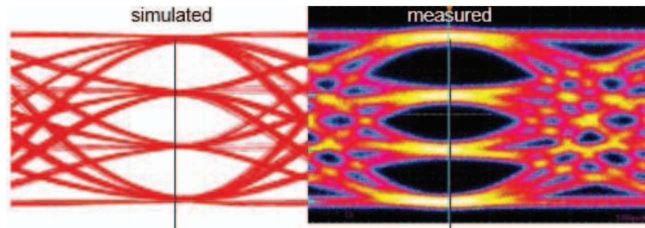

Fig 8: 28GBaud PAM4 eye

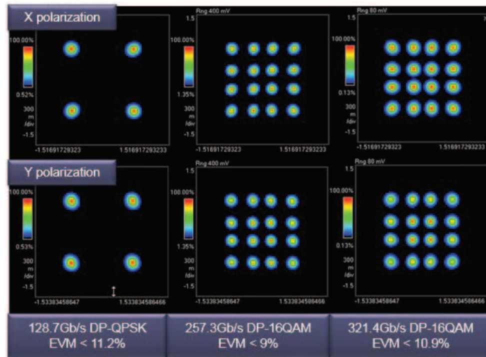

Fig 9: 321.4Gb/s DP-16QAM Demonstration

For even higher data rate longer reach applications, including intra Data Center connectivity, Silicon Photonics is being leveraged together with coherent modulation techniques. Fig 9 shows a 321.4Gb/s DP-16QAM application recently demonstarted by Cisco [6].

C. *Optical Packaging*

For Data Center application, it's challenging to use traditional "gold boxes" for hermetic TOSA and ROSA packaging and meet the aggressive cost requirements. Instead, newer packaging approaches using 2.5D or 3D integration and assembly from the electrical IC world are starting to be used. Fig 10 shows a traditional TOSA approach used for Cisco's 100G CPAK LR4 product [4].

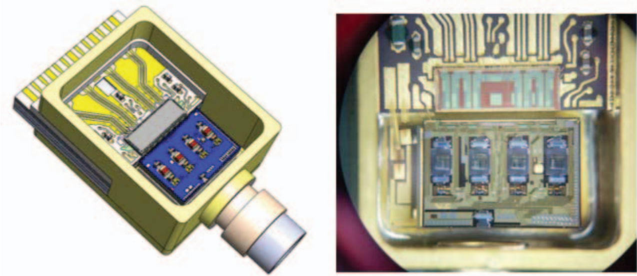

Fig 10: CPAK 100G LR4 TOSA

Fig 11 shows a 2.5D type of packaging platform approach used for Cisco's CPAK 10x10G LR family of products. With all these approaches, fiber alignment on the packaging platform is critical depending on the use of duplex fiber or a fiber array. In addition, based on the application, the type of laser and the requirement for cooling needs to be factored into the packaging choice.

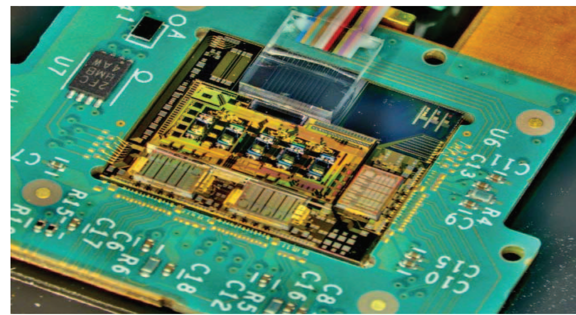

Fig 11: CPAK 10x10 LR Packaging Platform

For higher data rates and higher performance product requirements, flip chip assembly is also getting increasingly used. Fig 12 shows a driver flip chip attached to the Silicon Photonics IC for a Cisco coherent product [6].

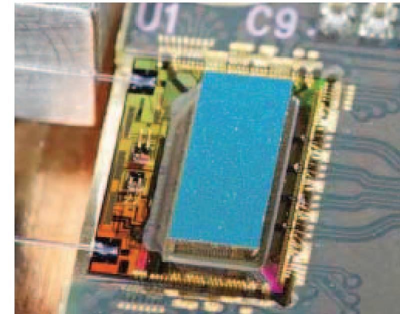

Fig 12: Flip chip assembly of Electrical driver and Silicon Photonic IC

To address the dual requirements of lower power dissipation and higher data rates, the electrical-to-optical interface (E-to-O) needs to move closer to the ASIC on the line card. This trend will require co-packaging of the E-to-O function with the ASIC and parallel electrical I/O on an interposer.

Overall, to meet Data Center objectives of high volume, low cost, power and overall performance, the developers of optical connectivity solutions are increasingly adopting IC industry

packaging approaches for Silicon Photonics. These electrical packaging approaches need to be modified to address some unique attach and alignment (coupling) challenges with respect to the optical interface for laser as well as fibers.

D. *Volume Wafer Manufacturing*

Availability of cost effective volume wafer manufacturing capacity is critical to the long term success of Silicon Photonics. To achieve this, Silicon Photonics designs and process technology platforms must leverage the available CMOS IC industry infrastructure. Increasingly, 300mm CMOS fabs are being used to process Silicon Photonics wafers. Wafer pricing, yields, fab cycle times have to be based on the "CMOS model". Aside from the benefits of a CMOS cost model in these fabs, the 300mm processes have significantly improved lithography resulting in higher performance for the Optical PDK building blocks. Longer term, these CMOS based processes will need to support fully "integrated" lasers as part of the overall Silicon Photonics platform.

E. *Wafer Level Assembly and Test*

As mentioned earlier, a significant cost driver for Silicon Photonics based products is the cost of assembly and test. To address assembly cost, wafer level assembly of optical components such as lasers (Fig 13) and wafer level burn-in is starting to be used.

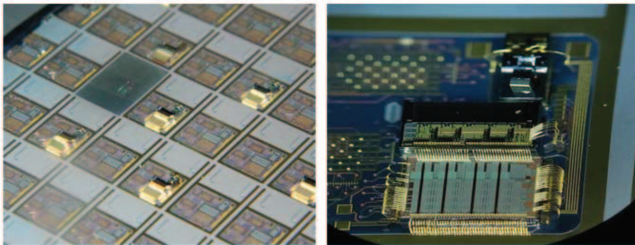

Fig 13: Wafer Level Assembly

Overall product related testing for specification compliance is also a very significant cost contributor. Wafer probers with electro-optic test capability are increasingly being deployed to fully test the Silicon Photonics ICs at the wafer level.

III. SUMMARY

Cisco's Silicon Photonics platform is fully qualified meeting Carrier class performance and reliability requirements. This platform has been used to develop a range of CPAK 100G IEEE standards compliant products which are currently in volume production. In order to meet the overall cost and performance requirements for Data Center optical connectivity, Silicon Photonics must leverage the IC industry "CMOS model" and other infrastructure including 2.5D and 3D packaging adapted for the laser and fiber optical interfaces.

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