Energy-Performance Optimized Design of Silicon Photonic Interconnection Networks for High-Performance Computing

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***Abstract*— We present detailed electrical and optical models of the elements that comprise a WDM silicon photonic link. The electronics is assumed to be based on 65 nm CMOS node and the optical modulators and demultiplexers are based on microring resonators. The goal of this study is to analyze the energy consumption and scalability of the link by finding the right combination of (number of channels × data rate per channel) that fully covers the available optical power budget. Based on the set of empirical and analytical models presented in this work, a maximum capacity of 0.75 Tbps can be envisioned for a point-to-point link with an energy consumption of 1.9 pJ/bit. Sub-pJ/bit energy consumption is also predicted for aggregated bitrates up to 0.35 Tbps.**

I. Introduction

AS THE YEAR 2020 approaches, performance scaling of computing systems is increasingly threatened by energy consumption, and more precisely, by the energy consumption associated with data-movement. Smaller CMOS feature size allows a reduction of the energy required to perform logical operations, but is of lesser help to reduce expenses related to data movement. To send data over distance, one must fight against the loss and the limited bandwidth of the wire. For example coaxial cables are limited to a bandwidth on the order of 10-60 GHz. Therefore every signal propagated over an electrical wire needs to be reshaped and retimed after short distances if the signal exceeds a few Gbps. In the case of integrated circuits, bandwidth and loss limiting factors are only marginally affected by finer lithographical means, unless a new paradigm in data movement is adopted and data is sent using optical frequencies. Optics eliminates a key obstacle to energy efficiency of data movement, since at such frequencies only the end detector must be electrically charged/discharged [1].

Optical communication technology has been leveraged in the last decade to progressively connect continents, countries, cities, boroughs and buildings with optical fibers. The attenuation of a modern standard single-mode fiber (SSMF) can be as low as 0.2 dB/km [2], resulting in much longer reaches. Another advantage resides in the very large bandwidth available over the optical fiber. The range of frequencies at which fibers are nearly transparent provides a total bandwidth clearly in excess of tens of THz, thus enabling communication on the order of Terabit/s.

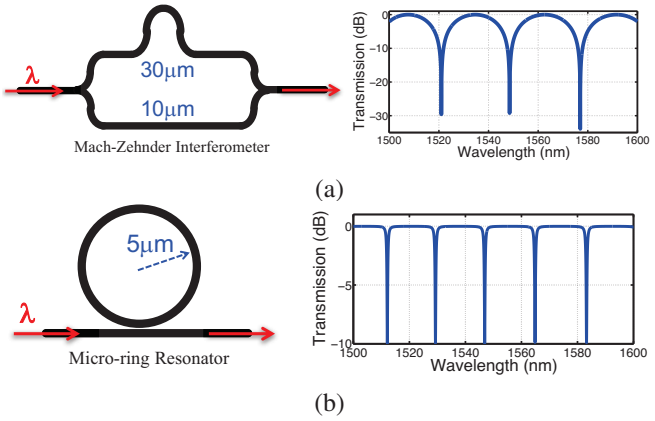

Fig. 1. Schematic of a Mach-Zehnder interferometer based on silicon waveguides (450 nm × 220 nm cross-section) and its corresponding wavelength response. The 3dB bandwidth of each dip is about 9.35 nm. (b) Schematic of a microring resonator with 5μm radius and its corresponding wavelength response. The 3dB bandwidth of each resonance is about 0.5 nm.

Terabit-bandwidth capable optical fibers are being installed to our houses and offices, but will also be deployed inside our computers eventually. Deployment of optical fibers in High-performance computing (HPC) platforms, which heavily rely on parallel computing and thus are in high need of interconnection bandwidth, has already begun. However, HPC systems will draw much larger benefits out of photonics if the cost of optical interfaces, defined hereafter as transceivers, is progressively reduced over time [3].

Until today, costs of photonic equipment was significant in part because optical transceivers have relied to a large extent on direct bandgap III-V semiconductor compounds such as indium phosphide or gallium arsenide, along with their specific fabrication techniques. The smaller market offered to these III-V components prevented the development cost to be amortized as extensively as the ones invested in silicon based semiconductor industry. Luckily, the situation is changing with the emergence of silicon photonics. Historically, silicon is not the first choice material for optoelectronics, mostly due to the difficulty to emit light (due to the indirect bandgap structure, electron-hole pair recombination in a silicon diode must be assisted by a phonon to be radiative which causes light emission in silicon to be an inefficient

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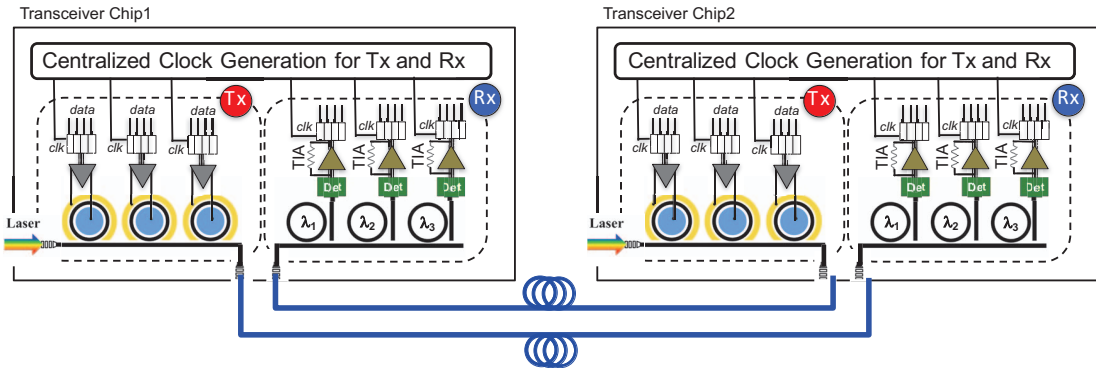


Fig. 2. Schematic of a full-duplex chip-to-chip optical interconnect based on silicon photonics. Each is equipped with an optical transceiver interface that can support wavelength-division-multiplexing (WDM) optical signaling. The receiver includes wavelength selective filters for demultiplexing.

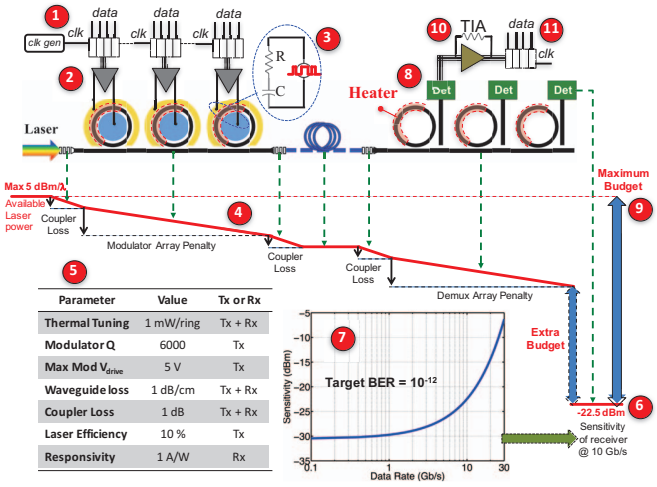
process). However, silicon-based optical components benefit from a high refractive index contrast between silicon and silica or air, allowing micron/submicron-scale light guiding structures. These structures can in turn be arranged to obtain interferences or resonances at particular wavelengths. Fig. 1(a) shows the wavelength response on the output port of a Mach-Zehnder interferometer when its input port is excited, while Fig. 1(b) illustrates the wavelength response of a ring resonator. Refractive index of silicon can also be precisely modified by changing the concentration of charge carriers [4]. Moreover, because changing this index takes no longer than tens of picoseconds, fast optical modulations ($>$ 10 Gb/s) can be realized with silicon-based devices.

The key enabler for silicon photonics, however, has been the capability to etch the micro-scale structures with enough precision through slightly adapted [5] or unmodified silicon CMOS processes [6]. Benefiting both from decades of industry investment, and from an installed electronics design automation (EDA) and fabrication environment, silicon photonics offers the possibility to drastically reduce the costs of optical transceivers. In addition, transceivers are far easier to integrate along with conventional electronics if they share the same substrate and material [7]. Silicon photonics thus also allows us to foresee deeply integrated optical transceivers in the future.

At the time this paper is being written, silicon photonics is clearly industrially and commercially emerging. After several "early bird" products targeted for the telecom market, silicon photonics-based transceivers are being introduced in supercomputers (HPC) and are about to be massively adopted for datacenters as their cost-per-provided-bandwidth will soon reach $\sim$\$1/Gbps [8]. Progresses toward full integration of optical transceivers with compute elements are also being realized [7].

In order to optimally exploit the benefits of this emerging technology in computing systems, a precise understanding of their main engineering trade-offs is required. Hence, the design of silicon photonic point-to-point links is a multi-facetted problem demanding several balanced design choices.

As it is hard to directly exploit the THz-order optical bandwidth available, optical links generally use optical wavelength division multiplexed (WDM) signaling which consists of optically combining multiple optical channels, each modulated



Parameter	Value	Tx or Rx
Thermal Tuning	1 mW/ring	Tx + Rx
Modulator Q	6000	Tx
Max Mod V_{drive}	5 V	Tx
Waveguide loss	1 dB/cm	Tx + Rx
Coupler Loss	1 dB	Tx + Rx
Laser Efficiency	10 %	Tx
Responsivity	1 A/W	Rx

Fig. 3. Schematic of a unidirectional silicon photonic link. (1) Clock generation and serialization. (2) High-speed drivers. (3) RC representation of optical modulator and thermal tuning. (4) Evolution of optical power budget along the link. (5) Key assumptions for optical devices. (6) Optical sensitivity level of the receiver. (7) Our sensitivity model as a function of data rate for 65 nm CMOS node. (8) Microring demultiplexing array with thermal tuning followed by photodetectors. (9) Maximum available optical power budget. (10) Transimpedance amplifier frontend of the receiver. (11) Deserialization of the electrical data.

at a rate compatible with high-speed electrical drivers and optical modulators, to achieve a high aggregated throughput within a single fiber. As we will further illustrate in this paper, a typical design trade-off is the choice of the number of optical channels packed together as WDM signaling in conjunction with the channel bitrate to employ [9]. More channels modulated at higher bitrates are of course desirable. High bitrate signals, however, are more sensitive to distortions resulting from imperfect modulators and filters, and are also more energy consuming. On the other hand, multiplying endlessly the number of channels eventually obliges to reduce the frequency guard-bands present between adjacent channels which can lead to severe optical crosstalk phenomena [10]. A good knowledge of the link's elements is required to balance these two limitations and locate the sweet-spot leading to minimal energy consumption or maximal scalability.

In this paper, we aim to clearly introduce the main factors determining the scalability and energy consumption of photonic links. For this purpose, we present and summarize our recent work on silicon photonic modeling [9]–[12]. We employ

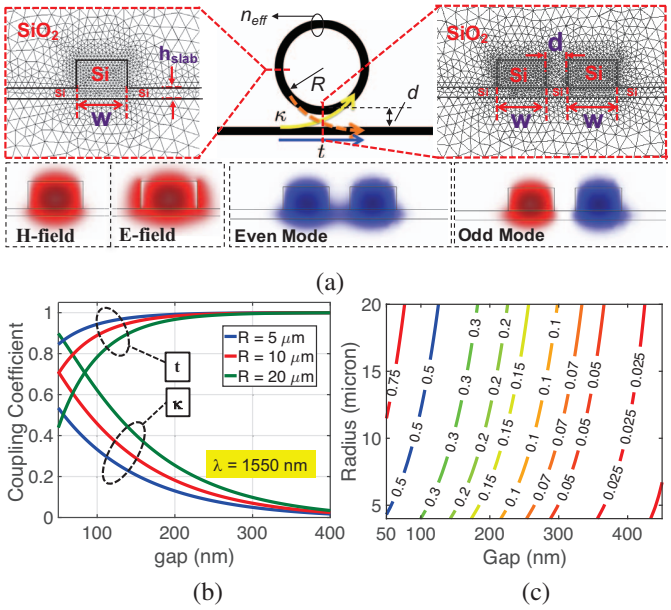


Fig. 4. (a) Schematic of a ring-waveguide structure with only one coupling waveguide. The cross-section of single rib and coupled rib waveguides and the mode profiles from COMSOL are also shown. The rib waveguides are 450nm × 220 nm with 100 nm slab. (b) Coupling coefficients (κ and t) as a function of coupling gap at 1550nm with three different radii calculated from our compact modeling approach. (c) Contours of κ for various gap sizes and radii at 1550nm. A smaller gap size and larger radius result in a stronger coupling between the ring and the waveguide.

our models to analyze how the power consumption of the various link elements is affected by the bitrate, under different set of assumptions and constraints taken on device capabilities. We present, for each bitrate, the number of channels that maximizes the total link bandwidth (in units of Tbps) and evaluate the energy consumption (in units of pJ/bit) associated with that link.

The general link model used throughout this study is presented in Section II. The section details one by one the models of the optical impairments present along the link and models expressing the energy consumption of the various link components. Section III presents the results of this study and section IV presents the conclusions.

II. Chip-to-chip Optical Interconnect

In this section, we present details of modeling a point-to-point link based on silicon photonic elements. Microring resonators are selected as the enabling optical devices for modulation at the transmitter side and demultiplexing at the receiver side due to their small area footprint.

A photonic interconnect enables transmission and reception of high density (Tb/s) optical data streams. Fig. 2 shows a general scheme of a uni-directional point-to-point link established between two transceivers. Two such links are combined simultaneously to obtain full-duplex capability. No additional clock-data recovery (CDR) mechanism is considered inside the Rx unit in our analysis. It is assumed that clock generators located in the two transceivers are either fed by a common, closely located centralized clock, or synchronized via a clock forwarding mechanism, with one of the WDM channels dedicated to clock [13]. Fig. 3 provides more details of the Tx-Rx elements. The individual models for capturing the optical and electrical behavior of the link are described as follows:

A. Laser Source and Consumption

The laser source is assumed to be located off-chip and injected into the transmitter. An application of a silicon photonic WDM transceiver with a comb laser source has been recently demonstrated by HP Labs [14]. We assume a comb laser source providing any desirable number of lines while maintaining the same wall-plug efficiency of about 10% per each line (flat efficiency model). In practice, a single comb laser source will likely be limited to around 40 channels, but multiple comb sources can be combined. Due to the optical nonlinearities of a microring modulator [15], the maximum optical power per each line of the comb laser is kept to 5 dBm (3.16 mW) in our analysis. Due to the nonlinearities of silicon material, the total output power of the laser that can be coupled into the transmitter is kept at 20 dBm (100mW).

In order to estimate the minimal amount of power required by the link to achieve error-free operation, the link optical power budget must be evaluated. For this aim, the optical power penalties [9] associated with each optical operation must be obtained. A description of these power penalties is proposed in the following sub-sections B to E.

B. Vertical Grating Couplers

Coupling of the comb laser into the transceiver chip is assumed to be based on vertical grating couplers. Grating couplers with more than 75% coupling efficiency (∼1.2 dB loss) and 78 nm bandwidth around 1310 nm optical wavelength have been demonstrated in 2015 [16]. A recent work [17] has demonstrated silicon-based grating couplers with 4 dB coupling loss at 1550nm and a 1dB bandwidth of 40 nm. We envision in our analysis, a coupling loss of 1 dB and 50 nm of bandwidth for the grating coupler at 1550 nm wavelength.

C. Silicon Waveguides

We assume rectangular silicon waveguides with a cross-section of 450 nm × 220 nm can be fabricated. Typically, the width of the waveguide is kept below 600 nm to ensure single mode operation. In order to accurately capture the dispersive behavior of the optical mode inside the waveguide (effective index, $n_{\text{eff}}(\lambda)$), we performed a mode analysis in COMSOL over the range of 1500nm-1600nm and imported the results into our modeling environment [11] (n_{eff} = 2.36 at 1550nm). The propagation loss of the silicon waveguides is largely due to the roughness of the sidewalls, resulting in scattering of the light. Wider waveguides have shown to be less affected by sidewall roughness. In our analysis, we consider 1 dB/cm propagation loss for the straight waveguides. The loss for the curved waveguides that build the ring structures, however, is in general dependent on the radius of the curvature. Bending losses have been recently characterized by Jayatilleka et al. [18]. Based on these results, we proposed to express bending loss as a function of radius with a power law equation

$$Loss_{dB/cm} = a \times (R_{\mu m})^{-b} + c \qquad (1)$$

with a = 1.09×10^{9}, b = 10.15, and c = 1 dB/cm [12]. We utilize this model to perform various optimizations on the loss and quality factor of the ring resonators [9].

D. Microring Modulators

Putting a ring resonator in the proximity of a straight waveguide causes the light to couple into the ring and out of it. The structure is shown in Fig. 4(a) along with the finite-element modal analysis from COMSOL. The coupling between a ring and a waveguide is modeled by the coupling coefficients t (through coupling) and κ (cross-coupling) as explained by Yariv [19] ($t^2 + \kappa^2 = 1$). In order to accurately capture the dependence of these coupling coefficients on the radius, on the gap separating the ring from the straight waveguide, and on the wavelength, we discretize the non-uniform coupling region and assume a uniform coupling for each segment. The results are shown in Fig. 4(b) as a function of gap, while Fig. 4(c) provides the contours of κ for a wide range of radii and coupling gaps. The periodic transmission spectrum of the structure is given by

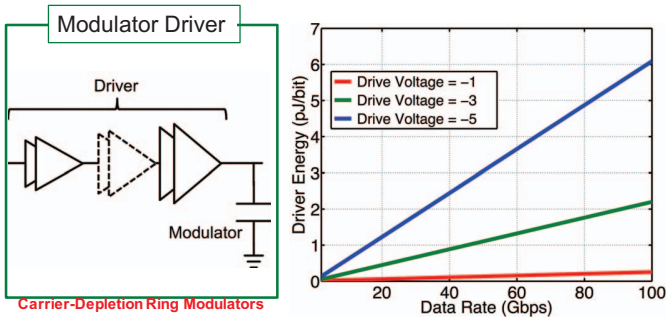
$$TR = \left| \frac{t - \sqrt{L}\exp(-j\delta\phi)}{1 - t\sqrt{L}\exp(-j\delta\phi)} \right|^2 \quad (2)$$

where L is the round-trip optical power loss inside the ring, t is the through coefficient of the coupling region, and $\delta\phi$ is the relative round-trip phase shift with respect to the target resonance $\delta\phi = -2\pi \times \delta\lambda / FSR_{nm}$ and $\delta\lambda = \lambda - \lambda_{res}$. FSR is the free-spectral range of the resonance spectrum approximated as $FSR_{nm} = \lambda^2_{res(nm)}/(2\pi R_{nm} \times n_g)$ where n_g = 4.2. Finally, the half-power bandwidth (full width at half maximum or the 3dB bandwidth) of each resonance is given by $\Delta\lambda_{3dB} = FSR_{nm} \times 1/\pi \times \cos^{-1}(1-(1-t\times\sqrt{L})^2/(2t\times\sqrt{L}))$ and the quality factor of the resonance is defined as $Q = \lambda_{res}/\Delta\lambda_{3dB}$.

In order to perform on-off-keying (OOK) modulation on an optical carrier at λ_0, the resonance is initially tuned to λ_0 and then the spectral response is shifted leveraging the electro-optical effect of free-carrier dispersion. This is the only mechanism in Silicon fast enough to enable high-speed electro-optic modulation (10 Gb/s and beyond). Free-carrier dispersion is triggered and controlled by placing a PN region (carrier depletion type) with typical doping levels on the order of 10^{17} – 10^{18} /cm^3 around the modulating structure. We use the empirical Soref's equations [20] that govern the change of index and loss of silicon as a function of change in carrier density in conjunction with the modeling presented in [13]. Based on the driving voltage of the modulator, the change in phase shift ($\delta\phi$) and round-trip loss inside the ring (L) and 3dB bandwidth ($\Delta\lambda_{3dB}$) is calculated and the quality of the optical modulation in terms of the optical power penalty of modulator is evaluated. More details of power penalty analysis of an array of microring modulators are presented in [9].

E. Optical Demultiplexing

A wavelength demultiplexer is required at the receiver to isolate the various individual channels of the WDM signal. Structures that are wavelength selective such as arrayed-waveguide grating (AWG) or microring resonators are typical candidates. Since AWGs usually occupy a large footprint, we assume demultiplexing based on ring resonators as shown in Fig. 2 and marked by (8) in Fig. 3. For each individual channel, we optimize the ring such that the power penalty associated with the whole demultiplexer array is minimized [10]. The power penalty imposed on each channel consists of three parts: a) The insertion loss of the ring - independent of the number of channels and their data rate. b) The truncation effect - only dependent on the data rate; strong truncation arises when the bandwidth dropped by a ring is small compared to the signal bandwidth (a mathematical description of the distortions can be found in Reference [9]). c) Optical crosstalk due to the imperfect suppression of adjacent channels - both number of channels and data rate dependent. In our recent work [10], we mathematically and experimentally investigated the optical power penalty due to inter-channel and intra-channel crosstalks. For the WDM receiver architecture considered in this paper, only inter-channel crosstalk in taken into account.



(a) (b)

Fig. 5. (a) Schematic of the high-speed driver with the capacitive load of the optical modulator. (b) Plots of our model for the energy consumption of the high-speed driver as a function of data rate and driving voltage in 65 nm CMOS node.

F. High-speed Drivers

The high-speed driver provides fast and large output voltage swing to charge and discharge the optical modulator, assumed here to be a ring modulator operated through carrier depletion mechanism. This is marked by (2) on Fig. 3. The driver architecture is based on cascaded amplifier and buffer stages as shown in Fig. 5(a). The model for the energy consumption of the driver is from the design presented in [21] and is adapted to various capacitive loads and drive voltages based on the following linear equation:

$$E \approx \text{slope} \times DR + \text{constant} \quad (3)$$

where E is the energy consumption in J/bit unit and DR is data rate in bits/sec unit. The slope and constant factors are calculated as

$$\text{slope} = 1.4 \times 10^{-23} \times \left(\frac{V_{mod}}{2V_{DD}}\right)^2 \times \left(\frac{C_{mod}}{C_{ref}}\right) \quad (4a)$$

$$\text{constant} = 8.4 \times 10^{-14} + \frac{1}{4}\left(C_{mod}V_{mod}^2 - C_{ref}(2V_{DD})^2\right) \quad (4b)$$

where V_{DD} = 1.2 V is the supply voltage in 65 nm CMOS, V_{mod} is the peak-to-peak driving voltage applied to the optical modulator, C_{mod} is the equivalent capacitive load of the modulator, and C_{ref} = 50 fF is a reference capacitor that has been used in the simulations of the driver. A plot of Eq. (3)

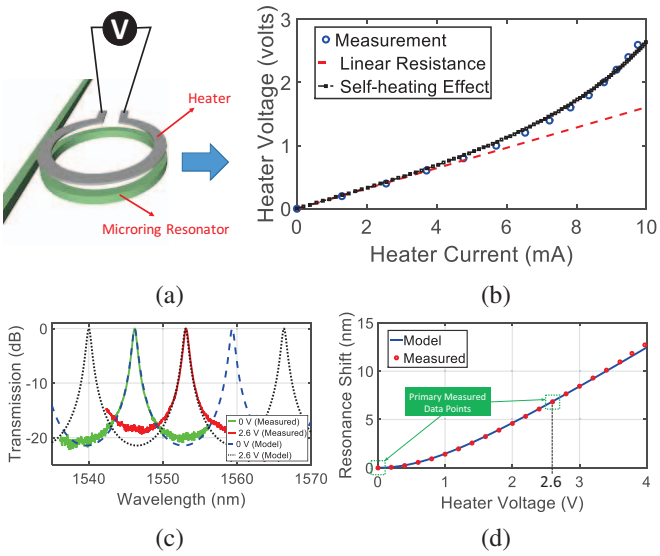


Fig. 6. Accurate modeling of the thermo-optic behavior of microring resonators. (a) Schematic of a microring with integrated metallic heater. (b) Measured data for the V-I response of an integrated micro-heater. (c) Experimental measurement of the thermo-optic response of a ring resonator. (d) Shift of resonance over a full FSR of the ring as a function of heater voltage.

is presented in Fig. 5(b) for C_{mod} = 50 fF and three drive swings.

G. Thermal Tuning of Microring Resonators

Microring resonators are sensitive to thermal changes since the refractive index of silicon changes with temperature. Temperature in the immediate neighborhood of a ring must therefore be controlled with a micro-heater. The schematic of a ring resonator with a micro-heater situated above the ring is shown in Fig. 6(a). By applying a voltage to the heater and running electrical current through it, ohmic power is dissipated and temperature rises. The shift of resonance is related to the change of temperature by the following equation:

$$\Delta\lambda_{res(nm)} = \left(\frac{2\pi R_{nm}}{\lambda_{res(nm)}}\Gamma\frac{dn_{si}}{dT}\Delta T_{ring}(V)\right) FSR_{nm} \quad (5)$$

where ΔT_{ring} is the change in ring's temperature, Γ is the confinement of the optical mode inside the ring and $dn_{si}/dT \approx 1.86\times10^{-4}$ /K is the thermo-optic coefficient of silicon. The change in ring's temperature as a function of heater voltage depends on the nonlinear V-I response of the heater. Fig. 6(b) shows our experimental measured V-I data points (blue circles) along with an expected linear V-I curve (dashed red line). In the first-order approximation, the change in the temperature of the heater is linearly related to the ohmic power dissipated by the heater. This leads to the following nonlinear V-I characteristic:

$$I(V) = \frac{V}{R_{linear}} \times \frac{2}{1+\sqrt{1+K_v V^2}} \quad (6)$$

where R_{linear} is the slope of the dashed red line in Fig. 6(b). We define K_v as the self-heating coefficient of the heater. This equation can be almost perfectly fitted to the measured V-I data in Fig. 6(b) if K_v is set appropriately. As shown in Fig. 6(c), we measured the spectral response of a ring for heater voltages 0 volt (green curve) and 2.6 volt (red curve) and observed a 6.84 nm red-shift in the resonance. These two measurements were enough to extract all the necessary parameters. The blue curve in Fig. 6(d) represents our model for the ring–heater system which almost perfectly matches our measurements.

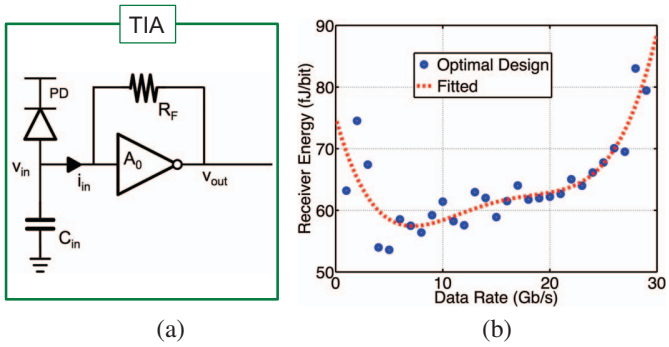


Fig. 7. (a) Schematic of a photodiode followed by a transimpedance amplifier (TIA). (b) Optimal energy design points of the TIA as a function of data rate at the optical sensitivity level of the receiver.

H. Photodiode and Transimpedance Amplifier

The job of the photodiode is to convert the optical power into electrical current (characterized as the responsivity parameter). In other words, the photodiode takes in the optically modulated data and removes the optical carrier (direct down conversion). Typically based on Germanium, two types of photodiodes are predominantly used in silicon photonics: a) PIN photodiodes with a large intrinsic region, and, b) Avalanche photodiodes (APD) that can also provide internal amplification of the current through an avalanche process, at the expense of additional quantum noise [22]. In this analysis, we assume a simple PIN photodiode with a responsivity of 1 A/W and a speed in excess of 45 GHz [23].

The transimpedance amplifier (TIA) is the electrical frontend of the receiver. As shown in Fig. 7(a), the feedback resistance, R_f, converts the generated photocurrent into a voltage that is fed into the decision circuitry to lift the signal from a small analog voltage to a full digital signal. We model the consumption and capability of the TIA using a database of various designs in 65 nm CMOS [24]. The design that for a given bit-rate and photocurrent (received from the diode) leads to the lowest power consumption is selected. For example, the data points in Fig. 7(b) indicate the energy consumption of the TIA at the sensitivity level of the receiver. A plot of the sensitivity values (in dBm) as a function of data rate is marked by (7) in Fig. 3.

III. Analysis of the Optical Link

Based on all the electrical and optical models provided in the previous section, we perform an analysis of the performance of the silicon photonic link. The objective of this analysis is to find the right combination of N_λ (number of channels) and DR (optical rate of each channel). We start by looking for the $N_\lambda \times DR$ product leading to the minimal energy consumption for a given optical aggregation rate for the link. Fig. 8(a) shows the minimal energy for 200 Gbps to 800 Gbps aggregation based on the optimization of the radius

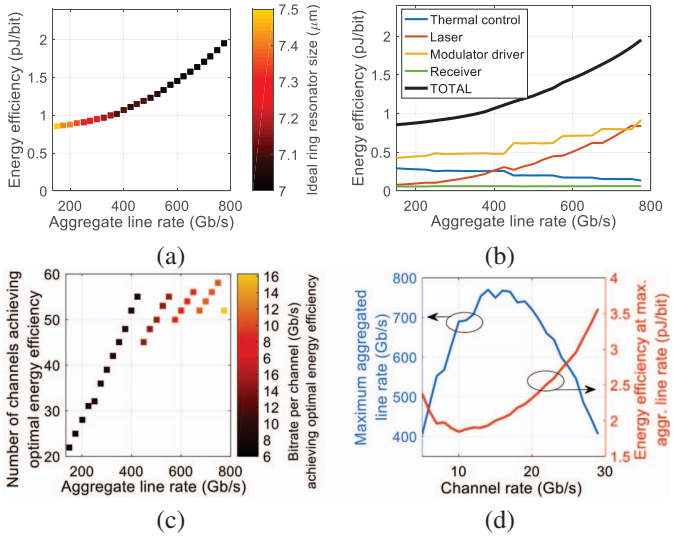


Fig. 8. (a) Minimum energy consumption of the link for given aggregations based on optimum value for the ring radius. (b) Breakdown of energy consumption. (c) Breakdown of the number of channels and the required data rate per channels for minimum energy consumption. (d) Evaluation of the maximum supported aggregation and the associated energy consumption for various channel rates.

and gaps of the rings. The rings are always set to their critical coupling operation point [12], [19]. This chart shows that ring radius of about 7μm leads to the best energy performance of the link. The breakdown of the energy numbers are plotted in Fig. 8(b) indicating that the laser consumption becomes critical at higher data rates while the static thermal tuning has a declining trend. Finally, Fig. 8(c) provides details of the number of channels and the required data rate per channel that lead to the minimal energy consumption for the target aggregation.

Next, the product leading to the maximal aggregation is investigated. Here, we simply sweep the optical data rate of each channel and increase the number of channels until the available optical power budget is fully utilized. Fig. 8(d) plots the results indicating a maximum possible aggregation of about 800 Gbps at 15 Gbps channel rate. The energy consumption associated with each case is also plotted. Note that the minimum point of the energy curve is not at the maximum point of the aggregation curve. This further reiterates the fact that designing a silicon photonic link requires certain electrical and optical tradeoffs.

We note that the results shown here differ substantially from the ones reported in our previous publications (maximal aggregation rate of 2.1 Tb/s in [9], 1.9 Tb/s in [25]). In these studies, low-loss ring resonators of small diameter were assumed realizable [26], whereas in the present work, we specifically evaluate the loss of the rings as function of the diameter using the model detailed in [12]. This also reveals how widely the maximum aggregation rate depends on the capability of making low loss rings, thus on fabrication capabilities.

IV. Conclusions

We presented a detailed discussion on the modeling of silicon photonic point-to-point links. Overall, this discussion underlines the fact that the design of silicon photonic links is subject to a variety of constraints and trade-offs. Designing silicon photonic links, and by extension, networks, requires a collection of tools and models, not only to attain optimal performance, but simply to guarantee error-free operation.

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