Three-Terminal MTJ-Based Nonvolatile Logic Circuits with Self-Terminated Writing Mechanism for Ultra-Low-Power VLSI Processor

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Abstract—**Magnetic-Tunnel Junction (MTJ)-based nonvolatile logic circuits have some possibility to solve the power-dissipation problem seriously focusing on the present CMOS-only-based VLSI processors. Three terminal MTJ devices are the promising candidate as nonvolatile storage device to realize such a nonvolatile logic circuit. However, its writing energy is still serious in comparison with conventional CMOS-only-based logic circuits. In this paper, a new MTJ-based nonvolatile logic circuit with self-terminated mechanism is proposed and its energy efficiency is evaluated in comparison with the corresponding previous work. In addition, some recent research topics related to MTJ-based nonvolatile logic-circuit design and its application, such as a computer-aided-design (CAD) tool considering a stochastic MTJ-switching behavior and the application to a resilient "die-hard" VLSI processor against sudden power-supply outage, are also demonstrated.**

I. INTRODUCTION

In the Internet of Everything (IoE) era, it is strongly necessary to establish ultra-low-power VLSI architecture, while still increasing high-performance processing power. In the present CMOS-only-based VLSI, however, there are several serious problems such as communication bottleneck between memory and logic modules inside a VLSI chip, increasing power dissipation, especially standby power dissipation, and device-characteristic variation effect. On the other hand, several emerging storage devices are getting developed to overcome the weak points of ordinary semiconductor memories; dynamic random-access memory (DRAM) and static random-access memory (SRAM). Especially, magneto-resistive random-access memory (MRAM) that has already undergone a few incarnations, is now converging on a scheme for upending the memory business. Spin-transfer torque (STT) MRAM promises speed and reliability comparable to that of SRAM, where SRAM is the quick-access memory embedded inside microprocessors, along with the "non-volatility" of flash, the storage of smartphones and other portables [1-2]. Since magnetic tunnel junction (MTJ) device, the key element of MRAM, is easily distributed over a logic-circuit plane by using a three-dimensional (3D) stack structure as shown in Fig. 1, performance degradation due to intra-chip global wires could be drastically mitigated, which could be lead to a high-performance, ultra-low-power and highly reliable (or highly resilient such as "die-hard"-like) logic LSIs [3-5].

One of the most useful methods to cut off leakage power is to use power gating. If the power gating is applied in the conventional CMOS-only-based logic LSI, a part of standby power can be surely eliminated, but two additional operations, "back-up" and "boost-up" procedures, must be additionally applied before and after utilizing the power gating, respectively, which may discourage to apply the power-gating technique. In contrast, the use of nonvolatile devices as storage elements maximizes the outcome of power-saving using the power-gating technique. Since a judicious combination between nonvolatile devices and power-gating technique has been naturally realized in the MTJ-based nonvolatile VLSI-processor architecture, it is truly expected that the wasted power dissipation could be ideally eliminated.

In order to accelerate the implementation of nonvolatile logic LSIs, you must make efforts to develop key technologies in every LSI-design hierarchy from device/material level to system-architecture/application level. In the following section, some concrete efforts to develop nonvolatile logic LSIs are demonstrated. First, a self-termination technique is introduced to minimize the write energy of 3-terminal MTJs as well as to verify its write operation [6-9]. In addition, two more recent research topics related to MTJ-based nonvolatile logic-circuit design and its application, such as a computer-aided-design (CAD) tool considering a stochastic MTJ-switching behavior [10-12] and the application to a resilient "die-hard" VLSI processor against sudden power-supply outage [13-16], are also demonstrated.

II. DESIGN OF A 3-TERMINAL MTJ-BASED FLIP-FLOP WITH SELF-TERMINATED WRITE MECHANISM

A nonvolatile flip-flop (NV-FF) is an essential component for the nonvolatile logic LSI since temporal data of each function block must be clock-synchronized, backed up before power-off, and recalled just after power-on. An MTJ device is the best candidate to implement the NV-FF owing to its virtually unlimited endurance, CMOS compatibility, and 3-dimensional stacking capability. While various types of MTJ-based NV-FFs have been proposed, there are important issues for the MTJ-based NV-FF design. The first issue is the stochastic nature in MTJ switching. Even in the same MTJ device, the actual time to complete the write operation varies dramatically. Therefore, a longer time write current pulse is

required for the reliable write operation than that of average one, which results in a large amount of energy consumption. The large amount write energy consumption is critical for the backup operation because temporal data in each NV-FF must be stored into the MTJ device before power-off. Thus, the time during which the energy saved by the power-gating technique equals to the energy lost by the backup/recall operations (referred as break-even time), becomes long. As a result, fine-grained power-gating technique cannot be applicable and the potential of nonvolatile logic LSI is not fully utilized. To overcome this issue, a self-terminated NV-FF, which makes it possible to minimize write energy for the MTJ device by monitoring the voltage change in MTJ switching and terminating write current, has been reported [6-9]. In particular, a 3-terminal MTJ (3T-MTJ) device is focused on to realize high-speed nonvolatile memories and high-performance logic gates. Since the write current path is separated from the read current path in the 3T-MTJ device, both a sense circuit for reading MTJ resistance and a write driver for applying write current can be individually optimized.

Figure 2(a) shows the schematic diagram of the self-terminated NV-FF, which is composed of a master latch, a slave latch, a write driver, a nonvolatile storage cell, and a self-termination circuit, and Figure 2(b) shows the comparison of nonvolatile storage cells using the 2T-MTJ device and the 3T-MTJ device. In case of 3T-MTJ-based nonvolatile storage cell, the read-operation path is separated from the write-operation path, which makes it possible to relax design space exploration.

Figure 3 shows the basic behavior of the self-terminated NV-FF. Three times of backup operation (denoted as *BCK*) are performed just after each basic operation (denoted as *OP*). In the first backup operation, $Nq=0$ is stored into the MTJ device as *M*. After the MTJ switching, both *DONE* and *STR* quickly become high and low, respectively. Then, the write current I_{WR} is terminated. In the second backup operation, $Nq=1$ is stored into the MTJ device in the similar manner. In the third backup operation, in contrast, I_{WR} is skipped because both *Nq* and *M* are '1' and the backup operation is skipped.

Figure 4(a) shows the comparison of 20 cases of backup energy consumption in conventional 3T-MTJ-based NV-FF using the worst-cased-oriented method and those of the self-terminated NV-FF. By utilizing the self-terminated mechanism, the backup energy consumption is greatly reduced. In fact, the average backup energy is reduced by 69% compared with that of a conventional non-self-terminated method as shown in Fig. 4(b).

III. CONTENT-AWARE WRITE ERROR MASKING TECHNIQUE CONSIDERING STOCHASTIC MTJ-SWITCHING BEHAVIOR

In order to design practical-scale MTJ/MOS-hybrid logic LSI and to broaden the scope of its application, it is important to establish a sophisticated design environment that can faithfully reflect the physical behavior of the MTJ device, while retaining good compatibility with standard EDA tools for CMOS-based VLSI. Especially in the case of such a novel logic LSI design, the effect of stochastic behavior of MTJ devices due to unavoidable thermal fluctuations of magnetization [17] must be reproduced since it often causes unexpected fatal errors in performing logic operations. Some approaches have been reported, based on Verilog-A model, however, these results were limited only to primitive logic gates or logic circuits with regular structure such as logic-array structure. From this point of view, a new design flow for MTJ/MOS-hybrid LSI considering stochastic behavior of MTJ devices has been reported by combining new supplementary design libraries that reflect the physical behavior of MTJ device and de-facto standard EDA tools [10]. By utilizing the proposed flow, various MTJ-based nonvolatile logic-in-memory (NV-LIM) circuits can be designed with Verilog Hardware Description Language (Verilog-HDL). Their operation including the effect of MTJ's stochastic switching behavior can be verified by analog-mixed-signal (AMS) simulation. Figure 5 shows a layout of the microprocessor with 90nm MOS/100nm perpendicular MTJ technology generated by the proposed flow, whose layout validity can be completely verified through DRC and LVS using standard EDA tools. The processor is based on a general purpose 32-bit microprocessor (ARM Cortex-M0), where all flip-flops in it are replaced with nonvolatile flip-flops to add non-volatility. Figure 6 shows a block diagram of the test-bench structure monitoring stochastic behavior of MTJ devices. Both counting of the number of write errors by digital simulation and difference calculation of resistance values of each MTJ device by analog simulation are simultaneously executed by maximally utilizing the AMS simulation environment.

As an concrete example of nonvolatile logic-LSI design using the above CAD environment, an MTJ-based video coding (motion-vector (MV) prediction) hardware with an MTJ-write-error-rate relaxation scheme is demonstrated under a 90 nm MOS and 75 nm perpendicular MTJ process. Figure 7 shows the circuit structure of a processing element (PE) with a dynamic error masking function. The basic function of the PE is to calculate the absolute difference between input and the stored pixel values in an 8-bit nonvolatile memory. The error masking function is embedded into each PE compactly by partially sharing the circuit for absolute difference function. The PE has two modes; test mode and operation mode. If non-negligible errors are found in the check mode, 1-bit nonvolatile flip-flop (NVFF) is set to 1, and the PE outputs 0 in the operation mode independent of the input data until the next write operation occurs. Figure 8 shows the effect of the proposed error checking function on relaxation of acceptable MTJ write error rate. Three different ways to handle error are listed by evaluating acceptable MTJ write error rate to satisfy less than 0.5-pixel average root-mean-square error in predicted MVs. The proposed dynamic error-checking scheme is quite simple but effectively mitigates the impact of failed memories regardless of the content of the video sequences, and achieves 7.8 times improvement at maximum. This technique can apply LIM-style circuitry in general, and would contribute to the design of highly reliable and low-power NV-LIM LSI.

IV. SUDDEN POWER-OUTAGE RESILIENT IN-PROCESSOR CHECKPOINTING TECHNIQUE

In energy harvesting applications, a power supply generated from a renewable power source is unstable that may

induce frequent sudden power outages, causing the inconsistency among distributed nonvolatile flip-flops (NVFFs) and hence failure rollbacks in conventional nonvolatile processors. Checkpointing techniques [18] using nonvolatile storage devices are one of effective solutions to realize continuous operations upon frequent power outages as shown in Fig. 9. The nonvolatile-storage based checkpointing can reduce the rollback time not to access the external storage while the consistency between two different nonvolatile stored data must be maintained. Until now, a few papers [19-20] have reported the methods using nonvolatile memories, such as MRAMs and ferroelectric RAMs, instead of SRAM, to store checkpoints. However, the within-processor consistency of stored data has not been considered.

The proposed in-processor checkpointing technique fixes the inconsistency using time-reminding redundant NV-FFs (TMRNVFFs). Fig. 10 shows a circuit diagram of the time-reminding redundant nonvolatile flip-flops (TM-RNVFFs), where the redundancy, r=3, is used. The TM-RNVFFs store the current and the past few data with the timing information of storing. If several NV-FFs fail to store the current data due to the sudden power outages, the proposed in-processor checkpointing technique exploits the timing information to find the common newest state among distributed NV-FFs, leading to correct rollbacks to the state with consistency.

The sudden power-outage effect is modeled to perform design space explorations at different configurations, such as redundancy and checkpointing period. Nonvolatile ARM Cortex-M0 processors are designed using hybrid 90nm CMOS and 70nm magnetic tunnel junction (MTJ) technologies as shown in Fig. 11. Table 1 summarizes the performance on nonvolatile ARM Cortex-M0 processors. Based on the design space explorations, the proposed nonvolatile processor achieves a several order-of magnitude reduction in rollback error probability with a power dissipation overhead of 11.6% and an area overhead of 52.1% in comparison with the conventional nonvolatile processor.

V. CONCLUSION

Some key techniques for realizing practical-scale nonvolatile logic LSIs have been introduced and their usefulness has been demonstrated in comparison with those of the corresponding conventional approaches. As a future prospect, it is also important to extend the nonvolatile MTJ-based computing technique toward non-standard VLSI-computing paradigm, such as brain-inspired computing.

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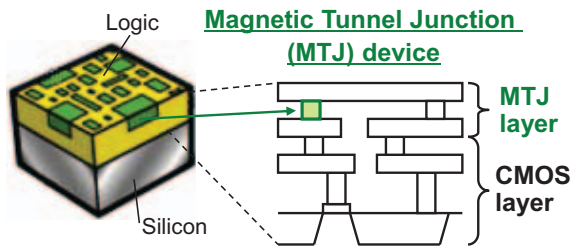
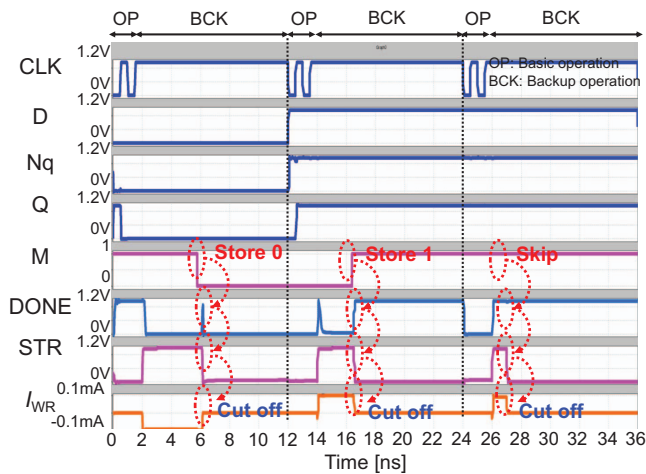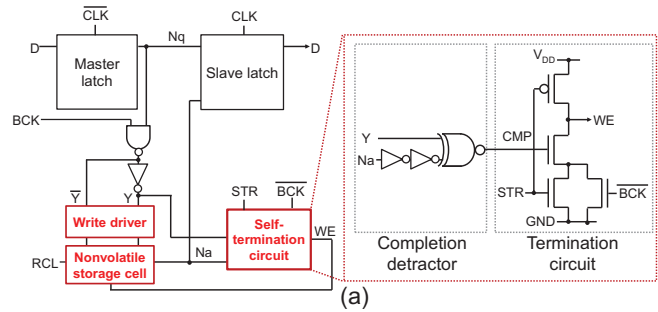Figure 1: MTJ-based Nonvolatile logic-LSI architecture with logic-in-memory structure.

(a)

Figure 3: Basic behavior, where three times of backup operations (denoted as BCK).are performed just after each basic operation (denoted as OP).

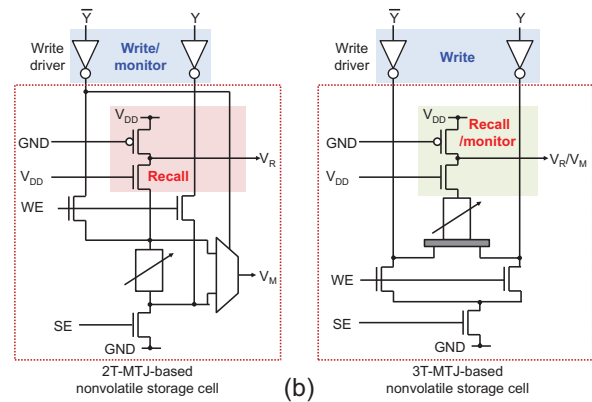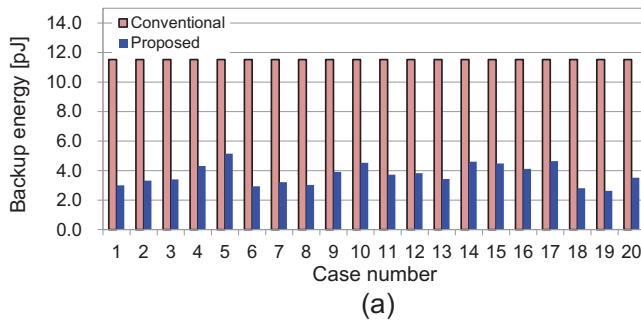

(b)

Figure 2: Design of a self-terminated NV-FF; (a) overall schematic, and (b) nonvolatile storage cell configurations.

(a)

	Worst-case-oriented (Conventional)[*3]	Self-terminated (Proposed)
Average backup energy [pJ] [*1, 2]	11.5 pJ	3.57 pJ

*1) The number of iterations is 100.
*2) Random patterns are used for the logic inputs and initial states of 3T-MTJ devices.
*3) The width of the write current pulse is fixed to 12 ns.

(b)

Figure 4: Monte-Carlo simulation result; (a) comparison of write energy consumptions with 20 benchmark circuits, (b) comparison of average energies.
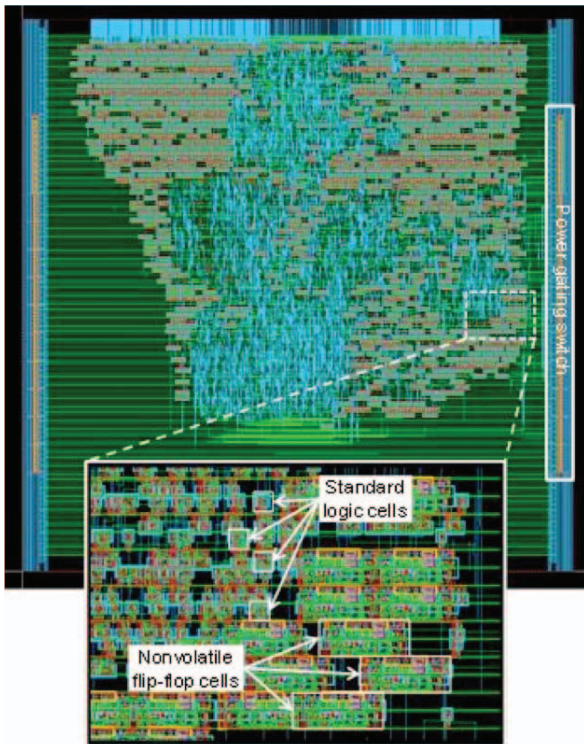
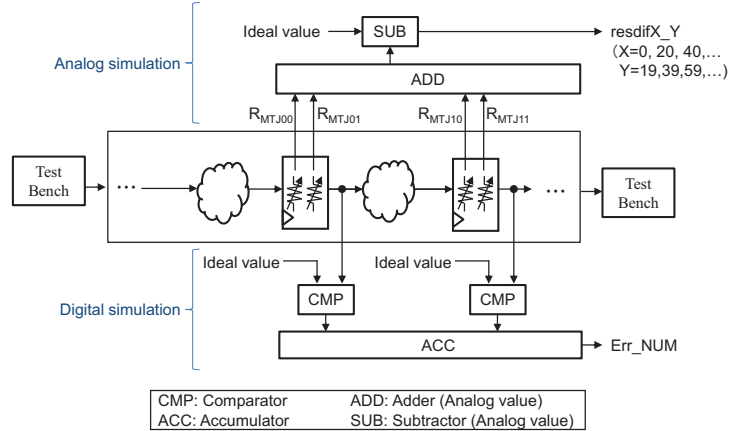Figure 5: Layout of experimental nonvolatile microprocessor.

Figure 6: Block diagram of the test-bench structure for simulation.

CMP: Comparator   ADD: Adder (Analog value)
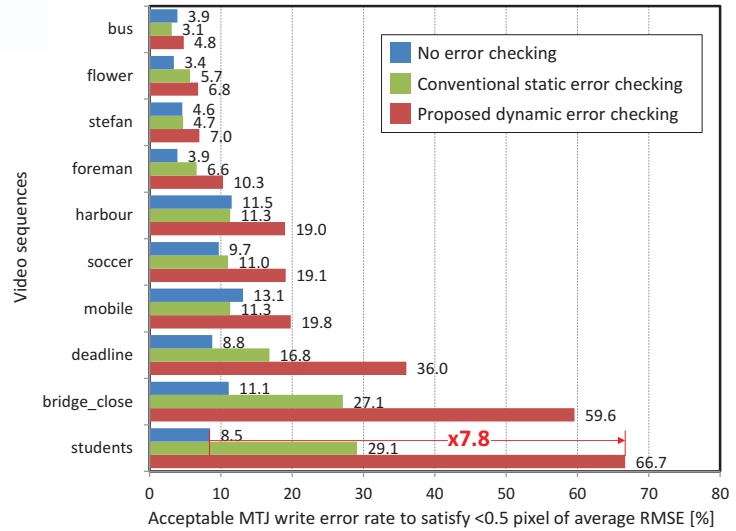ACC: Accumulator   SUB: Subtractor (Analog value)

Figure 8: Effect of an error masking function on relaxation of acceptable MTJ write error rate.
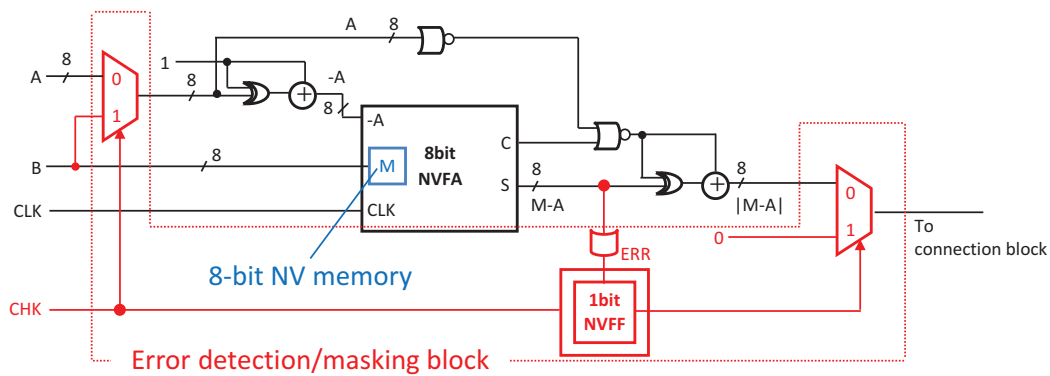

Figure 7: Processing element with error detection/masking functions. The existence of error is represented by the signal ERR.
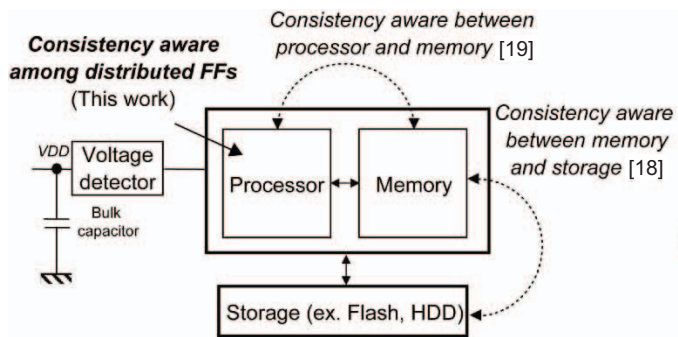
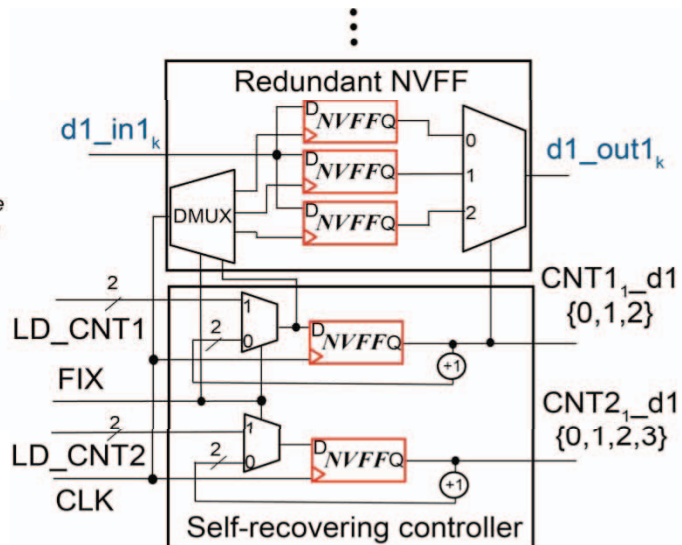Figure 9: Consistency-aware checkponting using nonvolatile devices.

Figure 10: Time-reminding redundant nonvolatile flip-flops (TM-RNVFFs), where the redundancy, $r=3$, is used.
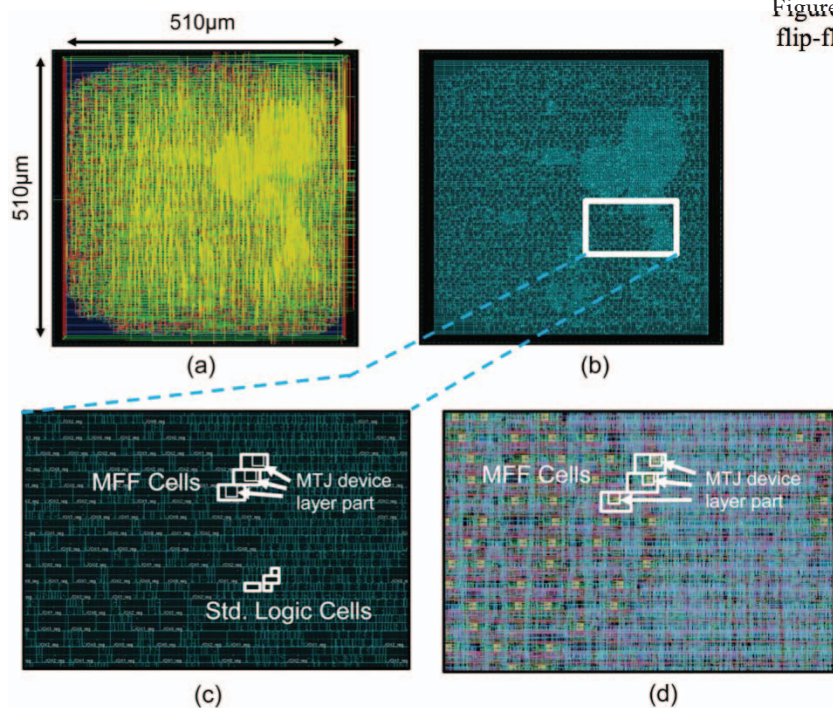

Figure 11: Layout of the proposed nonvolatile ARM Cortex-M0 processor designed using hybrid 90nm CMOS and 70nm MTJ technologies; (a) the layout produced using an automatic place-and-route tool, (b) the cell placement view w/o wiring, (c) a detailed layout consisting NV-FFs and standard logic cells, and (d) the final layout for chip fabrication.

Table 1: Performance comparison of nonvolatile ARM Cortex-M0 processors.

		Conventional	Proposed					
			Triple-redundant NVFFs (r=3)			Dual-redundant NVFFs (r=2)		
Configuration (k)		-	10	20	40	10	20	40
Total power dissipation [mW] @10 MHz (P_t)	n=1	3.04	5.42	4.97	4.75	3.89	3.51	3.29
	n=5	1.06	1.99	1.75	1.63	1.46	1.28	1.16
	n=10	0.82	1.56	1.35	1.24	1.16	1.00	0.90
	n=20	0.69	1.35	1.15	1.05	1.01	0.86	0.77
Rollback error probability (p_E) @ $\sigma_G=1$ and $\sigma_L=0.015$	n=1	0.3173	0.0027	0.0027	0.0027	0.0455	0.0455	0.0455
	n=5	0.3173	~0	~0	4.71E-08	~0	~0	5.55E-12
	n=10	0.3173	~0	~0	4.71E-08	~0	~0	5.55E-12
	n=20	0.3173	~0	~0	4.71E-08	~0	~0	5.55E-12
Area [μm^2]		85,282	197,073	186,835	177,307	150,492	136,858	129,681
Write energy per checkpointing [pJ]		247	428	403	390	304	278	265
Re-computation energy (E_r) [pJ] (n=10)		256	511	426	383	385	326	288