Workload Dependent Reliability Timing Analysis Flow

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***Abstract*— Silicon measurements indicate a change in frequency limiting path rankings as per aging and also as a function of workload. This paper proposes a simulation flow that leads to the identification of workload specific aged critical paths. Gate-level models are a means to estimate aging of the critical paths by taking into consideration the stress experienced by corresponding standard cells for a given digital circuit workload during circuit operational lifetime. We thus estimate the workload based aging margins for a particular design using this simulation flow.**

Keywords— Workload, Aging, Critical Path, Reliability

I. PROBLEM STATEMENT AND FLOW METHODOLOGY

A. Problem Statement :

The reliability models based analysis flow has allowed for a 2-2.5X reduction in design margins [1]. The frequency degradation spread coupled with a negligible degradation of the critical path on circuit aging leads to a conclusion that the critical path changes as per aging [2]. The workload influence on aging is investigated with the aim of exploring further reduction in design margins and a more precise in-situ monitor insertion strategy. Also, the number of PVTs demanded by the design teams for signoff timing verification is increasing exponentially and it has become imperative to develop industrially applicable solutions. This paper proposes such a workload reliability simulation flow.

B. Workload Dependent Aged Timing analysis Flow :

Signal probability and switching activity at the standard cell inputs are workload indicators [3]. These workload indicators of a specific application running on a processor circuit, that is representative of the circuit workload during its lifetime is dumped into a VCD file during gate level simulations. Signal probability and switching activity values at the inputs of each standard cell in the design is extracted from this VCD file [5]. The aged timing library files with standard cells aged at 50% input signal probability based on the Design In Reliability (DiR) models already exist. This aged cell delay value at 50% signal probability and workload dependent signal probability values are used to calculate the workload specific delay (**Fig. 1**). This paper introduces the method of using workload indicators to calculate path delay aging margins. This paper does not address HCI effects due to switching activity at GHz frequency range. Terms signal probability and duty cycle mean the same and are used interchangeably during this analysis.

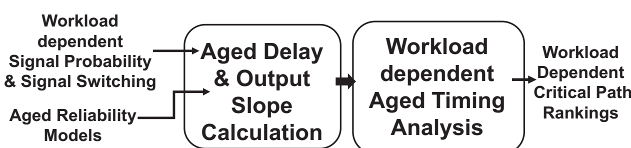

Fig 1. Design Workload Dependent Timing Analysis

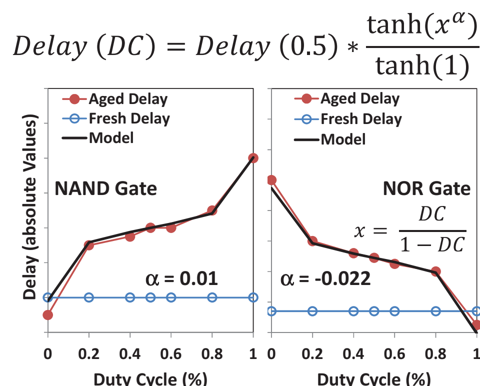

Fig 2. Standard Cell Aging Dependence on Duty Cycle (Input Signal Probability) for arc A

II. HIERARCHICAL APPROACH TO FLOW DEVELOPMENT

A. Workload Impact on Aging of Standard Cells

The present aged library characterization assumes a uniform workload of 50% duty cycle at all inputs during its operational lifetime. The resulting aging simulations is thus not workload dependent and the influence of input signal probability on timing degradation is not considered. (**Fig 2**) proposes a new gate level analytical model that enables the calculation of duty cycle dependent aged cell delay with the knowledge of preexisting 50% duty cycle aged delay in standard aged library. The aged delay for different duty cycles ranging from 0% to 100% for a certain arc is obtained from aged timing library files characterized for respective input duty

cycles and plotted in red. A bounded sigmoid function that models the aged delay dependence on input duty cycle is depicted in black. The choice of such a function was for its robustness and analytical inverse function. This dependence is characterized by a certain '**α**' exponent of the bounded sigmoid function.

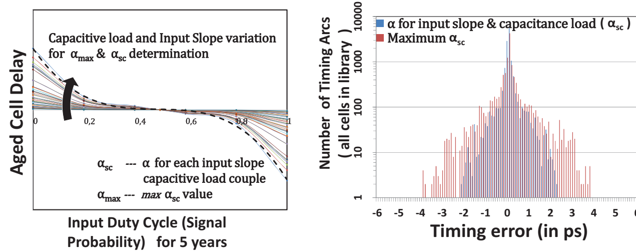

Fig 3a. Standard cell characterization for α determination
Fig 3b. Error range of 2ps for α_{sc} and 4ps for α_{max}

Cell delay and output slope of a certain timing arc vary as a function of capacitive load and input slope which is the basis of creation of timing library files. Variation of aged cell delay on arc A for a 2-input NOR gate is studied for a range of loads and input slopes, where the different line plot in **Fig 3a** represents aged cell delay corresponding to a input slope and capacitive load pair. The '**α**' value corresponding to the worst case input slope and capacitive load is chosen as the '**α**' value of a particular standard cell in this study. This method of choosing '**α**' injects a certain pessimism into the aged cell delay calculation and is a limitation of this analysis. Accuracy of this approach for a duty cycle between 0% and 100% for a standard cell library of multiple cells with 15,000 timing arcs yields a maximum tolerance of 4ps **(Fig 3b)** and a null average delay difference with the cell library. An analysis of '**α**' for the corresponding input slope and capacitive load couple '$\boldsymbol{\alpha_{sc}}$' yields an error margin of 2ps (**Fig 3b**). Thus, a gain in accuracy is observed with a case dependent '**α**' choice and an error comparison between the two methods allows for accuracy validation of this method.

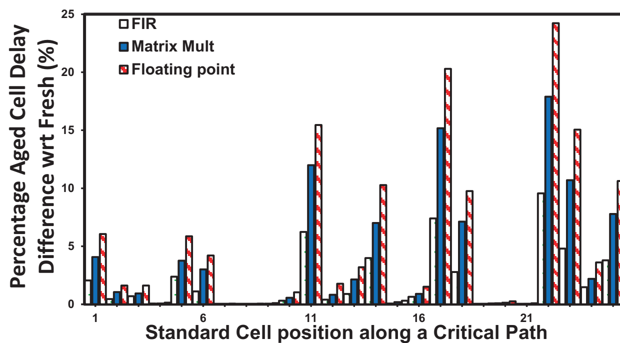

Fig 4. Workload Dependent Standard Cell Aging along a Critical Path

B. *Cumulative Workload Impact on Design Frequency Limiting Paths*

The cumulative delay of each of the standard cells along the frequency limiting paths of a digital design determine the path delay. The aged delay is a function of the input duty cycle modelled by the equation in **Fig. 2**. Workload dependent signal probability at the cell inputs and the aged cell delay at 50% duty cycle are given as inputs to this equation to determine the workload dependent aged delay. The duty cycle based aged delay model is used for the calculation for delay of critical path elements and plotted (**Fig 4**). We observe that the aged delay of the standard cells differ significantly with respect to workload.

This analysis is extended to 100 near critical paths in the open source microcontroller MSP430 design [6] testcase. The workload dependent duty cycle is obtained from the VCD file. The method used for determining the critical path delay as mentioned above is used to calculate the aged path delays and plotted (**Fig. 5**). We conclude that, for workload independent analysis, a difference of 2-3x is observed between the mean path delay degradation on aging and critical path delay. Workload consideration translates into changes in the mean and standard deviation for the same testcase.

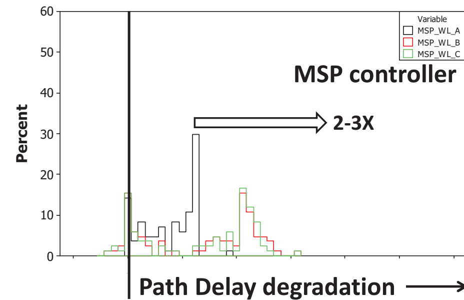

Fig 5. Workload Impact on Path Delay distribution for MSP design

CONCLUSION

Delay degradation calculation based on the signal probability paves way for an easy light weight solution for workload or signal probability based aged timing analysis in an industrial setting by bypassing all the surplus standard cell characterization with a reasonable degree of accuracy. Aging margins for a workload can thus be quantified and the accurate estimation of workload dependent aged critical path ranking allows for a judicious use of in-situ performance monitors without an increase in area overhead. Efforts are underway to include this method in design & verification flow.

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