Robust TSV-based 3D NoC Design to Counteract Electromigration and Crosstalk Noise

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***Abstract*—A 3D network-on-chip (3D NoC) is an enabler for the design of high-performance and energy-efficient manycore chips. Most popular 3D NoCs utilize the Through-Silicon-Via (TSV)-based vertical links (VLs) as the communication pillars between the planar dies. However, the TSVs in a 3D NoC may fail due to both workload-induced stress and crosstalk capacitance. This failure negatively affects the overall achievable performance of the 3D NoC. In this work, we analyze the joint effects of workload-induced stress and crosstalk on the TSV mean-time-to-failure (MTTF) and hence the 3D NoC lifetime. We demonstrate that if we only consider the effects of electromigration on the TSVs due to workload-induced stress then the estimated MTTF and the subsequently lifetime of 3D NoC are too optimistic. Due to the combined effects of workload and crosstalk noise, the lifetime of 3D NoC reduces significantly. Subsequently, we demonstrate that a spare TSV allocation methodology considering the joint effects of workload and crosstalk noise enhances the lifetime of the 3D NoC by a factor of 4.6 compared to when only the workload is considered for a given spare budget of 5%.**

Keywords—Crosstalk; electromigration; TSVs; MTTF; 3D NoC; manycore chip; lifetime; reliability.

I. Introduction

A three-dimensional network-on-chip (3D NoC) has the potential to significantly improve the performance of manycore chips. Most 3D NoCs utilize through-silicon-vias (TSVs) as the vertical communication links between the planar dies to exploit the benefits of shorter communication distance, and increased packing density [1][2]. However, the anticipated performance gain of 3D NoCs can be compromised due to TSV failure [3][4]. One of the major reasons for TSV failure in a 3D NoC is the nonhomogeneous workload distribution for the vertical links (VLs). The resultant stress causes electromigration effects for TSVs and thereby increasing their resistances, which in turn increase the delay. Ultimately, it will negatively affect the NoC performance [5]. In addition, TSVs in a 3D NoC are placed in bundles to create the VLs. In each VL, the cross-coupling effects from the neighbors increase the worst-case delay of each TSV [6]. The combined effects of workload-induced stress and crosstalk lead to significant performance and reliability concerns for TSV-enabled 3D manycore chips. The failure of TSVs changes network configuration, increases the network latency, degrades system performance, and ultimately reduces the overall NoC lifetime.

To improve the reliability of any 3D IC, spare TSV allocation has been advocated [3][4]. However, the joint effects of workload-induced stress and crosstalk were not considered for spare TSV allocation. In this work, our goal is to explore the combined effects of these two TSV reliability issues on the performance and robustness of a 3D NoC. Consequently, we evaluate the efficacy of a spare TSV allocation scheme by considering the joint effects of workload-induced stress and crosstalk to enhance the lifetime of the 3D NoC.

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II. Related Prior Work

Several studies have addressed TSV failures in a 3D IC. Prior work focused on exploring the types of TSV faults, analytical and statistical modeling of TSV failures, developing strategies to reduce the number of fabrication and bonding defects, handling timing faults, and improving chip yield rates [7] [8]. Consequently, fault tolerant architectures were developed [9], and spare TSV (sTSV) allocation strategies were proposed to improve reliability [3][4].

Several studies have also explored electromigration (EM) induced TSV failures and modeling of TSVs under EM [10] [11]. The effects of externally applied stress on EM were analyzed for TSV materials and the corresponding bonding wires [10]. The authors in [12] explored clock tree synthesis under EM faults and evaluated their impacts on clock-delay. Similarly, the effects of EM were analyzed on power and ground lines for a 3D IC [13]. A bundle-based spare TSV (sTSV) placement method and mapping strategy between the functional TSVs (fTSVs) and sTSVs were proposed for EM faults to achieve a target mean-time-to-failure (MTTF) for the system [14].

From the NoC design perspective, it has been demonstrated that a small-world network-enabled 3D NoC (3D SWNoC) is extremely robust against VL failures [15]. The effect of workload-induced stress on the TSV-based vertical links of a 3D NoC has also been addressed [16]. In particular, due to the non-homogeneous workload, heavily used TSVs wear-out quickly and contribute to the wear-out of neighboring TSVs. Hence, the MTTF of those TSVs will decrease, which will adversely affect the overall lifetime of the chip. It is also shown that by employing adaptive routing, the MTTF of a 3D NoC can be improved significantly [16].

In addition, crosstalk severely affects the delay, and consequently the MTTFs of the TSVs. Hence, if we only consider the workload-induced stress for analyzing the 3D NoC reliability, we would be targeting only one part of the overall problem. The combined effects of the electromigration arising out of workload-induced stress and the crosstalk capacitance need to be considered to determine the realistic lifetime of a 3D NoC. Consequently, any sTSV allocation method to improve 3D NoC reliability must consider these two factors in conjunction. Hence, in this paper, our focus is to evaluate the

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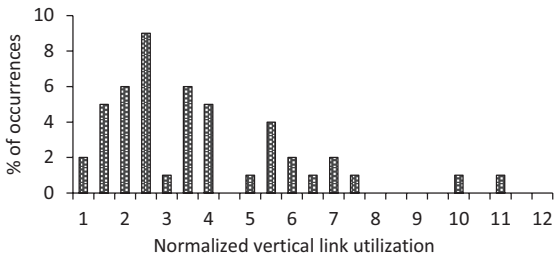

Fig. 1: Variation in vertical link utilization pattern for the DEDUP benchmark from the PARSEC benchmark suite.

combined impact of electromigration and crosstalk on TSV MTTF and 3D NoC reliability.

III. TSV Reliability From 3D NoC Perspective

In this section, we discuss the TSV failure mechanism from a 3D NoC perspective and also present the effects of workload-induced stress and crosstalk noise on the TSV MTTF.

A. Effects of Workload-induced Stress

In a 3D NoC, the VLs consisting of TSVs undergo large variation in workload distribution depending on the NoC architecture and application. To explain this, in Fig. 1, we plot the workload distribution for all the TSV-enabled VLs in a 3D NoC for one of the well-known PARSEC benchmarks, viz., DEDUP. To characterize the individual workload for each VL, we define the active VL utilization factor, $u_k(t)$, at any given instant of time, t, for the k^{th} VL as –

$$u_k(t)=\frac{Busy\ (t,\ k)}{Cycles\ (t,\ k)}\ ,\quad \forall_{\ k}\in\{1,2,...,N\} \tag{1}$$

where, N is the total number of VLs; $Busy$ $(t,\ k)$ is the number of cycles during which k^{th} VL has actively transferred data; and $Cycles$ $(t,\ k)$ indicates the total number of simulation cycles. In this figure, the horizontal axis is normalized with respect to the minimum value of $u_k(t)$ and the vertical axis indicates the percentage of VLs having a particular utilization value. From this figure, it can be seen that the average utilization metric has a large variation across the VLs. Such variation of workloads, seen for other benchmarks as well, across the VLs causes non-homogeneous stress. From the physical perspective, the workload-induced stress causes the TSV material to undergo electromigration at the junction of the TSVs and their respective landing pads. In addition, higher workload makes the EM effects more pronounced. As a result, a void is created at the TSV landing pad resulting in reduction of the effective TSV cross sectional area, and forcing current to pass through the TSV barrier material (e.g., TiN). The net outcome of the increase in VL utilization is that the resistance, and consequently, the delay of each TSV belonging to the VL also increases. The increase in resistance of TSVs with time can be modeled as [5]-

$$\mathrm{R}(t)\text{-}\ R_0=A\ \ln\left(\frac{t}{t_0}\right) \tag{2}$$

Here, t_0 is the time when the size of the void created at the landing pad equals that of the TSV cross sectional area; the factor, A, is aging coefficient (independent of the stress condition and only depends on the TSV barrier material); and

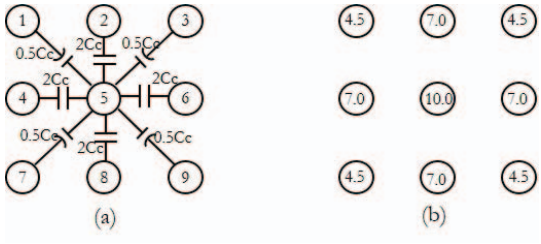

Fig. 2: Placement of TSVs in a grid. (a) The worst case crosstalk capacitance for the center TSV (TSV 5). (b) The aggregation of worst case C_c values for each TSV.

R_0 is initial resistance of the TSV. The parameter, t, is the active utilization time, and hence, a linear function of $u_k(t)$. The large workload variation among the VLs (and that of the TSVs) results in different rate of increase for the resistance parameter, $R(t)$, and consequently varying TSV delay.

B. Effects of Crosstalk Capacitance

Crosstalk noise in a TSV bundle mainly depends on two important factors, viz., the exact location of the TSV (which determines the proximity to other TSVs), and the bit patterns. For a TSV based 3D IC, this causes variation in delay. To illustrate this, we consider the most popular TSV placement strategy viz. the grid-based arrangement. Fig. 2 shows the TSV placement for a 3x3 configuration and the associated worst case crosstalk capacitances for each TSV in the bundle. For a single signal transition between a pair of adjacent TSVs, the crosstalk capacitance is assumed to be C_c. As seen from the figure, the center TSV is subject to the highest crosstalk noise (10 C_c), while the adjacent neighbors face the second highest (7 C_c) and finally, the corner TSVs has the minimum crosstalk (4.5 C_c). While the self-capacitance is same for all TSVs in the bundle, the crosstalk depends on the bit pattern and the position of the TSV in the bundle. Hence, the delays of the TSVs in a bundle also vary. We have considered a 3x3 bundle to visually demonstrate the crosstalk effects, however, all other grid based configurations i.e., 3x4, 4x4, 4x5, 5x5 etc. are supersets of this particular placement strategy. Hence, the worst case crosstalk as found in this 3x3 grid pattern is applicable to the other configurations also.

C. Joint Effects of Workload and Crosstalk on TSV MTTF

Due to the above-mentioned variation in the TSV resistance arising out of workload-induced stress and the crosstalk, the delay of the TSV also increases. At a certain point of time, the delay increases beyond the acceptable limit imposed by the timing constraint of the system. This scenario can be considered as a failure of TSV, and the corresponding time is termed as the mean-time-to-failure (MTTF). In general, 10% increase in delay is considered as the failure of a TSV [5] [11]. In this work, we also consider the time corresponding to this 10% increase in delay as the MTTF for any TSV [5] [11]. The overall MTTFs depend on the workload-induced stress as well as the crosstalk capacitance. If we do not consider any of these factors, the MTTFs show large deviation from the actual values.

IV. Problem Formulation

In this work, we consider the small-world network enabled 3D NoC (3D SWNoC) as the suitable architecture for exploring

the effects of electromigration and crosstalk on the overall reliability and lifetime. This particular architecture is chosen due to its better performance and robustness compared to other existing counterparts [15]. Our target is to explore how the workload variation and crosstalk affect the overall performance and reliability of a 3D SWNoC. Note that, the subsequent analysis presented in this work is general, and it can be equally applied to any other TSV-enabled 3D NoC.

A. Reliability Metric: Lifetime of 3D NoC

Without any VL failure, the 3D SWNoC initially (at $t = 0$) exhibits lower energy-delay-product (EDP) values compared to a standard 3D MESH [15]. However, due to VL failure, the EDP increases progressively and at a certain time, the EDP of 3D SWNoC increases beyond that of a fault-free 3D MESH. At this point, the 3D SWNoC is no longer more efficient than the 3D MESH, and the corresponding time is termed as the *lifetime* of the 3D SWNoC. To express it formally-

$$lifetime_{\text{3D SWNoC}} = \left\{ t : (EDP_{\text{3D SWNoC (at } t=t)} = EDP_{\text{3D MESH (at } t=0)}) \right\} \quad (3)$$

Hence, the term, *lifetime* of 3D SWNoC, indicates the period of time up to which it operates with a lower EDP than a conventional 3D MESH. In this context, the EDP of 3D MESH is considered merely as a reference point for comparative study. However, any other definition of lifetime of 3D NoC (e.g. 10% increase in EDP value), is applicable as well.

B. Problem statement

In this work, we consider a 3D NoC with multiple planar dies. The inter die communication take place though N number of VLs (each VL having n fTSVs). The 3D NoC executes a set of applications and due to the nature of the applications, the workload distribution of the VLs is nonhomogeneous and some of the VLs experience higher traffic load than the others. Moreover, individual TSVs in each bundle are affected by crosstalk capacitance. Consequently, the MTTFs of these VLs vary depending on the position of individual TSVs in a bundle and the workload-induced stress of the VLs. Traditionally, TSV failure in a 3D IC has been addressed by spare TSV allocation. In this work, we consider the joint effect of workload-induced stress and TSV crosstalk capacitance on a spare TSV allocation methodology to improve the overall MTTF of a 3D NoC.

In most of the existing sTSV allocation algorithms TSV failures arising out of clustering faults, fabrication and bonding defects, uniform-random faults and timing faults are explored [3] [4] [8]. In contrast, we target the TSV failure due to the nonhomogeneous workload-induced stress that degrades NoC performance over time along with the crosstalk capacitance.

C. TSV Fault Model with Workload Variation and Crosstalk

To determine the delay of any TSV, we consider the circuit model shown in Fig. 3 [17], where $R_{workload}$ is the net increase in the resistance value, $R(t)$, due to workload-induced stress. In the figure, the parameters- R_{TSV}, L_{TSV}, C_{TSV} indicate the TSV resistance, inductance, and self-capacitance respectively, while C_c' denotes the effective crosstalk of a TSV. The parameter, $R_{workload}$, has value of zero at $t = 0$, and then depending on the workload characteristics, starts to increase. Intuitively, the TSV

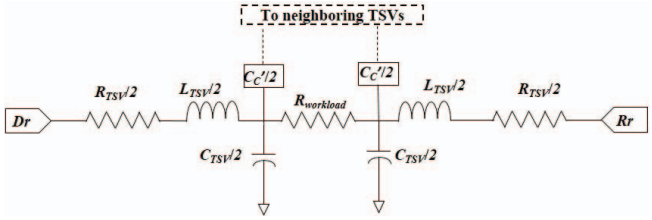

Fig. 3: Equivalent circuit model of TSV to determine the effects of workload-induced stress and crosstalk.

with the worst case crosstalk in the highest utilized VL is expected to have the maximum delay and the lowest MTTF. Consequently, this particular combination becomes the main bottleneck for the 3D SWNoC from both the performance and reliability perspectives.

D. Spare TSV Allocation for Reliability Improvement

The goal of sTSV allocation is to replace the failed fTSVs with spare ones so that a certain level of achievable performance is maintained. However, the spare allocation methodology should incorporate the effects of both electromigration (workload-induced stress) and crosstalk. To undertake a detailed analysis regarding this joint effect, any existing sTSV allocation mechanism can be adopted. In this work, we consider the sTSV allocation algorithm proposed in [14], where the main goal was to handle EM-induced faults. For this algorithm, at each step, the TSV with the minimum MTTF was explored, and subsequently allocated with the spares until the upper limit on the budget is reached or the target system MTTF is achieved. However, to employ this algorithm in our work, we make two main modifications. First, we consider the joint effects from workload-induced stress and crosstalk capacitances together on the TSV MTTFs. Secondly, our goal is to maximize the lifetime of the 3D NoC by considering the EDP profile and TSV MTTFs. In order to identify the TSV with the lowest MTTF, at any particular time, t, we consider the utilization pattern $u_k(t)$, and corresponding crosstalk capacitance value of that particular TSV. Allocating a spare to the TSV with lowest MTTF ensures the minimal effect of TSV failures on the NoC EDP profile and thereby the lifetime of 3D NoC is maximized.

V. Experimental Results and Analysis

In this section, we analyze the performance of the 3D SWNoC in the presence of workload-induced stress and crosstalk noise. Subsequently, we discuss the efficacy of a sTSV allocation mechanism in the presence of these two factors to enhance the lifetime of the 3D SWNoC.

A. Experimental Setup

We consider a Chip Multiprocessor (CMP) consisting of 64 cores and 64 routers equally partitioned into four layers. In each die, 16 cores (and associated routers) are placed at regular intervals in a grid pattern and TSVs act as VLs in between layers. The TSV dimensions for this work are- length of 15 μm, diameter of 2.3 μm, and pitch of 30 μm [5] [18]. The TSV model parameters i.e. R_{TSV}, L_{TSV}, C_{TSV}, C_c' are calculated following [18] [19]. The associated logic circuitry is synthesized from an RTL level design using the ST 28-nm standard cell library in Synopsys™ Design Vision.

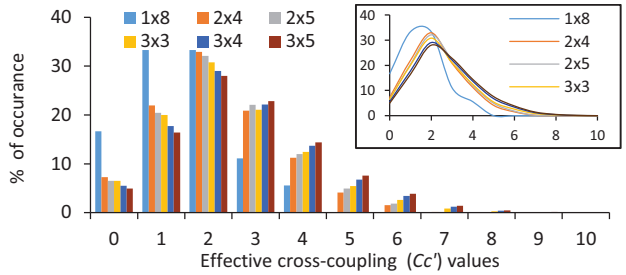

Fig. 4: Variation of crosstalk capacitances for different TSV grid based placement configurations

Table I: Worst case and effective crosstalk capacitances for TSV bundles with different configurations

Grid Patterns	Worst C_c'	Effective C_c'
1x8	4 C_c	1.56 C_c
2x4	7 C_c	2.25 C_c
3x3	10 C_c	2.46 C_c
3x4	10 C_c	2.63 C_c
3x5	10 C_c	2.81 C_c

To evaluate the performance of 3D NoCs, we use a cycle-accurate NoC simulator that can simulate any regular or irregular 3D architecture. The length of each message is 64 flits and each flit consists of 32 bits. The NoC simulator uses wormhole routing, where the data flits follow the header flits once the routers establish a path. For the 3D SWNoC network, the topology-agnostic Adaptive Layered Shortest Path Routing (ALASH) algorithm is adopted [20]. The energy consumption of the network routers was obtained from the synthesized netlist by running Synopsys™ Prime Power, while the energy dissipated by wireline links was obtained through HSPICE simulations. We consider CANNEAL, DEDUP and VIPS benchmarks from PARSEC [21], and FFT, RADIX and WATER from SPLASH-2 suite in this performance evaluation [22]. These benchmarks vary in characteristics from being computation-intensive to communication-intensive in nature and thus are of particular interest in this work.

B. *Analyzing TSV MTTF*

In this section, we analyze the effects of crosstalk capacitance and workload on TSV delay and MTTF.

1) Determination of Effective C_c' Values

To evaluate the effects of neighboring TSVs on C_c' value, we consider in total six different TSV placement configurations i.e. 1x8, 2x4, 2x5, 3x3, 3x4, 3x5 and apply all the possible bit patterns (signals) to determine the effective C_c' values. Fig. 4 shows the variation of C_c' for these configurations (inset shows their respective envelopes). The vertical axis indicates the percentage of occurrence for any particular C_c' value.

Table II: Effective crosstalk capacitance for different types of TSVs in a 3x3 grid pattern based placement

Types of TSVs	TSVs	Worst C_c'	Effective C_c'
1	5	10 C_c	4.04 C_c
2	2, 4, 6, 8	7 C_c	2.74 C_c
3	1, 3, 7, 9	4.5 C_c	1.77 C_c

**In this work, C_c is the amount of crosstalk for a single signal transition between two neighboring TSVs.*

As seen from the figure, the grid pattern 1x8 has the lowest value for C_c' (clustered towards the left) while 3x5 shows the maximum possible C_c' value (having higher Cc values more frequently) among all of them. In a 1x8 configuration, the worst case crosstalk has a value of 4 C_c while the grid patterns of 3x3, 3x4, 3x5 have the worst value of 10 C_c. In addition, the latter grid patterns have 1, 2, and 3 candidates respectively those can potentially face the highest 10 C_c values. As a result, the C_c' distribution curve for 3x5 shifts to the right on the horizontal axis. For other placement configurations e.g. 4x4, 4x5, 5x5, 5x6, 6x6 etc., the worst case C_c' remains same as 3x3 configuration (10 C_c), however the number of TSVs having the highest C_c' values increases. As a result, the effective C_c' also increases for those grid patterns as well. In this work, we consider a 32-bit datalink (flit width is 32 bits) and 4:1 serialization ratio for the TSVs. Hence, we choose the 3x3 gird pattern as it satisfies the VL design requirements for further MTTF analysis.

From the practical point of view, the TSVs in a 3D NoC do not always encounter the worst case crosstalk noise. Hence, we also calculate the effective C_c' value by considering all possible bit patterns for the TSVs in a bundle. Table I shows the effective values for C_c' for the above mentioned TSV bundles. As expected, the 3x5 grid has the highest amount of average effective C_c' value among all the configurations while the lowest value is observed for 1x8 grid pattern. However, due to the comparatively longer inter-TSV wire-length requirement, the this 1x8 configuration is not considered in practice.

2) Joint Effects Of Crosstalk and Workload on MTTFs

The joint effects of workload-induced stress and crosstalk capacitance can result in the large variation in TSV MTTFs for the 3D SWNoC. To explain this, we consider the 3x3 TSV grid pattern from Fig. 2. For this grid pattern, all nine TSVs are numbered from 1 through 9 as shown in this figure. These TSVs can be categorized into three types based on their worst case

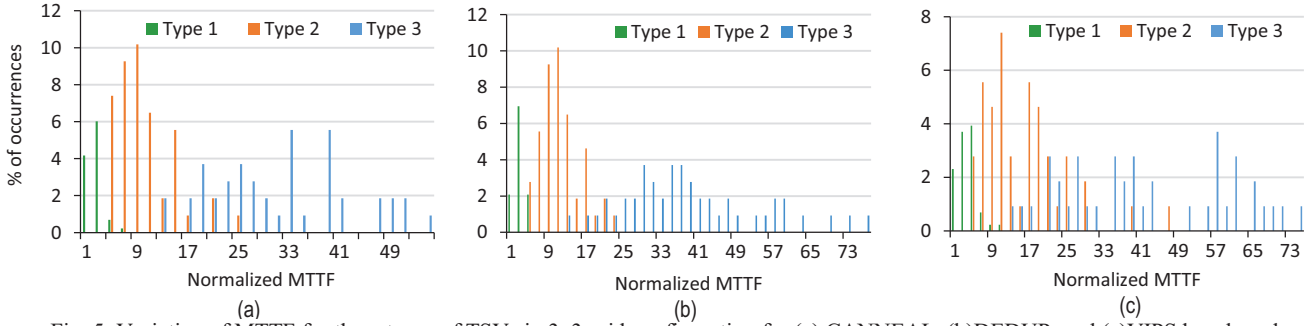

Fig. 5: Variation of MTTF for three types of TSVs in 3x3 grid configuration for (a) CANNEAL, (b)DEDUP, and (c)VIPS benchmark.

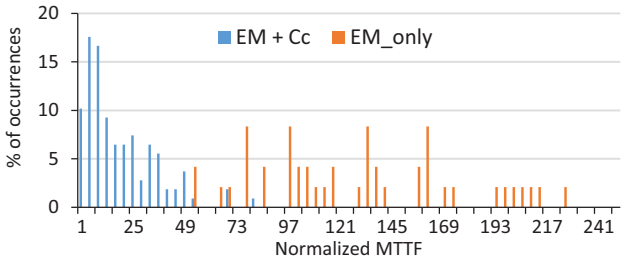

Fig. 6: Effects of only workload-induced stress (EM_only) and joint effects of EM and crosstalk capacitances (EM + Cc) on TSV MTTF distribution for CANNEAL benchmark.

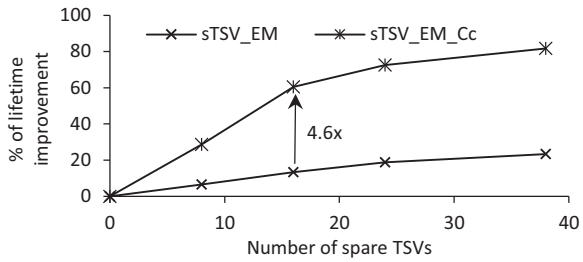

Fig. 7: Improvement of lifetime of 3D SWNoC with the spare TSV allocation algorithm by considering only workload-induced stress (sTSV_EM) and the joint effects (sTSV_EM_C_c).

crosstalk capacitances (similar classes can be identified for 3x4, 3x5, 4x4, 5x5 placements as well). The first type (Type 1) consists of the center TSV of each bundle (TSV 5, shown in Fig. 2), which has the highest amount of C_c' value (shown in Table 2). The second (Type 2) and third (Type 3) categories are the adjacent neighbors of Type 1 TSVs (TSVs 2, 4, 6, 8), and the corner TSVs of the bundle (TSVs 1, 3, 7, 9) respectively. These classes i.e. Type 1, 2, and 3 have in total 1, 4 and 4 candidates respectively for this particular 3x3 grid pattern. Table II shows the worst case and effective (averaged over all possible bit patterns for the 3x3 grid) crosstalk capacitances. We consider the effective capacitance values for the following MTTF distribution analysis.

Now, in addition to the crosstalk capacitance, the resistance of the TSVs also increases due to the workload-induced stress and resulting electromigration (equations (1) and (2) in Section III). These two together increase the TSV delay and influence the overall MTTF. Fig. 5 shows the variation of MTTF vs. the occurrence frequency (in percentage) for the above-mentioned three types of TSVs considering the joint effects of workload and crosstalk capacitance. We consider all the TSVs belonging to different VLs. The horizontal axis indicates the normalized MTTFs (normalized with respect to the lowest value of the system). For this MTTF analysis purpose, we have considered three benchmarks from the PARSEC suite viz. CANNEAL, DEDUP, VIPS. These benchmarks are chosen as the representative of high, medium, and low traffic-injection benchmarks. From these figures, it is seen that the MTTFs vary widely among different types of TSVs. Expectedly, Type 1 has the maximum crosstalk capacitance values, and consequently, the lowest MTTFs, while type 3 TSVs have the minimum effective C_c' and the resultant highest MTTFs. Workload variation and resultant nonuniform stress result in different resistance values for the TSVs belonging to various VLs. On top of this, the presence of crosstalk capacitance, each TSV within the VL possesses different MTTF. Hence, large variation in MTTFs is observed for different TSVs across the VLs.

3) TSV MTTFs with only Workload-induced Stress

From the above analysis, it is clear that the MTTFs are significantly affected by the crosstalk capacitance. However, if we only consider the workload-induced stress without considering the effects of crosstalk capacitance from the neighboring TSVs, then the resultant TSV MTTFs may have significant deviation from the actual one. To explain this, Fig. 6 plots the TSV MTTF variation for the CANNEAL benchmark considering both these cases. Other benchmarks also have similar distributions, however, we have omitted presenting those for brevity. The MTTFs with only considering workload-induced stress are marked as *EM_only* while the joint effects of workload and crosstalk are considered for the *EM+*C_c. From the figure it is clear that the *EM_only* overestimates the MTTFs (clustered towards right in the figure) and fails to capture the actual MTTF distribution. Actually, when we consider the joint effects of EM and crosstalk then the MTTF distribution shifts towards left in Fig. 6. Hence, incorporation of crosstalk capacitances with workload variation is required for comprehensive analysis of TSV MTTFs and overall reliability.

C. Reliability of 3D NoC with Spare TSV Allocation

The wide variation in TSV MTTF ensues the performance degradation of 3D SWNoC during the execution of any application. In this subsection, the joint effects of workload variation and crosstalk are discussed for allocating the sTSVs to enhance the reliability of 3D SWNoC.

1) Joint Effects of EM and Cc on Spare TSV Allocation

The joint effects from workload-induced stress and crosstalk noise on TSV MTTF also affect the performance of sTSV allocation methodology. To explain this, we consider two cases for the sTSV allocation algorithm outlined in Section IV.D. For the first case, during the allocation, we only consider the effect of workload-induced stress without considering crosstalk, while for the second, the joint effects are considered. The average lifetime improvements of 3D SWNoC with these two cases considering the PARSEC and SPLASH-2 benchmarks mentioned above are plotted in Fig. 7. The improvement in lifetime is normalized with respect to the lifetime of 3D SWNoC without any spare. The two lifetimes are marked as *sTSV_EM* and *sTSV_EM_*C_c respectively.

It is evident that *sTSV_EM_*C_c shows significant lifetime improvement over *sTSV_EM* for any number of spares. Both the *sTSV_EM* and *sTSV_EM_*C_c algorithms explore the TSV with the lowest MTTF and allocate spare to minimize the negative effect of TSV failure. However, *sTSV_EM* only considers workload-induced stress without evaluating any effects from crosstalk capacitance. When we only consider the EM effect arising due to the workload-induced stress then the individual TSVs in a VL are indistinguishable from each other (resistance of each TSV is affected equally by the workload). Consequently, the spare allocation mechanism assigns sTSVs to the whole bundle. This fails to exploit the full benefits of spares as some of the TSVs in the bundle may not require spares

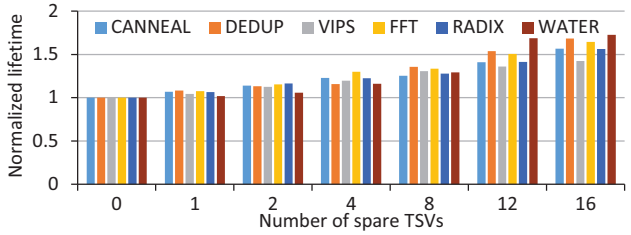

Fig. 8: Lifetime of 3D SWNoC with different number of sTSVs considering the joint effects of workload–induced stress and crosstalk.

(whose MTTFs are comparatively higher, viz. Type 2 and Type 3 TSVs from Fig. 5). Instead of allocating spares to Type 2 and Type 3 TSVs in a highly utilized VL, the spare allocation should assign spares to Type 1 TSV of the next highly utilized VL. In contrast, for *sTSV_EM_C$_c$* allocation, the exact TSV within the VL having the lowest MTTF is identified by exploiting the knowledge of crosstalk capacitance and workload-induced stress. This ensures spare allocation to the most critical TSVs belonging to various VLs rather than allocating spares to all the TSVs in a specific bundle. This strategy ensures the best possible usage of spares and thereby minimizing the adverse effect of TSV failure on the whole NoC. Hence, the *sTSV_EM_C$_c$* performs better than *sTSV_EM* for any spare budget and maximizes the NoC lifetime.

2) *Lifetime Improvement of TSV based 3D NoC*

In this subsection, we analyze how the lifetime defined in (3) of the 3D SWNoC varies with different applications and given spare budgets. Fig. 8 shows the normalized maximum lifetime achieved by varying the number of sTSVs considering the earlier-mentioned SPLASH-2 and PARSEC benchmarks for the 3D SWNoC. The lifetime is normalized with respect to that value of the SWNoC without any sTSV allocation.

From the figure it is seen that as the number of sTSVs increases, the lifetime improvement also increases. For example, with sixteen sTSV, the maximum lifetime improvements achieved for these six benchmarks vary from 43% to 72%. The highest and lowest improvements were observed for WATER and VIPS benchmarks respectively. These improvements are achieved with the *sTSV_EM_C$_C$* spare allocation algorithm (from previous section) considering the joint effects of crosstalk noise and workload-induced stress. If we consider a 64 core system with 48 VLs and 8 TSVs for each VL (using a 4:1 mux for enabling 32-bit fit width), then a budget of 16 sTSVs represents ~5% of the overall TSVs (total 48*8 TSVs). In addition, from Fig. 8, it is seen that this 5% spares can achieve on average 59% lifetime improvement for TSV enabled 3D SWNoC. However, if the joint effects of crosstalk noises and workload-induced stresses are not considered then the lifetime improvement can be reduced significantly (as seen from Fig. 7).

VI. Conclusion

Reliability is a major concern for TSV based 3D NoCs due to nonhomogeneous workload-induced stress in the vertical links. In the presence of crosstalk effects from neighboring TSVs in a bundle, the MTTF of each TSV and the overall lifetime of the NoC degrade further. In this work, we have addressed the combined effects of electromigration arising due to workload-induced stress and crosstalk capacitance on TSV MTTF and hence the lifetime of the 3D NoC. Without considering the crosstalk capacitance, the TSV MTTF and NoC lifetime can be overestimated by at least one order of magnitude. We have also demonstrated that by allowing only a 5% spare TSV budget, the incorporated spare TSV allocation methodology can result in ~59% lifetime improvement of a 3D SWNoC for SPALSH-2 and PARSEC benchmarks considered in this work.

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