Timing-Aware Wire Width Optimization for SADP Process

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***Abstract*—Wire width optimization for SADP process is addressed, which involves a decision of how cut- and block-masks should form; a goal is to reduce wire delay in timing critical paths. The problem is formulated using a graph: a vertex corresponds to wire segment with its maximum length for widening as a vertex weight; an edge represents a potential conflict between two candidate wire segments that we wish to widen. A maximum weight independent set corresponds to an ideal solution. For a few circuits that we test, wire resistance of timing critical nets is reduced by 18.5% on average, which leads to 9.9% reduction in clock period.**

I. Introduction

For sub-7nm node, multi-patterning technology such as litho-etch-litho-etch (LELE) and self-aligned double patterning (SADP) is considered as a patterning solution of choice [1], [2]. SADP involves more processing steps, which is a disadvantage, but enough overlay margin through mandrel process and high resolution make SADP more suitable for fine patterning process. In conventional lithography, a wide pattern cannot be located close to another pattern of 1x pitch due to design rule; this however is allowed in SADP, which is another advantage.

It is well known that reducing wire delay is increasingly important due to the increase in copper resistance with technology scaling while wire capacitance remains relatively unchanged [3]. Adjusting wire width, through for instance progressive wire tapering [5], [6], is one popular method to reduce wire delay. Wire tapering, however, is difficult to implement in SADP process due to the existence of cut- and block-masks.

In this paper, we selectively adjust the width of timing critical wires while we take the design of cut- and block-masks into account. In particular, we selectively widen timing critical wires provided that all wires are initially at minimum width. We show that the problem can be modeled as a graph, in which a vertex corresponds to wire segment (on timing critical paths) with its maximum length for widening as a vertex weight, and an edge indicates a conflict between two candidate wires that are to be widened. A maximum weight independent set corresponds to an ideal solution.

II. Preliminaries

A. SADP Process

Conventional SADP process is illustrated in Fig. 1. For a given main design, mandrel is determined without any conflicting point; self-aligned sidewall spacers are formed by mandrel etch-back; unnecessary parts are removed by using a cut mask; required area to wide patterning is filled by block mask as a post process; finally, the metal wires can be formed with copper. SADP can make uniform and regular patterns following a series of these process. Process variations by lithography or loading effect of etch process can be reduced due to relatively large pattern align margin.

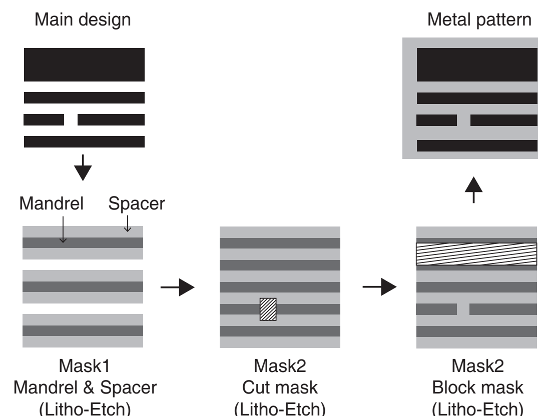

Fig. 1. SADP process.

B. Wire Widening and Limitations

SADP process can create patterns of forbidden pitches in conventional lithography. In general, there is design rule that can not be close to a wide pattern with 1x pitch space due to lithography limitations (Fig. 2(a)). However, in the SADP process, after a regular array pattern is formed, patterns of various widths can be located close to 1x pitch space using a block mask as shown in Fig. 2(b).

With the scaling of technology, the circuit performance can be weaken by process variations on pattern dimensions after design is complete. The degradation of circuit performance can be prevented through wire widening with block mask of SADP process; reduction of wire resistance results in improvement of wire delay. As shown in Fig. 3, the space between two patterns is opened by block mask; then, opened area can be filled using metal material. However, when metal widening is applied to overall chip, the pattern density can be increased and the metal height can be reduced by chemical mechanical polishing (CMP) dishing. Therefore, apply only to the critical path so that the pattern density does not deteriorate and the

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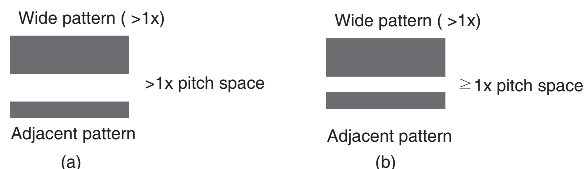

Fig. 2. Wide wire pattern adjacent to another wire (a) should be located with pitch larger than 1x in conventional lithography and (b) can be located with 1x pitch in SADP.

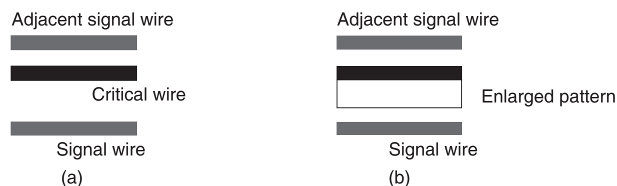

Fig. 3. Metal widening process; (a) before and (b) after metal widening.

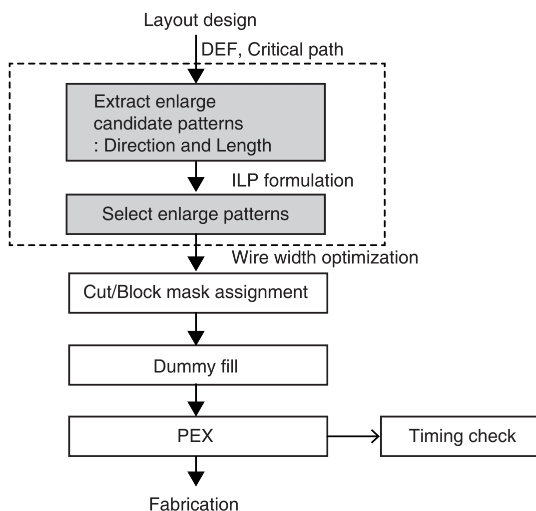

Fig. 4. Overall flow of wire width optimization process.

characteristics are improved. When the metal of critical path is enlarged, some conflicts occur with adjacent signal wires, which is the problem we address.

III. Wire Width Optimization

A. Overall Flow

Overall flow of our wire width optimization process is shown in Fig. 4. The top-k timing critical paths are determined after routing is complete and wires of nets are extracted for the wire widening. For each critical wire, we extract all possible wire widening candidate patterns. We consider the widening direction and also conflicts with other nets and enlarge candidate patterns. We select enlarged patterns so that the sum of enlarged pattern length is maximized. The enlarged patterns are selected by our proposed ILP formulation.

After our wire width optimization, cut for metal isolation and block mask for wide pattern formation can be assigned simultaneously for each metal pattern. We perform wire widening before dummy fill, as additional patterns are added. And then, dummy fill is inserted due to the relocation of cuts.

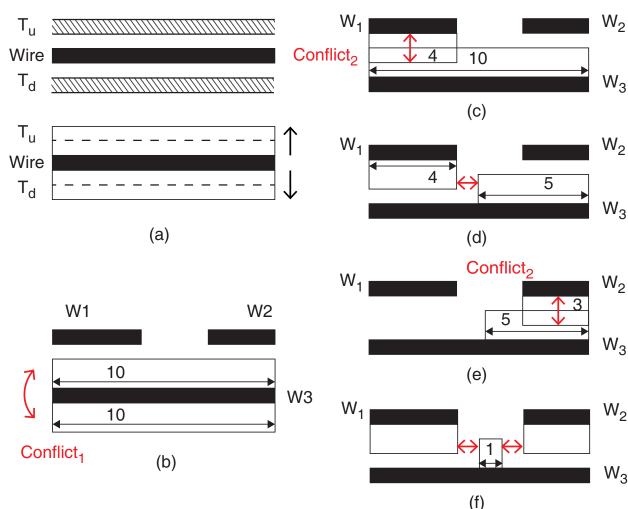

Fig. 5. (a) Critical and adjacent wire on the upper and lower metal track, (b) example of conflict layout to prevent 5x width, and (c)–(f) example of conflict layouts for minimum space rule and also how we create new widening candidate patterns.

We re-extract the RC of interconnects, and check the wire delay reduction by performing static timing analysis (STA).

Wire width optimization for critical paths are performed to maximize the widening length. Enlarged patterns must not overlap with signal nets or other enlarged patterns. They also must satisfy the minimum space rule to prevent the disturbance with adjacent patterns. Based on these conflicts, we first create all possible enlarged pattern candidates. We then create a conflict graph where each edge represents conflict between the two enlarged pattern candidates. We find a maximum weight independent set using an ILP-based formulation.

We assume SADP process is only applied to metal2 and metal3 layer in sub-7nm technology, as these metal layers have larger metal density compared to higher metal layers. For a given layout design, we extract the wire segments of metal2 and metal3 as a DEF file. We find the top-k timing critical paths, and mark the corresponding wire segments.

In Fig. 5(a), we assume there is a wire segment which is part of a critical path. When there is a metal track above the segment, T_u, and a metal track below the segment, T_d, our method can enlarge the wire to T_u or T_d. We define that the wire width after wire widening can only be 3x minimum metal width. If the wire widening uses both T_u and T_d tracks, the 5x minimum metal width segment can be problematic due to weakening caused by CMP dishing (Conflict_1 in Fig. 5(b)).

Since the purpose of our method is to maximize wire widening for critical paths, all possible cases should be considered. For enlarged patterns, various conflict cases are shown in Fig. 5(b), (c), and (e). All enlarged patterns must be formed to avoid signal wire on adjacent tracks whether it is critical net or not. As we mentioned before, wire widening must not create 5x minimum metal width wires. Therefore, we create conflicts between enlarged patterns of the same wire, that will create 5x width wires when selected together.

When the space between two enlarged patterns are not

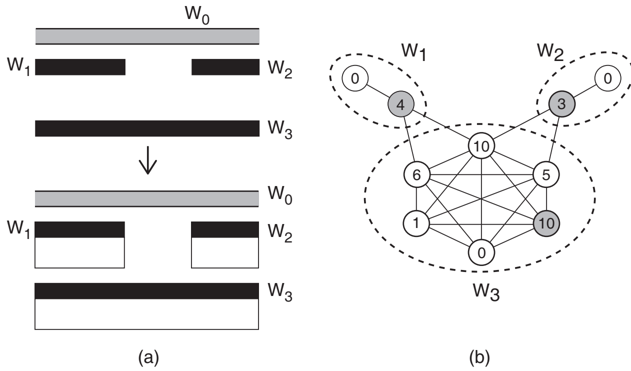

Fig. 6. (a) Original wire and optimal wire widening, and (b) its corresponding conflict graph.

sufficient, the patterns created on the block mask can merge or become a defect particle. Electrically, merging means the two wires will be shorted. Therefore, a minimum space rule exists between enlarged shapes. We create conflicts between enlarged patterns that violate this minimum space rule (Conflict_2 in Fig. 5(b)). This includes patterns that overlap with each other. When conflicts occur between patterns, we create additional enlarged pattern candidates. These are created by finding the enlarged pattern that has maximum length and is conflict-free. For example, when the enlarged pattern of W_1 and W_3 overlap as in Fig. 5(c), we add an enlarged pattern candidate for W_3 that does not overlap with the enlarged pattern of W_1. If we assume minimum space rule is 1 and the length of the enlarged pattern of W_1 is 4, the maximum length the enlarged pattern candidate of W_3 can have is 5 as shown in Fig. 5(d). A conflict occurs between this new enlarged pattern and the enlarged pattern of W_2 in Fig. 5(e). Therefore, we create an additional enlarged pattern candidate for W_3 (length is $5-3-1=1$) as shown in Fig. 5(f).

We find all possible enlarge patterns candidates by first creating enlarge patterns that have the maximum possible length. We then find conflicts between patterns and create additional candidates if required. We continue to check conflicts between all enlarged patterns until no additional candidates are created.

B. ILP Formulation

The objective of the widening process is to maximize the length of enlarged patterns without creating design rule violations similar to Fig. 6(a). To solve this problem, we introduce a graph $G(V,E,w)$ in which each vertex $i \in V$ corresponds to an enlarged pattern or a critical path metal segment. We find all of the possible enlarge patterns using the method describe above. Each vertex has a weight value, which is determined by the length of enlarged patterns (see the numbers in Fig. 6(b)). Each critical path metal segment has a vertex that represents when wire is not enlarged (the weight is therefore 0). We add edges between vertices, if the two vertices have conflicts. This occurs when enlarged patterns create 5x width wires or minimum space rule is violated.

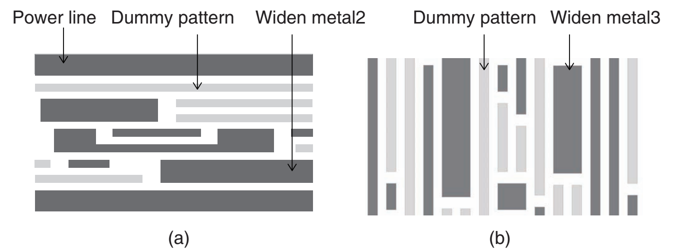

Fig. 7. Layout results of (a) metal2 and (b) metal3 layer after wire width optimization for critical path (test circuit mc).

Edges are also created between the vertices which represent no metal widening and the corresponding enlarged patterns for the segment. If we represent our problem using this conflict graph, the solution is identical to finding the maximum weighted independent set.

We formulate an ILP problem to optimally select the vertices which maximize the enlarged pattern length. Objective of our ILP is to maximize the metal widening of critical paths which we formulate as following,

$$\text{Maximize} \quad \sum_{i \in V} w_i x_i$$

subject to:

$$x_i + x_j \leq 1, \quad \forall e_{ij} \in E$$

For vertex i, w_i represents the vertex weight. x_i is a binary variable that is 1 if i is selected. For each edge e_{ij}, we add a constraint so that only one of the vertices connected by the edge can be selected.

IV. EXPERIMENTAL RESULTS

Wire widening is applied to metal2 and metal3. We perform unidirectional routing on metal2 and metal3 in SADP process. Various test circuits from Open Cores [7] and ITC99 [8] were synthesized using 28 nm industrial library; we assume that metal2 and metal3 layout of 28nm are appropriately shrunk to the layout of sub-7nm design rule. Metal2 and metal3 pitch is 35nm, and corresponding enlarged patterns are implemented the same as metal pitch; which minimum length of metal is complied with sub-7nm design rule. SADP process is assumed with ArF immersion lithography.

To solve the wire widening algorithm, ILP is formulated and our ILP is implemented by using C++ and solved using a commercial solver [9]. Runtime of ILP on all test circuits is less than 10 seconds. We add the selected enlarged patterns to the layout by implementing a Tcl script that is executed on a commercial tool. The dummy fill is inserted with one dimensional array patterns for metal2 and metal3. Afterwards, parasitic extraction and timing check is performed.

A. Pattern Density

The wire widening layout for critical paths of metal2 and metal3 is shown in Fig. 7, respectively. Dummy metal pattern (gray color) were inserted with enough buffer distance not to affect on main circuit. The amount of widen metal2 was relatively small compared to it of metal3 due to regularly

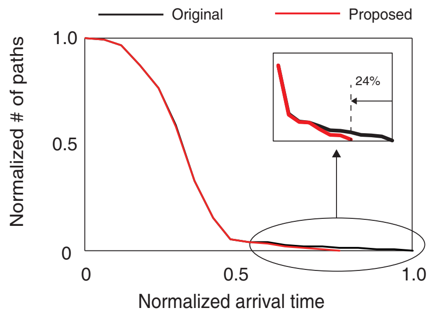

Fig. 8. Cumulative arrival time histogram of ac97 before (Original) and after (Proposed) our wire width optimization.

arrayed power lines, which have wide width and were excluded in wire width optimization.

The variation of pattern density can result in metal height variation by CMP dishing [10]. Since pattern density of metal2 and metal3 can increase after wire widening, we also verify the pattern density. Ideally, the pattern density of metal2 and metal3 can be adjusted during dummy fill insertion to be each respectively around 50% in SADP process. The local pattern density around critical nets was measured to be maximum 55%. In a previous study, 5% density difference was found to have a marginal impact on process variation [10].

B. Timing Assessment

The purpose of our experiment is to reduce the RC delay through the wire widening for critical paths. Table I presents the experimental results for various test circuits. The wire resistance of critical nets is reduced by 18.5% on average, while the wire capacitance is increased by 10.6%. Since the wire width of critical paths were enlarged from 1x to 3x width, the wire resistance were decreased, whereas the wire capacitance increase due to enlarged wires that increase ground capacitance. Coupling capacitance, which consisted 49.6% of the total capacitance in our test circuits, does not change as enlarged patterns simply replace dummy metal patterns and thus the distance between metal shapes are maintained.

The clock period is reduced on average by 9.9%. Fig. 8 shows the cumulative arrival time histogram of a test circuit, ac97, before and after our wire width optimization is performed. The arrival time of primary outputs is normalized to the clock period. We can observe that our wire width optimization method only affects the arrival time of timing-critical outputs. We measure the clock period reduction of applying wire widening on each metal layer. The clock period is reduced on average by 3% when wire widening is applied on metal2, and 7% when applied on metal3.

We also present the wire delay portion of critical nets in Table I. If a circuit has low wire delay portion on critical nets, the clock period reduction can be small even with large resistance reduction, such as test circuits b12 and aes_cipher. Therefore, circuits that have large resistance reduction and large wire delay portions can benefit greatly from our method.

TABLE I
THE WIRE DELAY PORTION OF CRITICAL PATHS, ALONG WITH THE WIRE RESISTANCE, CAPACITANCE, AND CLOCK PERIOD REDUCTION AFTER METAL WIDENING

Circuit	Critical nets			
	Resistance (%)	Cap. (%)	Wire delay portion (%)	Clock period (%)
ac97	-23.8	14.4	84.7	-23.9
aes_cipher	-16.1	7.8	54.6	-4.8
b12	-15.8	13.6	17.1	-2.6
b15	-16.7	13.4	62.2	-8.9
des3	-7.5	11.2	37.4	-7.8
eth	-26.8	8.6	77.4	-10.2
mc	-13.6	7.9	79.8	-7.4
spi	-16.0	13.0	59.7	-6.7
usbf	-17.8	11.6	49.7	-12.0
usfft4_2b	-23.8	7.0	76.9	-14.4
vga_enh	-24.5	8.3	80.6	-10.4
wb_con	-19.0	10.7	73.9	-9.2
Average	-18.5	10.6	62.8	-9.9

V. CONCLUSION

We have proposed a wire width optimization method to improve circuit timing in SADP process. A conflict graph has been constructed from an input metal2 and metal3 of timing critical paths; a maximum weight independent set yields the ideal solution. Our proposed method has been demonstrated in sub-7nm technology using various test circuits. Experimental results have indicated that wire resistance and clock period are reduced by 18.5% and 9.9%, respectively, on average of test circuits.

ACKNOWLEDGMENTS

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