Adaptive Interference Rejection in Human Body Communication using Variable Duty Cycle Integrating DDR Receiver

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***Abstract*— Connected smart wearable devices are becoming increasingly popular with the advent of cheap, miniaturized, ultra-low-power computing and communication. Human Body Communication (HBC) is emerging as an alternative to Wireless Body Area Network (WBAN) for communication among these devices, as it provides higher energy-efficiency and security. One of the biggest bottleneck of HBC is the interference picked up due to the human body antenna effect, with Signal to Interference Ratio often worse than -20dB. An interference robust integrating dual data rate (DDR) receiver is introduced which can adapt itself to changing interference conditions and provide high interference rejection by Pulse Width Modulation of integration clock, thus dynamically changing its duty cycle. The theory, architecture of the receiver is developed along with the adaptation algorithm to train the receiver to find the optimum duty cycle of operation. System-level simulations show >20 dB of rejection even in presence of variable interference frequencies.**

Keywords—Human Body Communication (HBC), Integrating Receiver, DDR, Body Coupled Communication (BCC), Pulse Width Modulation (PWM), Interference tolerance, Adaptive Filter.

I. Introduction

Rapid advancement in miniaturization of unit computing has led to widespread availability of low-cost, tiny form-factor computing units. This has propelled the growth of wearable devices like smart watches, fitness trackers, smart ear phones etc. This growth is expected to continue in the future and soon the average human will have multiple interconnected wearables on his/her body. With everyone carrying a significant amount of information on-body, people will seek to exchange them in a secure manner creating a human body area network (BAN). Such BANs will require energy-efficient and secure ways for these wearable devices to communicate. Human Body Communication (HBC) is potentially a strong alternative to Wireless Body Area Network (WBAN) for wearables as it meets both these requirements. Energy efficiency comes due to the human body showing significantly low loss compared to air for radio frequencies. Also it is easier for an attacker to snoop radio signals from air than from a human body making HBC more secure than WBAN [1].

The idea of HBC for Personal Area Network (PAN) was introduced by Zimmerman in [2]. In this work both the transmitter and receiver have a pair of electrodes and communication takes place via the transmitter *capacitively coupling* a displacement current into the human body, that is picked up by the receiver. In [3] the authors introduce *Galvanic coupling* for HBC. Two electrodes are used to induce current into the human body and two others to measure the potential difference. The primary bottleneck of HBC is due to the human body acting as an antenna in the FM frequency band leading to significant interference. Adaptive Frequency Hopping [4] and fixed narrowband signaling [5] techniques have been used to solve the interference problem. But they suffer from energy inefficiency due to the use of high carrier-frequencies, narrowband-signaling with agility requirements. In [1] the author proposes the use of an Integrating DDR (I-DDR) receiver with NRZ signaling scheme to reject FM interference in HBC, which does not require any filters leading to energy-efficient operation. The received signal is integrated over the symbol period, set to make the integrated interference zero over that duration. This leads to high interference rejection, allowing the receiver to function at signal to interference ratio (SIR) as low as -23dB. However, this puts the constraint on the symbol duration to be an integral multiple of the interference time period to be able to provide maximum rejection. Also, there needs to be a protocol level feedback to the transmitter to change data-rate in case the interference frequency changes. This paper solves this problem by introducing an I-DDR receiver that can adapt to changes in interference frequency, in a self-contained way, by varying the duty cycle of the integrating clock and hence the period of integration to dynamically achieve maximum interference rejection. The proposed receiver does not depend on any relation between the data rate and interference frequency. The theory for this PWM based integrating receiver is developed along with results of performance and closed loop behavior, showing its efficacy for different interference frequencies and SIR conditions.

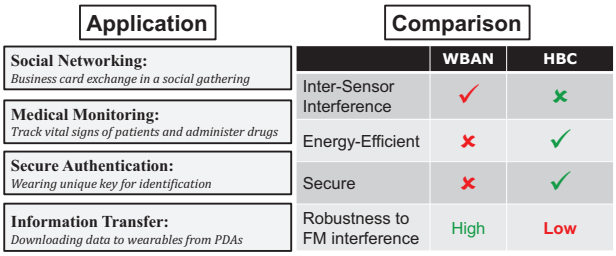

Figure 1: Application of HBC and comparison with WBAN

The rest of the paper is organized as follows, Section II highlights the applications of HBC, with the basic theory of HBC described in Section III, Section IV develops the theory of PWM adaptive HBC and the transceiver structure. Section V presents results with conclusion in section VI.

II. HBC Application

HBC is gaining popularity as it provides several advantages compared to WBAN (Figure 1) as follows: *(1) Energy-*

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efficiency: HBC is energy efficient due to low loss of the human body compared to air and as it is possible to do broadband data transmission without frequency up and down conversion. Utilizing the human body as a broadband channel HBC promises high energy efficiency in the range of tens of pJ/bit [6],[7],[8] significantly lesser than that of wireless transmission (>1nJ/bit [9]). *(2) Inter-Device Interference:* HBC minimizes the interference between devices as the signal is contained within the human body whereas in WBAN, the signal is transmitted through the wireless media interfering the operation of nearby devices. *(3) Security:* HBC benefits from increased security as one has to establish direct contact with the human body to snoop signal which can be done easily from the wireless medium for WBAN. However, the main downside with HBC is that it is limited by interference, as the human body acts as an antenna between 40-400 MHz and FM, walkie-talkie, cordless phone interference falls within this frequency band. The signal level at the receiver side can fall to -50 dBm [10] and the interference from the FM band can be -30 dBm, resulting in a SIR of -20 dB or lower. This paper solves this problem such that HBC can be used for promising applications, as follows:

A. Social networking

With almost everyone having a social and professional digital presence like Facebook or LinkedIn, HBC can be used to exchange social networking requests through smart watches when concerned people shake hands in a gathering.

B. Medical Monitoring

HBC can be used to aggregate and monitor the vital signs of a patient like pulse rate, blood sugar, blood pressure, ECG etc. from wearable/implantable sensors and administer appropriate dosage of drugs depending upon the captured signatures through remote health monitoring.

C. Authentication

Apart from the usual authentication of fingerprint or retinal detection, HBC can add an additional layer of unique identification if the user wears a unique key that can be verified when the user touches the sensor.

D. Information Transfer

Data can be transferred by HBC between Personal Device Assistants (PDA) if users wear a memory device and touch sensors on the PDAs. A user can download the map of a journey to a smartwatch by just touching a PC with fingers.

III. INTERFERENCE ROBUST HBC

The human body acts as a monopole or dipole antenna at frequencies determined by the height of the person. When the human body is not grounded the wavelength is twice the person's height, whereas a grounded body has a wavelength four times the height due to mirror effect [11]. So the resonance frequency of 6ft tall human being is 80MHz or 40MHz depending on whether the body is grounded or not. In actual case due to the lossy nature of the human body the resonance peaking is distributed and the human body behaves like an antenna in the 40-400MHz range [12]. As a result, the human body picks up interference from the omnipresent FM signals (88-108MHz).

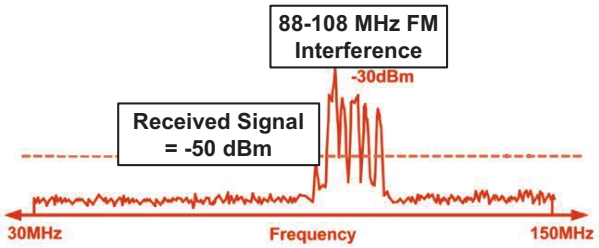

Figure 2: Measured FM interference affecting HBC [1]

Figure 2 shows a sample measurement of the FM interference experienced by the human body [4].

The primary challenge of HBC is to transmit data in conditions where SIR is as low as -20 dB. The authors in [4] suggest using 4 channel Adaptive Frequency Hopping to transmit data only on interference clean channels. [13] uses a Wideband signaling digital transceiver for data transmission. But these techniques require the signal to be modulated to a higher frequency and demodulated from there, creating energy inefficiency. However, in [1] the author uses an NRZ signaling scheme along with an I-DDR receiver to address the problem of signal transmission in the presence of large interference.

A. Theory of I-DDR reciever

The I-DDR receiver takes the integration of the NRZ data + interference over the symbol period (T_b) of data and samples it. After each integration period the integrator is reset for one clock cycle requiring two clock phases to sample alternate data bits; leading to a Dual Data Rate (DDR) receiver.

The received signal (S_{RX}) is a linear superposition of desired NRZ signal (S_{sig}) and the undesired interference (S_{intf}) of frequency ω_i, and can be expressed as follows:

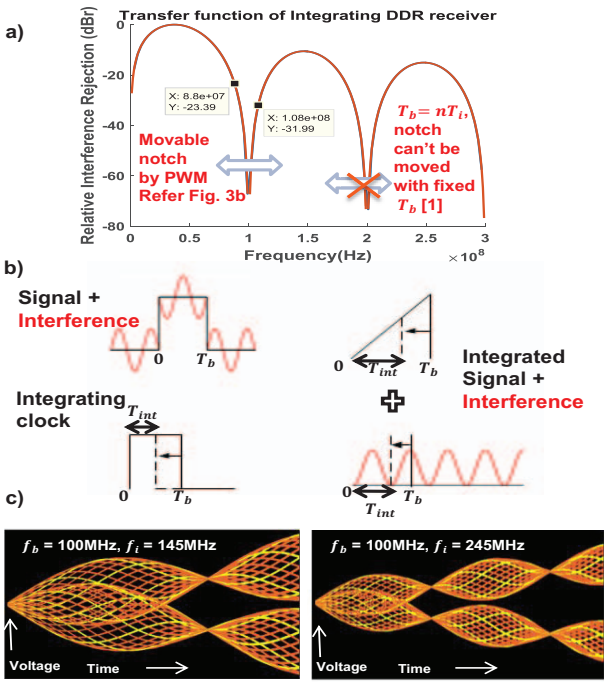

Figure 3: a) Interference suppression for different interferer frequency, for I-DDR receiver ($T_b = nT_i$) [1] b) Movability of notch with clock duty cycle c) Eye diagram showing increase in eye height for particular duty cycles for a particular data and interference frequency combination. These correspond to the optimum duty cycle of operation.

$$S_{RX} = S_{sig} + S_{intf}$$
$$S_{sig}(t) = \pm A_{sig} \quad 0 \le t \le T_b$$
$$S_{intf}(t) = A_{intf}\sin(\omega_i t + \varphi) \quad \forall\, t \qquad (1)$$

The integration of S_{RX} for a duration of T_b, can be written as

$$IS_{RX}(T_b) = IS_{sig}(T_b) + IS_{intf}(T_b)$$
$$IS_{sig}(T_b) = \int_0^{T_b} S_{sig} = \pm K_{int} A_{sig} T_b \qquad (2)$$
$$(K_{int} = integrator\ gain)$$
$$IS_{intf}(T_b) = \int_0^{T_b} S_{intf} = K_{int}\frac{A_{intf}\left[\cos(\varphi) - cos\left(2\pi\frac{T_b}{T_i} + \varphi\right)\right]}{\omega_i} \qquad (3)$$
$$= 0,\ \forall\, T_b = nT_i;\ n = positive\ integer$$
$$IS_{RX}(T_b) = IS_{sig}(T_b),\ \forall\, T_b = nT_i$$

Hence, for *any arbitrary phase* of the interference (φ), its contribution to the integrated signal can be nullified by choosing the data bit period as an integral multiple of the interference time period. This shows that the I-DDR receiver can be used as a notch filter to eliminate the FM interference from HBC, as shown in Figure 3a. In a practical scenario due to jitter it will not always be possible to sample at $t = T_b$; so the contribution from interference will be close to 0.

B. Limitations of the I-DDR reciever

The I-DDR receiver can provide high rejection only if the data symbol period is an integral multiple of interference period. In Figure 3a the null frequencies are at $1/T_b$, $2/T_b$, …, N/T_b; which shows to achieve maximum rejection the data rate is constrained by the interference. Also if there is a change in the interference frequency the receiver will not be able to nullify it while receiving data at a symbol duration decided by the transmitter for nullifying some other frequency.

In this work we propose an I-DDR receiver which can be tuned to reject any interference of no particular relation to the data frequency. The proposed receiver can also automatically adapt to reject a new frequency if there is any change in the interference.

IV. Dynamically Adaptive I-DDR Reciever

A. Variable Notch by PWM

In the I-DDR receiver proposed in [1], the integrating clock duty cycle is fixed at 50% with the integration phase equal to the symbol duration. Here the duty cycle of the clock i.e. the duration of the integration phase is varied to integrate the interference over any time duration T_{int}. The integrated signal and interference is as follows:

$$IS_{sig}(T_{int}) = \int_0^{T_{int}} S_{sig} = \pm K_{int} A_{sig} T_{int} \qquad (4)$$
$$IS_{intf}(T_{int}) = \int_0^{T_{int}} S_{intf} = K_{int}\frac{A_{intf}\left[\cos(\varphi) - cos\left(2\pi\frac{T_{int}}{T_i} + \varphi\right)\right]}{\omega_i} \qquad (5)$$

Let's say duration T_{int} corresponds to duty cycle $d = \frac{T_{int}}{T_{clk}} = \frac{T_{int}}{2T_b}$ and $T_b = kT_i$, where k can be a non-integer also

$$IS_{intf}(T_{int}) = K_{int}\frac{A_{intf}\left[\cos(\varphi) - cos\left(4\pi\frac{dkT_i}{T_i} + \varphi\right)\right]}{\omega_i}$$
$$= K_{int}\frac{A_{intf}[\cos(\varphi) - cos(2\pi(2dk) + \varphi)]}{\omega_i}$$
$$= 0,\ \forall\, dk = \frac{n}{2};\ n = positive\ integer \qquad (6)$$

The following result shows that for any arbitrary combination of data rate and interference frequency maximum interference rejection can be achieved by choosing clock duty cycle (d) as:

$$d = \frac{1}{2k}, \frac{2}{2k}, \ldots, \frac{N}{2k}\ \text{s.t.}\ d \le \frac{1}{2}\ ; k = \frac{T_b}{T_i} \qquad (7)$$

As exemplified by the previous equation, the key idea of the proposed receiver is to vary the duty cycle of the integrating clock and achieve maximum rejection for any arbitrary frequency (Figure 3b). This can be achieved by doing a Pulse Width Modulation (PWM) of the integrating clock. Figure 4 depicts a case where $T_b = 1.5T_i$ and as can be seen from the figure the interference integration over the symbol duration is non-zero (Figure 4d), which is sampled through a 50% duty cycle clock. Whereas for a clock of duty cycle 33.3% the interference contribution at the sampling points will be 0, as can be seen from the plot of the integrated interference.

For a particular ratio between the symbol and interference frequency there may be multiple points where $IS_{intf}(t) = 0$, resulting in high interference rejection. But $IS_{sig}(t)$ is an increasing function of T_{int}, so the point closest to the end of the symbol period where $IS_{intf}(t) = 0$ will have the maximum ratio of $IS_{sig}(t)/IS_{intf}(t)$ (i.e. SIR) leading to best possible interference rejection. Figure 5a shows that the relative interference rejection increases at the null points closer to the symbol period. This information is taken into account in deciding the start and stop points of the training algorithm for the receiver to lock to the best possible duty cycle.

One downside of reducing the integration period is the degradation of the SNR compared to the case where the integration is for the whole symbol duration as in the I-DDR receiver in [1]. But since HBC is generally SIR limited than

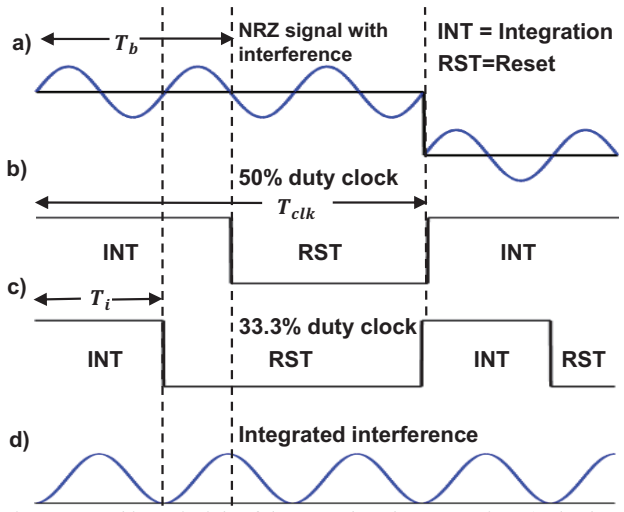

Figure 4: Working principle of the PWM based DDR receiver a) The data signal with the sinusoidal interference superimposed, with $T_b = 1.5T_i$ b) Clock waveform of 50% duty cycle with the integration period equal to the symbol duration c) Clock waveform with 33.3% duty cycle d) Integrated interference with time, which is close to 0 for d=33.3%, not d=50%. Thus d=33.3% clock provides maximum interference rejection

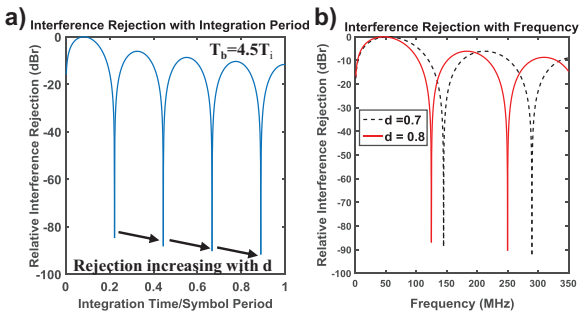

Figure 5: a) Interference suppression as a function of varying integration period, symbol frequency =100MHz, Interference frequency = 450MHz b) Change in null frequencies with duty cycle, symbol frequency =100MHz

SNR limited, this reduction in SNR does not strongly affect the overall system performance. Moreover, the PWM integrated signals still have better SNR than non-integrating systems.

B. Dynamic Adaptation for Correct PWM

From section IV.A it is clear that for a particular interference and data period the optimum duty cycle of operation can be expressed as $d_{opt} = \frac{NT_i}{2T_b}$ s.t. $\frac{NT_i}{2T_b} \leq \frac{1}{2}$ *and* $\frac{(N+1)T_i}{2T_b} > \frac{1}{2}$. But this will require us to determine the interference frequency, so a receiver is developed that can iteratively train itself to find the best duty cycle of operation for a certain interference.

In an eye diagram the eye height is defined as the vertical opening of the eye and gives us a measure about the amount of interference rejection. Higher eye height corresponds to better interference rejection. In the training phase the integrating clock duty cycle of the receiver is changed to find the best eye height. The eye height can be measured by Eye-opening Monitoring architectures; one such example is presented in [14]. The eye height is determined by placing different size masks on the receiver eye diagrams and measuring transition error. The vertical opening of the mask is set by two voltage levels from a DAC. Two different phase clocks created from a phase interpolator determines the sampling points for bit error calculation, which translates to the horizontal opening of the mask. A transition error occurs when the received voltage falls between the voltage levels set by the DAC at any one of the sampling points set by the phase interpolator. The vertical opening of the biggest mask for which the error rate is below a specified threshold determines the eye height.

The algorithm for the best duty cycle selection (*Optimum_duty_search*) does a linear search by varying the clock through PWM and looking at the trend of the measured eye height value. The starting point of the algorithm corresponds to 50% duty cycle clock. This is chosen as the starting point as the null closest to symbol duration has maximum rejection as seen in Figure 5a. In each training cycle the receiver is trained for a particular clock duty cycle with a predetermined large number of samples to have a good measure of the eye height. Between consecutive training cycles the clock duty cycle is reduced by an amount determined by whether eye height is showing an increasing or decreasing trend. In case of a decreasing trend it is reduced by a coarse amount compared to a fine reduction in case of an increasing trend. The algorithm stops when there is a decreasing trend following an increasing trend

Algorithm: Training algorithm to find operating duty cycle
Procedure Optimum_Duty_Search
Output: Optimum duty cycle opt_duty
opt_duty = 0.5 , duty_cycle = 0.5
pres_eye_height = 0, best_eye_height = 0
prev_trend = decreasing, stop_training = 0
repeat
prev_eye_height = pres_eye_height
pres_eye_height = **measure_eye_height** (duty_cycle)
if (pres_eye_height > prev_eye_height)
pres_trend = increasing
if (best_eye_height < pres_eye_height)
opt_duty = duty_cycle
best_eye_height = pres_eye_height
endif
duty_cycle = duty_cycle – fine_duty_change
else
pres_trend = decreasing
duty_cycle = duty_cycle – coarse_duty_change
endif
if (pres_trend == decreasing **&** prev_trend == increasing)
stop_training = 1
elseif (**time_exceeded**)
stop_training = 1
endif
prev_trend = pres_trend
until (stop_training == 0)
endprocedure

denoting that the eye height has reached a peak value, hence the duty cycle corresponds to one of the null points. As can be seen from Figure 5a each null has less rejection as the duty cycle is reduced. So the search is stopped as soon as a peak in the eye height is reached and the corresponding duty cycle is chosen as the optimum if the current eye height is better that of any previously chosen optimum during the training. The algorithm can also be stopped when the duration of training period exceeds a certain time but the optimum duty cycle chosen in that case can be sub optimal.

The update relation of the chosen optimum duty in each iteration of the training can be expressed as follows:

$$d_o(n) = (h_d > h_o)\ ?\ d(n) : d_o(n-1) \qquad (8)$$

Where $d_o(n)$ is the optimum duty cycle at nth iteration, $d(n)$ is the duty cycle for the nth iteration, h_d is the eye height for duty $d(n)$ and h_o is the best eye height chosen so far.

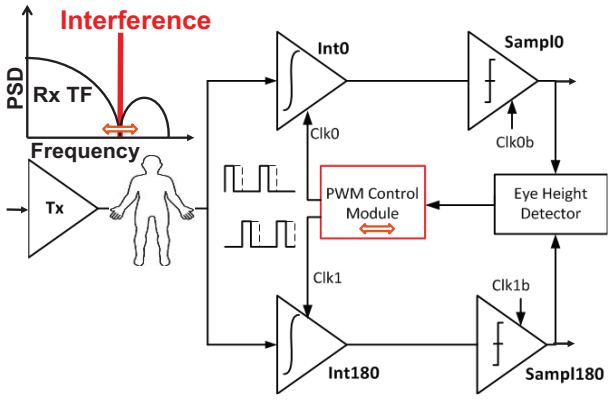

Figure 6: PWM based I-DDR Transceiver diagram

C. PWM based I- DDR HBC Transceiver

The transceiver is shown in Figure 6. The NRZ signal is transferred from the transmitter to the human body by capacitive coupling. The receiver has two paths, each working on 180 degree out of phase clocks. The eye height detection module measures the eye height of the received samples. The duty cycle selection module operates by taking input from the eye height detection module and fixes the duty cycle of the integration clock. The integrated signal is sampled at the end of the integration period. So the sampler runs on an inverted version of the integration clock. After the end of the integration period the integrator enters the reset phase and the next symbol is received by the other integrator and sampler.

V. System Level Analysis and Results

The system is tested with 100Mbps NRZ data under different interference conditions to determine the efficacy of the PWM based I-DDR receiver for interference rejection.

A. Eye height vs. Duty Cycle

Figure 7 shows the variation of eye height with duty cycle of the integrating clock for 3 different interference frequencies. It can be seen that the eye height shows distinct peaks around the duty cycles with maximum interference rejection. It is also evident from Figure 7c that the peak eye heights reduce as the clock duty cycle reduces from 50%.

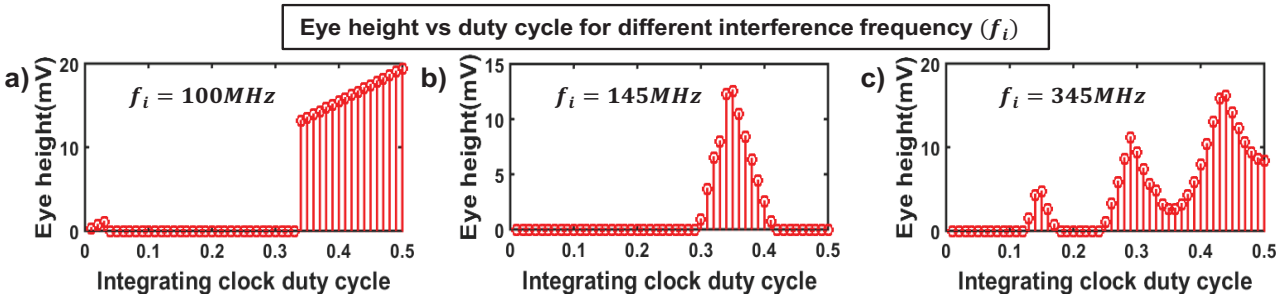

Figure 7: Variation of eye height with duty cycle of integrating clock for SIR = -24.5dB a) Data Frequency = 100MHz, Interference Frequency = 100MHz b) Data frequency = 100MHz, Interference Frequency = 145MHz c) Data frequency = 100MHz, Interference Frequency = 345MHz

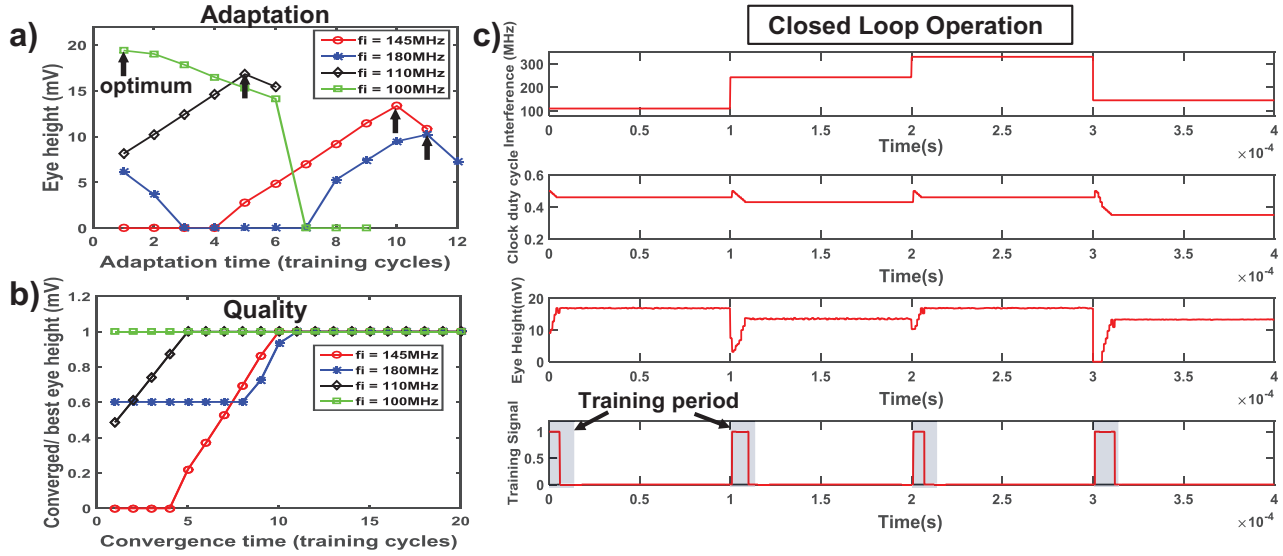

Figure 8: a) Eye height vs Adaptation time plot for different interference frequencies at fixed data frequency = 100MHz b) Quality of solution with time for data frequency = 100MHz and multiple interference frequencies c) Closed loop operation of the receiver at changing interference frequencies, showing how the operating duty cycle changes when the receiver is undergoing training due to frequency change and variation of eye height under different conditions.

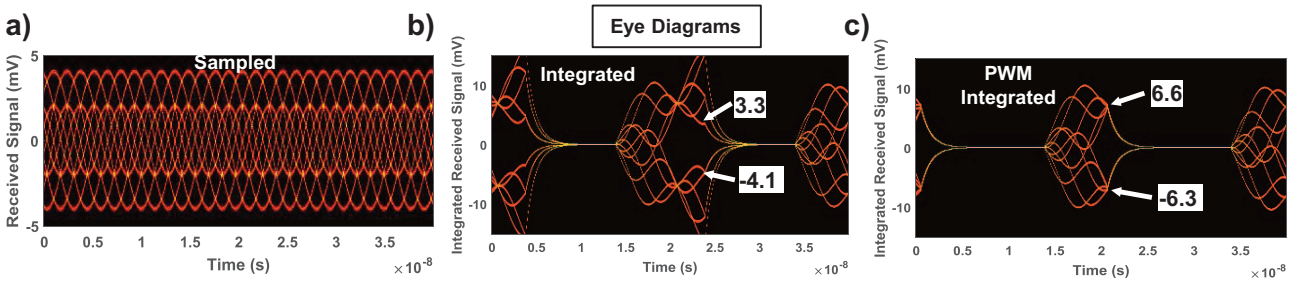

Figure 9: Data frequency = 100MHz, Interference Frequency = 145MHz, SIR = -24.5dB a) Normal Rx eye diagram b) Integrated Rx eye diagram with integration period equal to symbol duration as in I-DDR receiver [1] c) Integrated Rx eye diagram in PWM I-DDR receiver with duty cycle of 0.34 to provide maximum

B. Adaptation time

Figure 8a evaluates the automatic adaptation algorithm by showing how eye height evolves as the receiver is trained for different duty cycles for a particular interference frequency. Each training cycle consists of 5000 symbols which correspond to 50us for a data rate of 100Mbps. Consecutive training cycles differ by 1% (fine) or 3% (coarse) in terms of duty cycle of the clock. For 100MHz case the algorithm stops as the predetermined maximum time limit is exceeded. In all other cases, the training stops at an optimum duty cycle after a peak in the eye height vs duty cycle plot is encountered.

C. Convergence Time vs Quality of Solution

Convergence time is defined as the time given to the receiver to finish its training phase. The quality of solution is the ratio of eye height achieved for a particular convergence time to the best possible eye height achievable for that case. Figure 8b shows that the time required to achieve best solution differs considerably among different interference frequencies (1-12 cycles). The convergence time has to be decided considering the worst case scenario. The training algorithm also ensures that longer convergence time will always lead to better solution.

D. Continuous Operation of the Receiver

Figure 8c shows the continuous operation of the receiver as the interference frequency change with time. Each time there is a change in interference frequency the eye height reduces, and if it falls below a certain threshold compared to the present eye height the receiver enters a training phase of fixed duration. The training finishes when the algorithm finds an optimum duty cycle and locks to it until the next change in frequency. In a practical scenario interference frequency will change as the user moves or there is a change in transmission condition, which will be considerably less frequent than the case shown here for demonstration purposes. In this experiment the frequency is varied more than the FM frequency band to show the operation of the PWM based I-DDR receiver over a broader range.

E. Comparison of eye diagram with and without PWM

Figure 9 shows the comparison of the NRZ eye diagram for a normal receiver, I-DDR receiver with and without PWM capability. The interference frequency and data frequency is taken such that $T_b = 1.45T_i$ with SIR of -24.5dB. Figure 9a shows that the NRZ eye is completely closed. Figure 9b is for the I-DDR receiver without PWM capability showing an eye opening of 7.4mV, less than that of the receiver with PWM capability, operating at optimum duty cycle, having 12.9mV opening as shown in Figure 9c.

F. Rejection for different SIR

Figure 10 shows a comparison of eye height vs duty cycle plot for three different SIR. The eye height peak occurs at the same duty cycle irrespective of the interference strength and it is almost of the same magnitude. This shows that the receiver will be able to reject interference of any magnitude effectively if the proper integration period is chosen. The interference frequency is chosen as 345MHz for this experiment to observe interference independent multiple peaks in the eye height vs duty cycle plot.

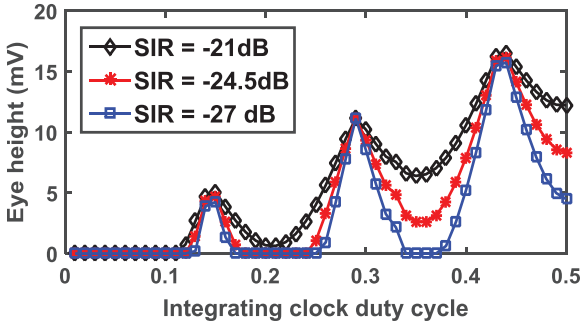

Figure 10: Eye height vs clock duty cycle plot for different SIR, Data frequency =100MHz, Interference frequency = 345MHz

VI. CONCLUSION

The importance of secure, low power communication among wearable devices is on the rise. HBC is a promising alternative to WBAN, but is limited by interference due to human body antenna effect. This work provides theoretical derivation and system level analysis results of an adaptive interference robust broadband Integrating DDR receiver which provides good interference rejection for SIR as low as -27dB and can dynamically adapt to arbitrary interference frequency, at the receiver, without changing data-rate of operation. The performance of he I-DDR receiver in presence of AM and FM interference is similar and will be explored in future work.

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