# High-Density MOM Capacitor Array with Novel Mortise-Tenon Structure for Low-Power SAR ADC

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***Abstract*—The design of capacitor structures have great impact on capacitance density, parasitic capacitance, routability, and matching quality of capacitor network in a SAR ADC, which may affect power, performance, and area of the whole data converter. Most of the recent studies focused on common-centroid placement and routing optimization of the capacitor network. Only few of them investigated the structures of highly integrated capacitors. In this paper, a novel mortise-tenon metal-oxide-metal capacitor structure is proposed, which has the advantages of high capacitance density and small parasitic capacitance. Based on the proposed structure, an integer-linear-programming based capacitor sizing and routing parasitic matching method is further introduced. Experimental results show that the proposed structure and method can achieve the best capacitance density and matching quality of the capacitor network in a SAR ADC.**

## I. Introduction

Successive-approximation-register (SAR) analog-to-digital converters (ADCs) have been one of the most widely used ADC architectures for nowadays demanding applications because of the advantage of lower power consumption. It consists of a comparator, an SAR with control logic, and a capacitor network [1]. The power, performance, and area of a SAR ADC are majorly determined by the following factors, including switching methods of the capacitor network, matching quality among capacitors, and layout structures of a unit capacitor as well as the corresponding parasitics.

According to [2], [3], the layout of capacitor network may contain four kinds of parasitic capacitance, as seen in Fig. 1, which are arising from intrinsic physical structures and/or interconnections within the capacitor network. In Fig. 1, $C^{TB}$, $C^{TS}$, $C^{BS}$, and $C^{BB}$ denote the parasitic capacitance from the top plate to bottom plate of a capacitor, from the top plate of a capacitor to substrate, from the bottom plate of a capacitor to substrate, and from the bottom plate of a capacitor to the bottom plate of another capacitor, respectively. $C^{TB}$ and $C^{TS}$ may have huge impact on linearity/accuracy of a SAR ADC, while $C^{BS}$ and $C^{BB}$ might slightly affect the stability of the reference voltage, $V_{REF}$.

To design an ultra-low-power and highly accurate SAR ADC, most of the recent studies focus on circuit design techniques for saving switching energy of the capacitor network [4]–[8]. Other studies introduce common-centroid placement and routing methods for improving matching quality among capacitors and reducing routing parasitics [2], [3], [9]–[13]. Only few previous work explore different structures of highly integrated capacitors [4], [14], [15]. The capacitor structures may have great impact on *capacitance density*, *parasitic capacitance*, *routability*, and *matching quality* of the capacitor network, and hence it may also greatly affect area, power, and performance of a SAR ADC.

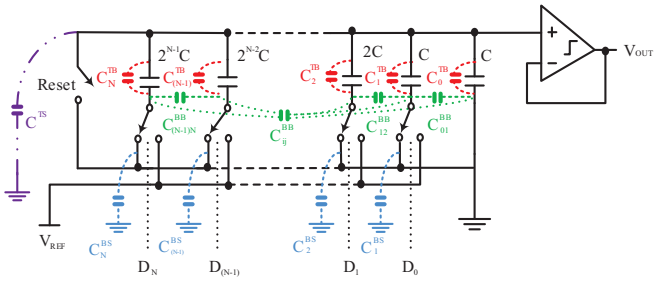


Fig. 1: The comparator and capacitor network of a SAR ADC with layout parasitics [3].

In this paper, we first comprehensively study the most commonly used capacitor structures, specifically for low-power SAR ADCs. In order to achieve even better power, performance, and area of a SAR ADC, we propose a novel mortise-tenon metal-oxide-metal (MOM) structure with the advantages of high capacitance density and small parasitic capacitance compared with all the other capacitor structures. In addition to capacitance density and parasitic capacitance, reliability enhancement, unit capacitor sizing, and other routing issues are also considered when designing the novel structure. Based on the mortise-tenon structure, an integer-linear-programming based capacitor sizing and routing parasitic matching method is further introduced. Experimental results show that the proposed mortise-tenon MOM structure can achieve the best capacitance density and matching quality of the capacitor network in a SAR ADC.

The rest of this paper is organized as follows. Section II introduces the most commonly used capacitor structures and motivates the need of a new structure. Section III presents the novel mortise-tenon structure. Section IV introduces an integrated placement and routing flow with dynamic mortise-tenon sizing. Section V reports the experimental results, and finally Section VI concludes this paper.

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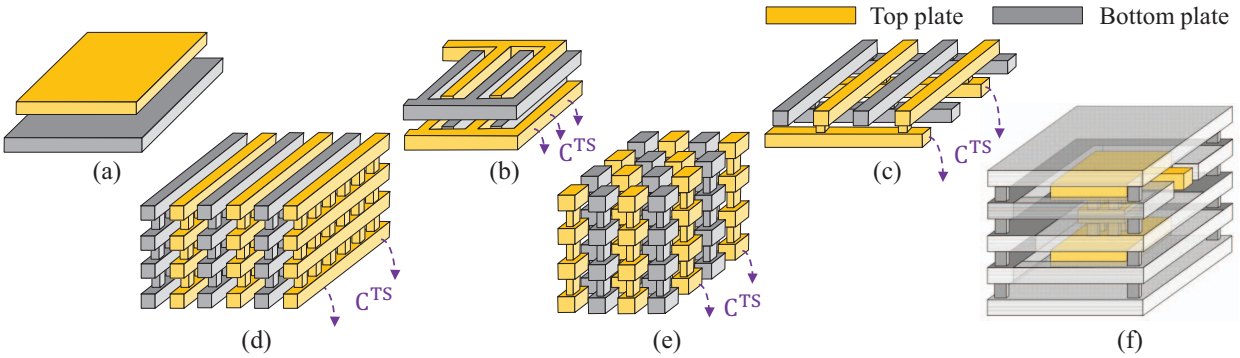



Fig. 2: (a) MIM capacitor. (b) MOM capacitor: interdigitated parallel wires. (c) MOM capacitor: woven. (d) MOM capacitor: parallel stacked wires. (e) MOM capacitor: vertical bars. (f) MOM capacitor: multi-layer sandwich.

## II. Most Commonly Used Capacitor Structures

A metal-insulator-metal (MIM) capacitor is composed of two metal layers and a special dielectric layer between them, as shown in Fig. 2(a). Although it has very small $C^{TS}$, its capacitance density is also quite low resulting in much larger layout area. Moreover, the special dielectric layer of MIM capacitors introduces extra cost because of an additional mask used in fabrication. In order to achieve higher capacitance density with less cost, various structures of MOM capacitors are developed [4], [14], [15], including interdigitated parallel wires, woven, parallel stacked wires, vertical bars, and multi-layer sandwich.

The MOM capacitor with interdigitated parallel wires, as shown in Fig. 2(b), consists of interleaving parallel wires in both lateral and vertical direction. The MOM capacitor with woven structure, as seen in Fig. 2(c), also consists of parallel wires, while the wire directions alternate between 0 and 90 degrees from one layer to another. Both structures takes advantage of all three dimensions of electric field and hence has high capacitance density. The MOM capacitor with parallel stack wires, as shown in Fig. 2(d) consists of metal slabs connected vertically using multiple vias forming vertical plates. It has higher capacitance density with only horizontal electric field due to the thinner separation in the lateral direction as the process technology advances. The MOM capacitor with vertical bars, as shown in Fig. 2(e), are composed of metal bars formed by stacked metal pieces and vias. The capacitance of the VB structure can have considerably high density because it utilizes both x- and y-direction electric field. Nevertheless, the extra routing layers to connect bars may reduce the effective volume. Although all these structures of MOM capacitors have higher capacitance density than MIM capacitors, the top-plate-to-substrate capacitance, $C^{TS}$, is too large to be applied to the capacitor network in a SAR ADC.

In order to reduce $C^{TS}$, Liu et al. [4] introduced a new structure of MOM capacitors, called multi-layer sandwich, as shown in Fig. 2(f), which uses bottom plate metals to enclose all top plate metals. However, the full enclosure of top plates causes reduction of density and difficulty when connecting all top plates of the capacitor network in a SAR ADC.

TABLE I: Comparison of density and top plate to substrate parasitic capacitance $C^{TS}$ for the MIM capacitor and MOM capacitor with the structures of interdigitated parallel wires (IPW), woven, parallel stacked wires (PSW), vertical bars (VB), and multi-layer sandwich (MLS).

| Structure | MIM | IPW | Woven | PSW | VB | MLS |
|---|---|---|---|---|---|---|
| Density | Low | Medium | Medium | High | High | Medium |
| $C^{TS}$ | Small | Large | Large | Large | Large | Small |
| Routibility | High | Medium | Medium | Medium | Low | Medium |

A summary of the aforementioned MIM and MOM capacitor structures is shown in Table I. Although MIM and multi-layer sandwich MOM capacitors have the smallest $C^{TS}$, we observed that their capacitance density and/or routability can still be further improved. Therefore, it is desirable to investigate new capacitor structures for achieving high capacitance density and high routability while maintaining very small $C^{TS}$.

## III. Novel Mortise-Tenon Structure

Inspired by mortise and tenon originally for joining wood pieces, the proposed mortise-tenon structure capacitor consists of a top plate tenon tongue and a bottom plate mortise hole as shown in Fig. 3(c). The idea behind this structure is to reduce top-plate-to-substrate parasitic capacitance $C^{TS}$ without compromising capacitor density. The development of the unit capacitor structure and the method for sizing a unit capacitor are discussed in the following subsections.

### A. Development of Unit Capacitor

*1) Reduction of Parasitic Capacitance:* A basic mortise-tenon structure without special considerations is shown in Fig. 3(a). The edge of topmost layer of the tenon is aligned with the outer surface of the mortise. This causes larger fringing parasitic capacitor from top plate to substrate, a.k.a. $C^{TS}$. To reduce this parasitic capacitance, we shall shrink the size of the tenon top layer to an extent that the top plate to substrate parasitic capacitance becomes zero after parasitic extraction and simulation using a commercial tool. A unit capacitor with parasitic reduction is shown in Fig. 3(b).

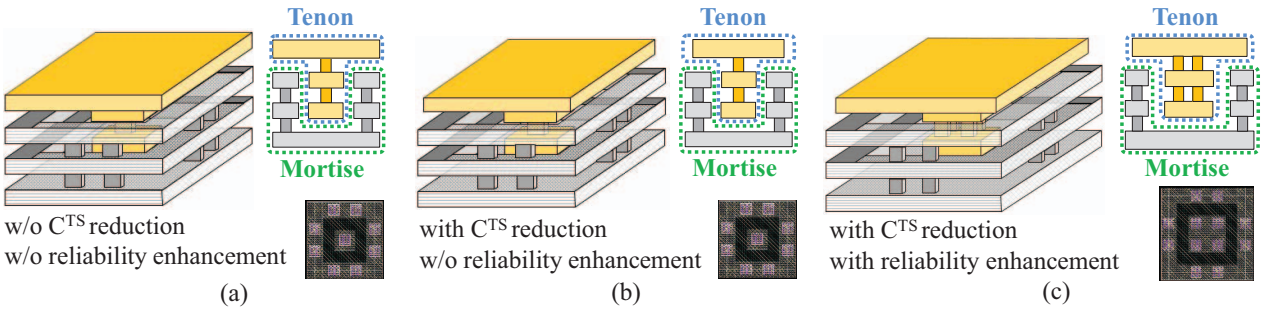



Fig. 3: The proposed mortise-tenon structure, (a) without parasitic reduction and reliability consideration, (b) with parasitic reduction but without reliability consideration, and (c) with both parasitic reduction and reliability consideration.

TABLE II: Comparison of unit capacitor characteristics for MIM, multi-layer sandwich (MLS) MOM [4], and mortise-tenon MOM capacitors. (All unit capacitors are of minimum area according to design rules of the TSMC 180 $nm$ process.)

| Structure | MIM | MLS [4] | Mortise-Tenon |
|---|---|---|---|
| Capacitance (fF) | 20.28 | 2.59 | 1.40 |
| Area ($\mu m \times \mu m$) | 8.80×8.80 | 3.33×3.33 | 2.22×2.22 |
| Metal layers | M5–M6 | M1–M5 | M1–M5 |
| Density (fF/$\mu m^2$) | 0.262 | 0.233 | 0.283 |
| $C^{TS}$ (fF) | ≈ 0 | ≈ 0 | ≈ 0 |

*2) Reliability Enhancement:* For reliability concerns, four vias instead of one for each layer are used for the tenon tongue in our implementation, as shown in Fig. 3(c). Compared with the multi-layer sandwich structure [4] based on the TSMC 180 $nm$ process, a unit capacitor based on the proposed mortise-tenon structure not only has negligible $C^{TS}$ but also higher capacitor density, as demonstrated in Table II, where the capacitance and $C^{TS}$ of each structure are extracted by a commercial tool.

### B. Sizing Unit Capacitors

Sizing a mortise-tenon MOM capacitor is different from sizing traditional MIM capacitors because the density of unit capacitors may change. For traditional MIM capacitors, the value of a capacitor is proportional to the area of horizontal plates due to the sole existence of vertical electric field. However, for mortise-tenon MOM capacitors, lateral electric field also contributes to capacitance. Therefore, a new effective sizing method is necessary.

Two sizing methods, single-tenon sizing method and multiple-tenon sizing method, are presented and compared. The single-tenon sizing method, as illustrated in Fig. 4(a), sizes up a capacitor by increasing the volume of its tenon tongue horizontally. Fig. 4(c) presents the resulting layout of a sized unit capacitor after applying this method. The multiple-tenon sizing method sizes up a capacitor by duplicating single capacitors and merging adjacent mortise walls. Fig. 4(b) illustrates the structure of a sized-up unit capacitor and Fig. 4(d) shows the layout of a unit capacitor after sizing up horizontally and vertically with the multiple-tenon sizing method.

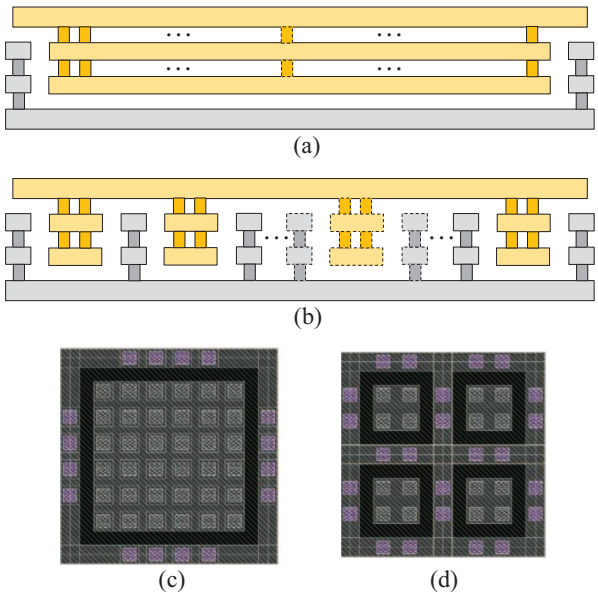



Fig. 4: (a)(c) Cross section and layout of a sized unit capacitor with a single large tenon. (b)(d) Cross section and layout of a sized unit capacitor with multiple small tenons.

The chart in Fig. 5 compares the capacitance growth based on the aforementioned sizing methods. As the unit capacitor sizes up, the capacitance density increases slightly with the multiple-tenon sizing method, while that decreases with the single-tenon sizing method. Therefore, the multiple-tenon sizing method is adopted in the SAR ADC application.

## IV. Common-Centroid Capacitor Placement and Routing with Dynamic Mortise-Tenon Sizing

### A. Common-Centroid Capacitor Placement and Routing

When placing and routing the capacitor network in a SAR ADC, the objective is to minimize systematic mismatch and random mismatch caused by process variation. We adopt the method in [3] to obtain a compact placement and detailed routing result with low capacitance mismatch. It starts with first applying the simulated annealing placement optimization and bipartite-matching trunk wire planning method introduced

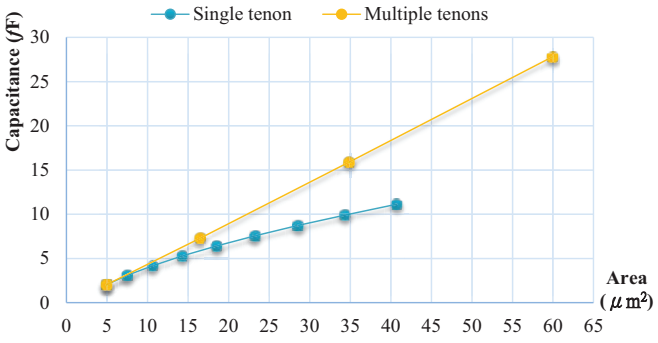



Fig. 5: Comparison of capacitance when sizing up a mortise-tenon unit capacitor with single tenon and multiple tenons.

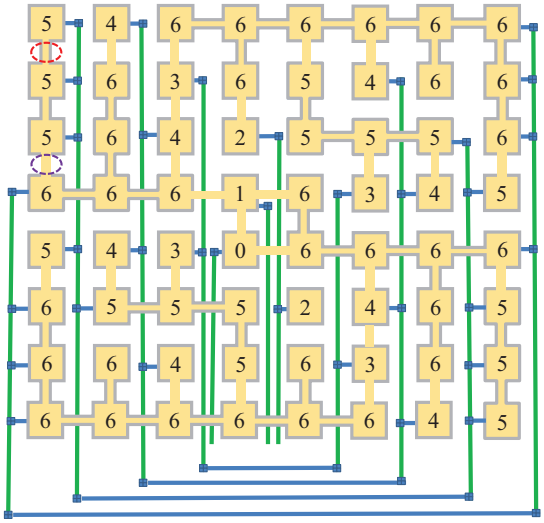


Fig. 6: Stick diagram layout of a common-centroid unit capacitor array in a 6-bit SAR ADC generated using the placement and detail routing method in [3]. The dashed circles show different top and bottom plate routing patterns.

in [2]. After acquiring the unit capacitor and trunk wire positions, a detailed router [3] will handle bottom plate routing using a connected-component algorithm. The bottom plate routing results consisting of a set of routed bottom plate islands are then transformed to a graph for the minimum-spanning-tree algorithm to find the shortest top plate routing. The generated layout for the capacitor network of a 6-bit SAR ADC is shown in Fig. 6. The dashed circles in Fig. 6 represents two types of layout patterns, which will be discussed in the next section.

### B. Dynamic Capacitor Sizing and Parasitic Matching

*1) Routing Patterns and Parasitic Capacitance:* Lin *et al.* [3] introduced three types of routing patterns, including overlap, non-overlap and single, as seen in Figs. 7(a), (d) and (e), respectively, and applied the genetic algorithm to minimize unit capacitor size and match routing parasitic by alternating routing patterns. For our mortise-tenon structure, the bottom plate routing has the flexibility to move among different layers, as shown in Figs. 7(a), (b) and (c). This flexibility provides more opportunities to match the induced parasitic capacitance for each ratioed capacitor.

Since the overlap patterns with different bottom plate layers provide sufficient varieties of capacitance to adjust capacitance ratio, the non-overlap pattern in Fig. 7(d) is not necessary in our mortise-tenon structure. With advanced process technologies, the dimensions of a unit capacitor also become too small to allow a non-overlap pattern.

*2) Progressive ILP Formulation for Capacitor Sizing and Parasitic Matching:* With different layers of bottom plate routing for different overlap patterns, we can fine-tune the capacitance ratio among different capacitors in a SAR ADC. Instead of applying the genetic algorithm, we formulate the problem of capacitor sizing and parasitic matching as an integer linear programming (ILP) problem. Given an $n$-bit SAR ADC capacitor network, a process technology with $N$ metal layers, and common-centroid placement and routing resulting from Section IV-A, the objective of our ILP formulation is to make the ratio of each capacitor $C_i$ closest to the ideal ratio $R_i$. Based on the common-centroid placement and routing result, the number of overlap routing patterns $P_{overlap}^{C_i}$ of each capacitor $C_i$ is available. Let ${}^{l}p_j^{C_i}$ be a binary variable which indicates that the overlap pattern in layer $l$ is selected for the $j$-th bottom-plate wire connection for $C_i$ when its value is one. The mathematical formulation is shown as follows.

$$min \sum_{i=0}^{n} \left( \widetilde{C}_i - R_i \cdot \widetilde{C}_{unit} \right)$$

$$s.t. \sum_{l=1}^{N-1} {}^{l}p_j^{C_i} = 1$$

$$\forall \{(i,j) | i = 1,2,...,n; j = 1,2,...,P_{overlap}^{C_i}\}.$$

$\widetilde{C}_{unit}$ is a slack variable to dynamically adjust the desirable unit capacitance based on available mortise-tenon structures after multiple-tenon sizing. $\widetilde{C}_i$ is the estimated capacitance calculated by adding up the simulated capacitance of each unit capacitor in $C_i$ with the routing wires parasitic capacitance according to their routing patterns. That is,

$$\widetilde{C}_i = \sum_{j=1}^{P_{overlap}^{C_i}} \sum_{l=1}^{N-1} \left( C_i + C_{overlap,l}^{TB} \cdot {}^{l}p_j^{C_i} \right), \qquad (1)$$

where $C_i$ is the simulated unit capacitor value and $C_{overlap,l}^{TB}$ is the parasitic capacitance for the overlap pattern in different layers, as shown in Figs. 7(a), (b) and (c).

In case the ratio of all capacitors does not pass the minimum requirement of differential nonlinearity (DNL) and integral nonlinearity (INL) (within $\pm 0.5$ LSB), the ILP optimization is called again and the size of each unit capacitor is increased using the multiple-tenon sizing method. Each time when unit capacitors are sized up, the width and height of each unit capacitor are enlarged by one unit. For example, from first iteration to second iteration a unit capacitor layout is changed from that in Fig. 3(c) to Fig. 4(d). This progressive sizing loop ends when the DNL and INL requirements are met.

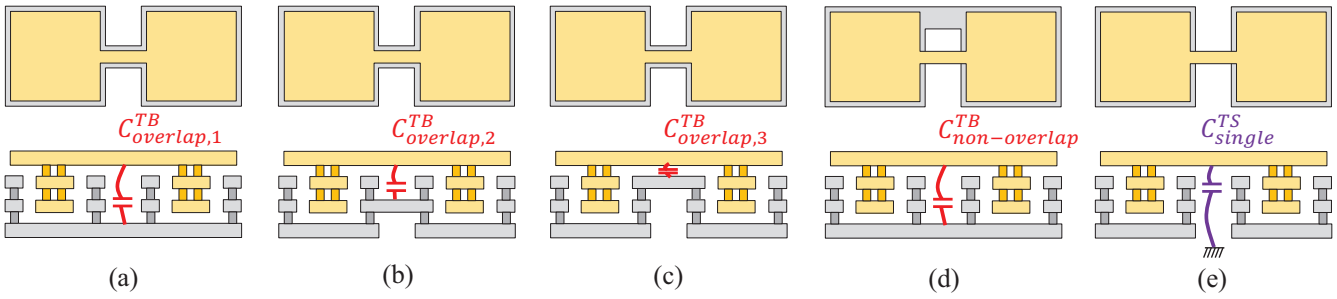



Fig. 7: Routing patterns between two adjacent unit capacitors in a capacitor array. (a)(b)(c) Overlapped top plate and bottom plate routing wires with different metal layers of the bottom plate routing wire. (d) Non-overlapped top plate and bottom plate routing wires. (e) A single top plate routing wire when the two unit capacitors belong to different capacitors in a SAR ADC.

## V. Experimental Results

Our automatic layout generation and sizing method for the capacitor network in a SAR ADC was implemented with C++ programming language and performed on an Intel Xeon 16-core CPU@2.4GHz machine with 48GB Memory. Six sets of binary weighted capacitors for SAR ADCs ranging from 6 to 10 bits are used as benchmarks for experiments based on the TSMC 180 $nm$ process. The basic information of the benchmarks is presented in Table III. The structure and routing of MIM capacitors based on [3] require two and three metal layers, respectively. In order to utilize the most metal layers based on the TSMC 180 $nm$ process for the proposed mortise-tenon MOM capacitors, five metal layers are used not only for the structure itself but also for routing. We first compare the area, DNL, INL, and power consumption resulting from [3] with MIM capacitors and those resulting from our method with the proposed mortise-tenon MOM capacitors. The results are shown in Table IV. It can be seen that both approaches can reach the acceptable DNL, INL range, $\pm 0.5$ LSB, while ours achieves 67% smaller unit capacitors in average, and thus occupies a 71% smaller area, and consumes 33% less power. The runtime for the largest circuit is only within few seconds. The final layouts of the capacitor network in a 9-bit SAR ADC resulting from [3] and our approach are compared in Figs. 8(a) and (b), respectively.

TABLE III: The benchmark circuits.

| Circuit | # of Cap. | Capacitor Ratio | # of Unit Cap. |
|---|---|---|---|
| SAR_ADC_6b | 7 | 1 : 1 : 2 : 4 : 8 : 16 : 32 | 64 |
| SAR_ADC_7b | 8 | 1 : 1 : 2 : 4 : 8 : 16 : 32 : 64 | 128 |
| SAR_ADC_8b | 9 | 1 : 1 : 2 : 4 : 8 : 16 : 32 : 64 : 128 | 256 |
| SAR_ADC_9b | 10 | 1 : 1 : 2 : 4 : 8 : 16 : 32 : 64 : 128 : 256 | 512 |
| SAR_ADC_10b | 11 | 1 : 1 : 2 : 4 : 8 : 16 : 32 : 64 : 128 : 256 : 512 | 1024 |

When comparing with the multi-layer sandwich structure, since [4] does not provide both automatic sizing method and layout automation flow, we were not able to reproduce the layout for detailed comparison. However, according to the placement of the capacitor array provided in [4], as seen in Fig 9(a), we could still compare the systematic mismatch (M) and spatial correlation coefficient (L) with our result based the same capacitor network. The metrics of both M and L are given in [9]. According to the respective M, L values presented in Figs 9(a) and (b), the proposed mortise-tenon structure can result in a better placement with less systematic mismatch and more spatial correlation (i.e. higher dispersion), while both routability and circuit performance are still guaranteed. Consequently, the generated layouts using our mortise-tenon structure will be more resistant to process variation.

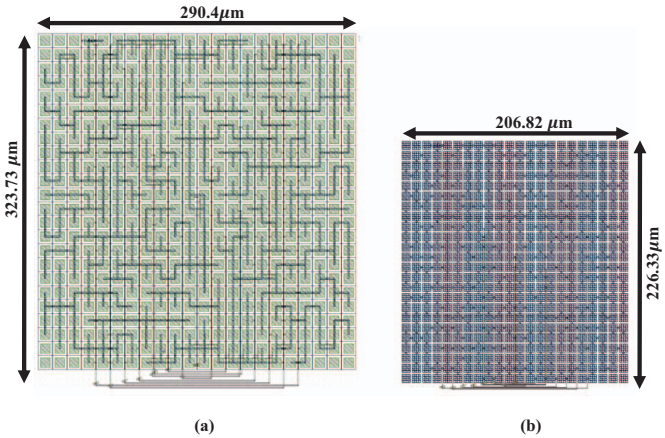


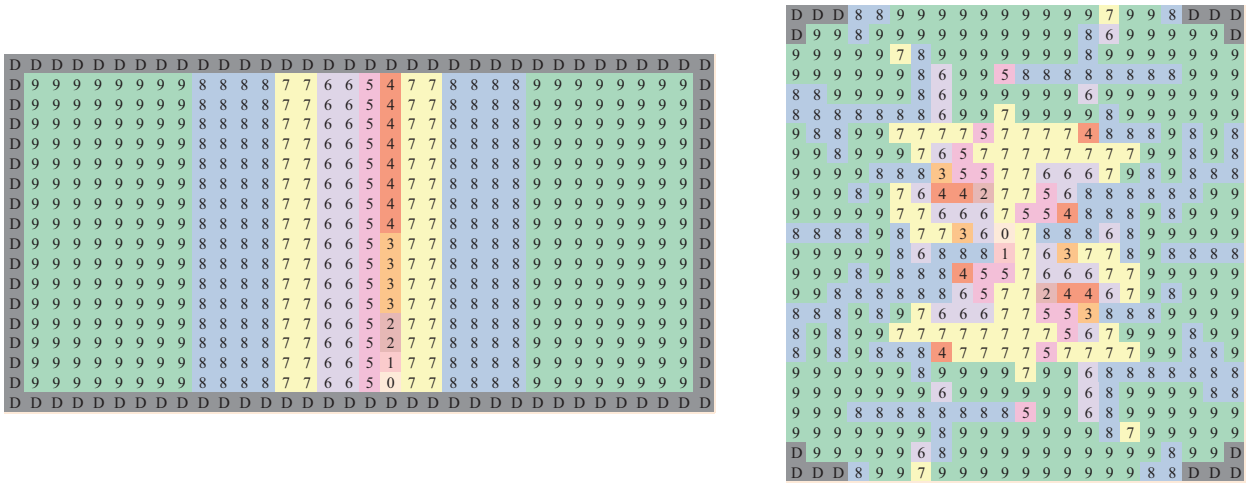

Fig. 8: The layouts of the capacitor network in a 9-bit SAR ADC based on (a) the approach in [3] with MIM capacitors, and (b) our approach with mortise-tenon MOM capacitors.

## VI. Conclusions

In this paper, we have comprehensively studied the most commonly used capacitor structures. To achieve even higher capacitance density and smaller parasitic capacitance for better area, performance, and power consumption of a SAR ADC, we have further proposed a novel mortise-tenon structure together with a new dynamic capacitor sizing and parasitic matching method. Experimental results have shown that the proposed mortise-tenon MOM structure can achieve the best capacitance density and matching quality of the capacitor network in a SAR ADC.

TABLE IV: Comparison of unit capacitance, total layout area of the capacitor array, maximum absolute DNL and INL, and power consumption of the capacitor network in each SAR ADC based on Lin *et al.*'s approach with MIM capacitors [3] and our approach with mortise-tenon MOM capacitors.

| Circuit | Lin *et al.*'s approach with MIM capacitors [3] | | | | | Our approach with mortise-tenon MOM capacitors | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Name | $C_{unit}$ ($f$F) | Area ($\mu m^2$) | DNL$_{max}$ (LSB) | INL$_{max}$ (LSB) | Power ($n$W) | $C_{unit}$ ($f$F) | Area ($\mu m^2$) | DNL$_{max}$ (LSB) | INL$_{max}$ (LSB) | Power ($n$W) |
| SAR_ADC_6b | 28 | 7077.60 | 0.211 | 0.363 | 45.63 | 7.29 | 2195.16 | 0.117 | 0.480 | 35.69 |
| SAR_ADC_7b | 39 | 19201.52 | 0.263 | 0.357 | 56.96 | 15.88 | 8234.69 | 0.220 | 0.342 | 47.21 |
| SAR_ADC_8b | 51 | 37579.66 | 0.132 | 0.403 | 82.34 | 15.88 | 14997.01 | 0.050 | 0.494 | 50.98 |
| SAR_ADC_9b | 73 | 94011.19 | 0.137 | 0.212 | 112.60 | 27.79 | 46808.54 | 0.218 | 0.350 | 67.46 |
| SAR_ADC_10b | 100 | 275727.71 | 0.297 | 0.189 | 137.55 | 27.79 | 104402.21 | 0.239 | 0.451 | 73.05 |
| Comparison | 1 | 1 | | | 1 | 0.33 | 0.29 | | | 0.67 |



M=8.161, L=31.284

(a)

M=1.179, L=36.990

(b)

Fig. 9: Comparison of two different placements of the capacitor network in a 9-bit SAR ADC, as well as the corresponding systematic mismatch (M) and spatial correlation (L). (a) The placement given in [4]. (b) The placement based on our approach.

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