Flying and Decoupling Capacitance Optimization for Area-Constrained On-Chip Switched-Capacitor Voltage Regulators

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***Abstract*— Switched-capacitor voltage regulators (SCVRs) are widely used in on-chip power management, due to high step-down efficiency and feasibility of integration. In this work, we present theoretical analysis and optimization methodology for flying and decoupling capacitance values for area-constrained on-chip SCVRs to achieve the highest system-level power efficiency. The proposed models for efficiency and droop voltage are validated with on-chip 2:1 SCVR implementations in both 65nm and 32nm CMOS, which show high model accuracy. The maximum and average error of the predicted optimal ratio between flying and decoupling capacitance are 5% and 1.7%, respectively.**

Keywords*— Switched-capacitor voltage converter; integrated voltage regulator; power conversion efficiency; voltage droop; capacitance optimization; area-constrained power management.

I. INTRODUCTION

On-chip power management has become increasingly important in modern processor designs for the pursuit of fine-grain dynamic voltage scaling, fast load regulation, and simpler board design. Buck converters have been widely used in portable devices for their high power efficiency, but lack of high-quality on-chip inductors has limited on-chip integration [1]. Linear regulators [2] exhibit linear dependence of efficiency on the input and output voltages, which makes it unfavorable for high step-down conversion. In comparison, SC voltage converters can offer a fully integrated solution with high-quality on-chip capacitors at integer conversion ratios [3-4]. Furthermore, recently proposed designs with binary and rational SC conversion ratios have largely enhanced the efficiency for a wide range of output voltages [5].

Theoretical analysis on efficiency and optimization of SC voltage converters have been conducted in prior works [6-10]. The output impedance models of fast and slow switching loss conditions for different SC conversion topologies were presented in [6]. In [7], the gate capacitance loss and CMOS capacitor bottom-plate loss were analyzed and optimized. The authors of [8] derived the output resistance and analyzed the switch width and frequency for optimal efficiency in SC voltage converters. Regulation analysis of high-power SC voltage converters is performed in [9] using a charge-balance transient-calculation modeling method, however closed-form analysis of droop voltage against abrupt load transients has not been presented. The trade-off of using flying and decoupling capacitance was analyzed in [10], but an integrated analysis considering both efficiency and droop was not presented.

Most standalone SCVRs in the literature are not designed with specific area constraints. While power densities are reported, decoupling capacitance are often not included in the overall reported area. However, in practical scenarios of SCVRs being employed in processors or embedded systems, strict area constraint usually exists, and the area of the SCVR plus the area of input/output decoupling capacitance need to fit in a given real estate. Considering that most of the SCVR area is devoted to capacitance [3-4], selection of appropriate flying capacitance versus decoupling capacitance directly affects the conversion efficiency, output current, and output droop voltage against load transients. The capacitors in SCVRs that will be investigated in this work are illustrated in Figure 1. Integrating the effects of both efficiency and output droop into system-level power, we present an area-constrained analysis and optimization of flying and decoupling capacitors in on-chip SCVRs.

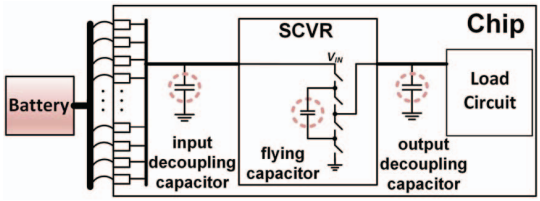

Figure 1. Illustration of the flying and decoupling capacitors in an on-chip SCVR that is connected from a battery.

II. ANALYSIS AND OPTIMIZATION OF AREA-CONSTRAINED SCVR

In this section, we present the efficiency model and droop model of SCVRs. We focus on 2:1 SC converters due to its prevalence in high-efficiency SCVR designs [3], and their use in state-of-the-art binary and rational-ratio SC converters [5].

A. Analysis of Conversion Efficiency and Output Current

The efficiency and power density of SC voltage converters are directly affected by the capacitor technology of the CMOS process, besides conversion ratio and topology. The sources of power loss in SC voltage converters include the following [6-8]:

(1) charging and discharging behavior of the flying capacitor causes slow switching loss (SSL) at the output, which is inversely proportional to the switching frequency and flying capacitance and is set by:

$$P_{SSL} = \frac{I_L^2}{N_{SSL} f_{sw} C_{fly}}, \quad (1)$$

where I_L is the load current of the SC converter, f_{sw} is the switching frequency, and C_{fly} is the flying capacitance. N_{SSL} is the coefficient depending on SC converter topology and $N_{SSL} = 4$ for a 2:1 SC converter.

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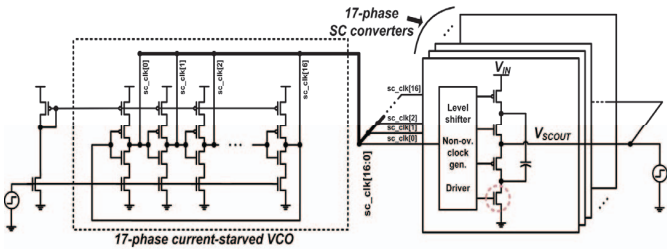

Figure 2. Schematic of SC voltage regulator used for droop analysis against load transients.

(2) current through the on-resistance of the non-ideal switches results in fast switching loss (FSL), which is set by:

$$P_{FSL} = I_L^2 \frac{R_{on}}{W_{sw}} N_{FSL}\,, \tag{2}$$

where W_{sw} is the switch width of the SC converter, and R_{on} is the on-resistance of the switch determined by the CMOS process. N_{FSL} is the coefficient depending on SC converter topology and $N_{FSL} = 2$ for a 2:1 SC converter.

(3) parasitic capacitance of the flying capacitor causes bottom-plate loss, which is proportional to the total bottom plate capacitance as well as the switching frequency and is set by:

$$P_{bott} = N_{bott} V_o^2 C_{bott} f_{sw}\,, \tag{3}$$

where N_{bott} is the number of bottom plates, C_{bott} is the bottom-plate capacitance, and V_o is the SC converter output voltage.

(4) parasitic capacitance of the SC switches causes switching loss due to its charging and discharging behavior, which is proportional to both switch width and frequency and is set by:

$$P_{sw} = k_{drive} N_{sw} C_{sw} V_{sw}^2 f_{sw}\,, \tag{4}$$

where k_{drive} is the constant of proportionality accounting for the pre-drivers [8], C_{sw} is the parasitic capacitance of the switch, N_{sw} is the number of switches that is conducting, and V_{sw} is the supply voltage of the driver stages.

The total power loss of a SC converter is the sum of the four aforementioned loss terms:

$$P_{loss} = \frac{I_L^2}{N_{SSL} f_{sw} C_{fly}} + I_L^2 \frac{R_{on}}{W_{sw}} N_{FSL} + V_o^2 C_{bott} f_{sw} + k_{drive} N_{sw} C_{sw} V_{sw}^2 f_{sw} \tag{5}$$

The optimal conversion efficiency for different load currents with a given flying capacitance can be determined with the minimization of P_{loss} by varying switching frequency and switch width of the SC converter:

$$\eta_{opt} = \left(1 + \frac{P_{loss\_min}}{P_{load}}\right)^{-1}, \tag{6}$$

where P_{loss_min} is the minimum value of P_{loss} for a given load current and flying capacitance, and P_{load} is the output power:

$$P_{load} = V_o I_L \tag{7}$$

Using the 'fmincon' optimization function in Matlab, the minimum power loss P_{loss} is determined with interior-point algorithm for various load currents and flying capacitance values, thereby obtaining the optimal efficiencies for 2:1 SC converters according to Eq. (6).

B. *Analysis of Droop Voltage against Load Transients*

The load transient behavior of a SCVR is determined by the operation of the SC converter, the input/output decoupling capacitance and the closed-loop regulation scheme. To analyze the effect of decoupling capacitance on SCVR output droop, we performed droop simulations as shown in Figure 2. The 17-phase interleaved SC converters are driven by a voltage-controlled oscillator (VCO) that provides a frequency modulation scheme against a load transient. Level shifters, non-overlapping clock generators, and driver stages are also implemented for proper clock distribution.

The droop voltage simulation results for a 102mA to 1.02A load step in 10ns , with 1nF-13nF of input and output decoupling capacitors are shown in Figure 3. As can be seen, for the same amount of capacitance (and thus area), the effect of input decoupling capacitance on the output droop is considerably weaker than that of the output decoupling capacitance. To that end, input decoupling capacitance is not considered in this work.

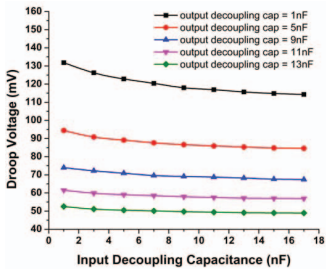

Figure 3. SCVR output droop voltage against fast load transients with input and output decoupling capacitances in 65nm.

During the steady state of the SCVR, when the current, switching frequency, switch width and other modulated parameters are kept constant, the load current is mainly provided by the flying capacitor. The minimum output voltage value in continuous cycles of the switching clocks [7] is set by:

$$V_o(t) = \frac{V_i}{2} - \frac{i_{SC}(t)}{4 C_{fly} \cdot f_{sw}} \tag{8}$$

Upon an abrupt load transient, the portion of current supplied by the output decoupling capacitor first instantaneously increases and then decreases as the SC converter provides more output current with a specific regulation scheme. The current provided by the decoupling capacitor $i_{cp}(t)$ is set by:

$$i_{cp}(t) = C_{cp} \cdot \frac{d\,V_o(t)}{dt}\,, \tag{9}$$

where C_{cp} is the decoupling capacitance. At the SCVR output, according to Kirchhoff's current law (KCL), the three current values have the following relationship during the load response:

$$N \cdot i_{SC}(t) + i_{cp}(t) = N \cdot i_L(t)\,, \tag{10}$$

where N is the number of interleaved phases in the SCVR, $i_{SC}(t)$ is the single-phase SC converter output current and $i_L(t)$ is the load current.

In realistic design cases, the SC input voltage Vi, flying capacitance C_{fly} , switching frequency f_{sw} , decoupling capacitance C_{cp}, the number of interleaved phases N and load current step $i_L(t)$ are already known. Then, a system of

differential equations, Eqs. (8)-(10), is formed that has $V_o(t)$, $i_{SC}(t)$ and $i_{cp}(t)$ as unknown variables. Assuming that the load current increases from I_0 to I_1 in transient time of Δt, starting at time 0, the time-domain single-phase load current is:

$$I_L(t) = \frac{I_1 - I_0}{\Delta t} \cdot t + I_0 \tag{11}$$

By solving the differential equation system above, the output voltage equation can be derived as follows:

$$V_o(t) = \frac{C_{cp}\,(I_1 - I_0)}{N \cdot \Delta t \cdot {K_0}^2} \cdot (1 - e^{-\frac{K_0}{C_{cp}} t}) - \frac{I_1 - I_0}{K_0 \cdot \Delta t} \cdot t + \frac{V_i}{2} - \frac{I_0}{K_0}, \tag{12}$$

As the output voltage before the load response is given by Eq. (8), the droop voltage of the SCVR at time $\Delta t/2$ is set by:

$$V_{droop\_sc} = -\frac{C_{cp}\,(I_1 - I_0)}{N \cdot \Delta t \cdot {K_0}^2} \cdot (1 - e^{-\frac{K_0}{C_{cp}} t}) + \frac{I_1 - I_0}{K_0 \cdot \Delta t} \cdot t \tag{13}$$

The first term of in Eq. (13) represents the droop voltage contributed from the output decoupling capacitance, and the second term represents the output voltage decrease caused by the operation of the SC converter.

In realistic conditions, the SCVR input voltage Vi is not constant due to $L \cdot di/dt$ voltage drop caused by the package inductor. For a load step from I_{SC0} to I_{SC1} in Δt, the additional amount of droop caused by the package inductor is set by:

$$V_{droop\_ind} = \frac{I_{sc1} - I_{sc0}}{2M} \cdot \frac{L_{pck}}{\Delta t} \cdot e^{-\frac{C_{cp}}{C_0}}, \tag{14}$$

where M is the number of I/O pins and L_{pck} is the inductance of each pin. C_0 is a fitting parameter obtained from simulation. Overall, the droop voltage of the on-chip SCVR is modeled as:

$$V_{droop} = -\frac{C_{cp}\,(I_1 - I_0)}{N \cdot \Delta t \cdot {K_0}^2} \cdot (1 - e^{-\frac{K_0}{C_{cp}} t}) + \frac{I_1 - I_0}{\Delta t \cdot K_0} \cdot t + \frac{I_{sc1} - I_{sc0}}{2M} \cdot \frac{L_{pck}}{\Delta t} \cdot e^{-\frac{C_{cp}}{C_0}} \tag{15}$$

C. Proposed Figure-of-Merit for System-Level Power Optimization

In order to evaluate the proposed optimization for an area-constrained SCVR design, we hereby propose a figure-of-merit (FOM) for the system-level power, as shown below:

$$FOM = \frac{P_{out}}{P_{out} + P_{loss} + V_{droop} \cdot I_{avg}}, \tag{16}$$

where P_{out} represents the output power at a target load current and P_{loss} is the power conversion loss. I_{avg} is the average current of the processor workload. Without losing generality, in this work, we assume I_{avg} to be the average value of the maximum load current I_{max} and the minimum load current of $0.1 \cdot I_{max}$, which becomes $0.55 \cdot I_{max}$. The minimum load current is set as 1/10 of the maximum load considering the leakage current of processors, and also serves as the initial current for the worst-case load step response.

The SCVR compares its output voltage to a target reference V_{ref} and continuously modulates the converter to keep the output voltage as close as possible to V_{ref}. When abrupt load transients occur, the SCVR can experience worst-case droop V_{droop}, which will bring down the output voltage to $V_{ref} - V_{droop}$. Since it is very difficult to precisely predict when the load transients will occur, to avoid any timing failure even when the droop occurs, $V_{ref} - V_{droop}$ needs to be the minimum supply voltage V_{min} for digital load circuits. This means that, in conditions without abrupt load transients, V_{ref} needs to be positioned at $V_{min} + V_{droop}$ to prevent any timing failure considering potential droop. To that end, V_{droop} becomes the supply voltage margin of the digital loads, and $V_{droop} \cdot I_{avg}$ represents the additional output power that needs to be provided to the load circuits considering that output droop can occur.

Assuming that a fixed die area is allocated to the total area of flying capacitors and decoupling capacitors, the area ratio between the two capacitors that results in the highest FOM can be obtained, which represents a system-level power-optimal SCVR design point. The FOM can be modeled by combining the efficiency model and droop voltage model from Section II:

$$FOM_{cal} = \left(\frac{1}{\eta_{opt}} + \frac{0.55 V_{droop}}{I_{max}}\right)^{-1} \tag{17}$$

III. EXPERIMENTAL RESULTS

In this section, we present simulation results in 65nm and 32nm CMOS and the comparison with model predictions. The flying capacitors and the decoupling capacitors are implemented with MIM capacitors in 65nm and with DT capacitors in 32nm.

A. Efficiency Experiments

To validate the proposed efficiency models, SCVR designs were implemented (Figure 2) in 65nm and 32nm CMOS. For each flying capacitance value, switching frequency and width are swept as design variables to obtain the optimal efficiency for different output currents. Then, this is iterated for a number of different flying capacitance values to obtain the optimal efficiencies. The comparisons of model calculation and simulation in 65nm and 32nm are shown in Figure 4, which includes multiple load current cases per SC converter phase across a wide flying capacitance range. The results show that the maximum efficiency error of the model is less than 1.4% for a 21× range of flying capacitance in 65nm, and less than 0.4% for a 10× range of flying capacitance in 32nm.

B. Droop Voltage Experiments

To validate the accuracy of the droop voltage models for a wide range of decoupling capacitance, simulations with

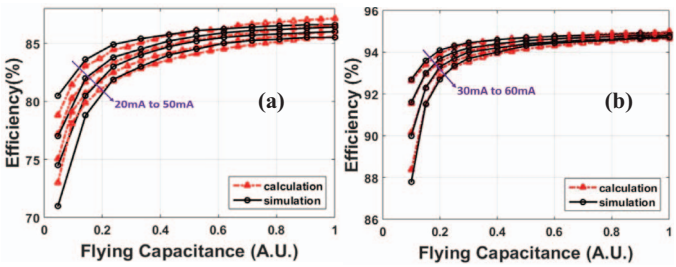

Figure 4. Simulated and calculated optimal efficiencies with different flying capacitances and load currents (per converter phase) in (a) 65nm and (b) 32nm.

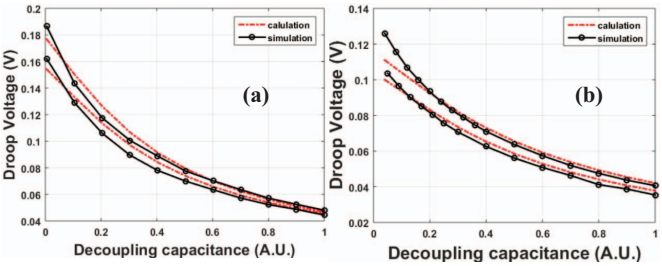

Figure 5. Simulated and calculated droop voltage for 51-510mA, 10ns load step in (a) 65nm and (b) 32nm for a 21× range of decoupling

regulation circuits are performed in both 65nm and 32nm CMOS. In the simulation setup (Figure 2), an output current source changes the load current from 51mA to 510mA in 10ns and a decoupling capacitance is set as a design variable. The output voltage regulation is implemented with a step increase in the control voltage of the VCO (left part of Figure 2) to provide an immediate increase of switching frequency so that the output voltage decrease is minimized. By sweeping the output decoupling capacitance value, different droop voltage values are obtained from simulations.

Figure 5 shows the comparison of model calculation and simulation in 65nm and 32nm CMOS, where the proposed model achieved good accuracy. In 65nm, the maximum and average prediction droop errors for decoupling capacitance up to 21× range is 8.4mV (7.6%) and 3.7mV (3.5%), respectively. In 32nm, the maximum and average droop errors are 15mV (11.9%) and 4.5mV (4.3%), respectively.

C. Flying/Decoupling Capacitance Optimization with FOM

Since the proposed figure-of-merit characterizes the performance of the SCVR, the FOM can be obtained through modeling calculation and simulations in 65nm and 32nm CMOS, by varying the ratio between flying and decoupling capacitance with an area constraint.

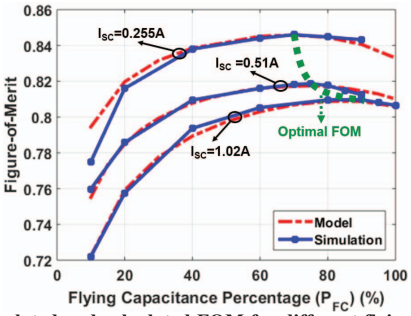

Figure 6. Simulated and calculated FOM for different flying capacitance percentage in 65nm CMOS at 0.255A, 0.51A and 1.02A SC currents.

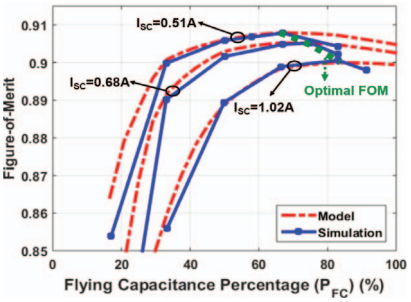

Figure 7. Simulated and calculated FOM for different flying capacitance percentage in 32nm CMOS with 0.51A, 0.68, and 1.02A SC currents.

In the 65nm design, the total on-chip MIM capacitors occupy a fixed die area of 1.7mm^2. The total flying capacitance is divided by 17 for a 17-phase interleaved SC converter, and the rest of the area is occupied by the decoupling capacitance. In the 32nm design, the total area of the deep-trench capacitors is 0.32mm^2. For different output current values of the SCVR, the optimal efficiencies with different flying capacitance percentage (P_{FC}) values are obtained by sweeping the frequency and width of the SC converter, and the droop voltages are obtained by running transient simulations with load step from 0.1× to 1× current. The FOM for each different flying capacitance percentage is determined with Eq. (16) based on the simulation results, at different load current cases. The modeled FOM is calculated with Eq. (17) according to the efficiency and droop voltage formulas. The comparison of simulated and calculated FOM versus flying capacitance percentage for three different load current cases in 65nm and 32nm CMOS are shown in Figure 6 and Figure 7, respectively. Compared to the simulation results (where the smallest P_{FC} step is 5%), the worst-case modeling error of P_{FC} is 5%.

IV. CONCLUSION

In this paper, we present an optimization methodology for flying and output decoupling capacitance of SCVRs under area constraints. The power efficiency and droop voltage against load transients are modeled with respect to flying capacitance and decoupling capacitance. Based on these models, we proposed a figure-of-merit that represents system-level power efficiency, capturing both efficiency and droop. The proposed FOM enabled optimization of the flying and decoupling capacitance values for area-constrained on-chip SCVRs. The models are validated with SCVR circuit simulations in 65nm and 32nm CMOS, showing good prediction accuracy.

REFERENCES

[1] M. Lee, et al., "0.76W/mm^2 on-chip fully-integrated buck converter with negatively-coupled, stacked-LC filter in 65nm CMOS," *ECCE*, 2014.

[2] M. Saint-Laurent, et al., "A 28nm DSP powered by an on-chip LDO for high-performance and energy-efficient mobile applications," *IEEE J. of Solid-State Circuits*, 2015.

[3] T. M. Andersen, et al., "4.7A sub-ns response on-chip switched-capacitor DC-DC voltage regulator delivering 3.7W/mm2 at 90% efficiency using deep-trench capacitors in 32nm SOI CMOS," *IEEE ISSCC*, 2014.

[4] X. Mi, et al., "Fully-integrated SC voltage regulator with on-chip current-sensing and workload optimization in 32nm SOI CMOS," *IEEE/ACM ISLPED*, 2015.

[5] W. Jung, et al., "A rational-conversion-ratio switched-capacitor DC-DC converter using negative-output feedback," *IEEE ISSCC*, 2016.

[6] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor DC–DC converters," *IEEE Trans. on Power Elec.*, 2008.

[7] H.-P. Le, et al., "Design techniques for fully integrated switched-capacitor DC-DC converters," *IEEE J. of Solid-State Circuits*, 2011.

[8] V. Sathe and J. Seo, "Analysis and optimization of CMOS switched-capacitor converters," *IEEE/ACM ISLPED*, 2015.

[9] B. Wu, et al., "Analysis of high-power switched-capacitor converter regulation based on charge-balance transient-calculation method," *IEEE Trans. on Power Elec.*, 2016.

[10] L. G. Salem, et al., "A footprint-constrained efficiency roadmap for on-chip switched-capacitor DC-DC converters," *IEEE ISCAS*, 2015.