Simulation-Based Design Procedure for sub 1 V CMOS Current Reference

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***Abstract*—This paper presents a new compact low supply current reference and a simulation-based design procedure to establish the circuit parameters quickly and efficiently. To verify the proposed design procedure, two sub 1 V example circuits for two different reference current values (80 nA and 800 nA) were designed and simulated using 0.35 μm CMOS technology. The circuits are robust against supply voltage variation without the need for external bandgap. A line sensitivity of approximately 1-2%/V over the supply voltage range from sub 1 V is achieved in both cases. The simulated temperature coefficient (TC) values are 93 ppm/°C and 197 ppm/°C in the temperature range from 0°C to 120°C for the 800 nA and 80 nA references, respectively.**

I. Introduction

The demand to further decrease the power of integral circuits forces the use of lower power supplies. Due to the complexity of the mathematical representation of real CMOS device behavior at the subthreshold, simulation-based procedures for the design of analog circuits such as gm/ID methodology [1] should be used. However, the applicability of gm/ID methodology is limited to the design of different amplifier circuits [2]–[4].

The design of other analog circuits, such as current references, is also driven by formulas that are unsuited for hand calculations. Thus, the approximations should be used; however, they can lead to far from optimal solutions. The optimization process of the circuit draft in electronic design automation (EDA) becomes very time consuming. The simulation-based procedure should provide a near optimal solution for the circuit parameters to minimize the demand for optimization.

Recently, various current reference circuits were proposed. According to the working principles, these circuits can be split into two main groups: first, the references based on the summation of the complement to the absolute temperature (CTAT) and proportional to the absolute temperature (PTAT) currents; second, the references based on the relation of CTAT or PTAT voltage to the CTAT or PTAT resistance. The first class of circuits [5], [6] suffers from design overcomplexity, including the matching of PTAT and CTAT generators and the summing circuit. For the second class of circuits [7]–[10], the design formulas typically are unsuited for hand calculations.

In this paper a new current reference related to the second class of circuits is proposed. The advantages of the proposed circuit are: the possibility of sub 1 V operation; low TC over the wide temperature range from 0 to 120 °C; very low supply sensitivity achieved without the use of external bandgap.

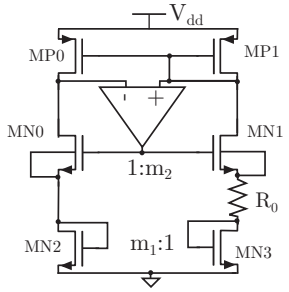

Fig. 1. Proposed current reference.

However, the primary advantage of the proposed circuit over [7]–[10] is a straightforward and simple simulation-based design procedure. To verify the proposed procedure, two reference circuits were designed and simulated in the 0.35 μm CMOS process of Austrian Microsystems (AMS).

The remainder of this paper is organized as follows. In section II, the operating principles of the current reference circuit are explained. Section III describes the proposed simulation-based design procedure. A comparison of the simulation results of two example designs to the state of the art is presented in section IV. Finally, section V concludes the paper.

II. Operating principle

The proposed current reference (Fig. 1) uses the relation of the PTAT voltage to the PTAT resistor:

$$I_{ref} = {V_0(\alpha_V(T-T_0)\pm 1)}/{R_0(\alpha_R(T-T_0)\pm 1)} \qquad (1)$$

The bulk contacts of the MN0 and MN1 transistors are tied to source, which is possible in the considered technology, because transistors can be manufactured in the separate N-tubes. The resistor in the N-well was chosen as the most efficient for area/resistance.

The current mirror MP0:MP1 equalizes the currents through two circuit branches. If the transistors MN0:MN1 are operating in the subthreshold region, the ratio between source voltages V_{s0} and V_{s1} of these transistors can be found from:

$$\begin{cases} I_{ref} = I_0^{MN0} e^{V_g/n\varphi_T} e^{-V_{th}^{MN0}/n\varphi_T}(e^{-V_{s0}/\varphi_T}) \\ I_{ref} = m_2 I_0^{MN0} e^{V_g/n\varphi_T} e^{-V_{th}^{MN1}/n\varphi_T}(e^{-V_{s1}/\varphi_T}), \end{cases} \qquad (2)$$

where $\varphi_T = {k}/{q}T$ is the termal voltage, V_{th} is the threshold voltage and m_2 is the width relation of MN1 to MN0.

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Assuming the subthreshold swing parameter $n \approx 1$, one can write:

$$V_{s1} = V_{s0} + \varphi_T \ln(m_2) + \Delta V_{th}^{MN0,1} \quad (3)$$

The reference current can be found from:

$$I_{ref} R = V_{s1} - V_{gs3}^{MN3}. \quad (4)$$

Substituting expression (3) for the source voltage of MN1 into the reference current equation (4):

$$I_{ref} R = \varphi_T \ln(m_2) + \Delta V_{th}^{MN0,1} + (V_{gs2} - V_{gs3}) \quad (5)$$

Similar to (2) the $V_{gs2} - V_{gs3}$ can be found from (m_1 is the width relation of MN2 to MN3):

$$\begin{cases} I_{ref} = m_1 I_0^{MN3} e^{V_{gs2}/n\varphi_T} e^{-V_{th}^{MN2}/n\varphi_T} \\ I_{ref} = I_0^{MN3} e^{V_{gs3}/n\varphi_T} e^{-V_{th}^{MN3}/n\varphi_T} \end{cases} \quad (6)$$

Thus, the reference current can be expressed as:

$$I_{ref} = \left(\varphi_T \ln(m_2/m_1) + \Delta V_{th}^{MN0,1} + \Delta V_{th}^{MN2,3}\right)/R. \quad (7)$$

Denoting T_0 as the reference temperature (generally 27°C is used), and introducing the notation:

$$V_0 = \varphi_{T_0} \ln(m_2/m_1) + \Delta V_{th}^{MN0,1} + \Delta V_{th}^{MN2,3}, \quad (8)$$

one can write the following expression for the reference current (in form of (1)):

$$I_{ref} = \frac{V_0 \left[\frac{\frac{k}{q}\ln(m_2/m_1)}{V_0}(T - T_0) + 1\right]}{R_0(\alpha_R(T - T_0) + 1)}. \quad (9)$$

Thus, if :

$$k/q \ln(m_2/m_1)/V_0 = \alpha_R, \quad (10)$$

the reference current I_{ref} becomes temperature stable at the certain values of m_2, m_1 and V_0.

Although the V_{th} depends of the temperature as [11] the ΔV_{th} of two MOS transistors depends mostly on their geometry (if the $V_{bs} = 0$), as:

$$\Delta V_{th} \approx k_3 t_{ox} \left(1/W_1 - 1/W_2\right) \Phi_S(T_0), \quad (11)$$

where k_3 is model parameter and $\Phi_S(T_0)$ is the surface potential at reference temperature.

So, it *can* be possible to find the m_1, m_2 values to get the temperature independent current for all resistor values.

III. Simulation-based design procedure

Although the theoretical expression for the reference current was presented in the previous section, it is not suited for the practical design because of complexity of possible expressions for the absolute widths of the transistors and their relations (m_1 and m_2). Because of this, the simulation-based procedure was designed. The required steps can be summarized as follows:

1) The widths of MN3 and MN0 are set to the minimum value, which satisfies two conditions: first, for the chosen I_{ref}, the transistor should operate in subthreshold region. Second, the process influence on the ΔV_{th} should be minimized. To satisfy the second condition the V_{th} should be simulated across the process corners as a function of transistor width W for the given bias current.

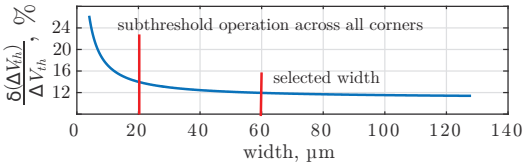

Fig. 2. $\frac{\delta(\Delta V_{th})}{\Delta V_{th}}$ process sensitivity as a function of width

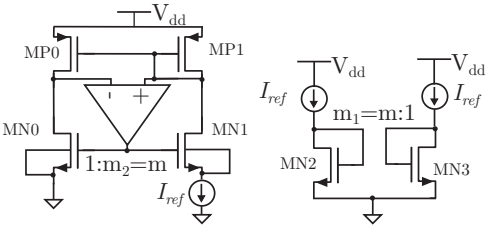

Fig. 3. Simulation setup to determine $(m1, m2)$ values, which will satisfy the zero TC condition (10) at the nominal corner.

Then, the first derivative of the V_{th} should be taken. The first order behavior of the ΔV_{th} is then described as $\Delta V_{th} = \Delta W V'_{th}$, where V'_{th} is the first order derivative of V_{th} at width W. The accuracy is set by the simulation step ΔW. The dependency of ΔV_{th} on the process variation as a function of W can be found from:

$$\frac{\delta(\Delta V_{th})}{\Delta V_{th}} = \frac{\max(V'_{th}) - \min(V'_{th})}{V'^{\text{nominal corner}}_{th}}, \quad (12)$$

where $\max(V'_{th})$ is the V'_{th} for the corner, where it is maximal, and $\min(V'_{th})$ is the V'_{th} for the corner, where it is minimal. An example of such s plot for the bias current 0.8 μA (beginning from $L > 2\mu m$, the value of $\frac{\delta(\Delta V_{th})}{\Delta V_{th}}$ shows no dependency from L in the subthreshold, so the channel length was set to $L = 4\mu m$,) is presented in Fig.2. The widths of MN0 and MN3 are set to 60 μm.

2) Find the range of $(m1, m2)$ values, which will satisfy the zero TC condition (10) at the nominal corner. To do this the circuit in Fig. 1 can be split into two parts, as shown in Fig. 3. Doing so allows us to obtain the $(m1, m2)$ values, which satisfy the zero TC condition (10), separately for transistor pairs (MN0, MN1) and (MN2, MN3). The theoretical possibility to accomplish this split can be seen from expressions (8)-(11) as the zero TC condition (10) has no dependency from the operating point.

The DC simulation is done for the temperature range -40°C...+120°C for different values of $(m1, m2)$. Because of circuit splitting, the $(m1, m2)$ can be set to one variable m. The simulation results are analyzed in Matlab, to obtain the $(m1, m2)$ values, which will satisfy the zero TC condition (Fig.4). As shown in the figure, each value of $m1$ corresponds to only one $m2$ value, which guarantees the equality of temperature coefficients $\alpha_V = \alpha_R$.

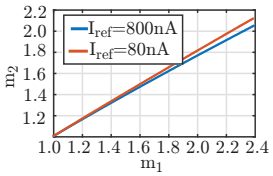

Fig. 4. (m_1, m_2) values, which correspond to the $\alpha_V = \alpha_R = 6.2 \times 10^{-4}$ (TC of the N-well resistor in the 0.35 μ m AMS process).

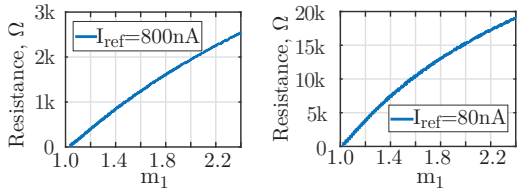

Fig. 5. Resistance values, which correspond to each (m_1, m_2) pair. Two reference currents are considered: $I_{ref} = 800$ nA and $I_{ref} = 80$ nA

3) From the same simulation results, the values of V_0, which correspond to each (m_1, m_2) pair can be found. From these values, the needed R_0 values can be easily found as $R_0 = V_0/I_{ref}$. These values are shown in Fig. 5.

4) Now, with the $(m1, m2)$ set defined one can pick out the minimum (m_1, m_2) values which correspond to the desired TC over mismatch. For the technology used, the desired matching of the parameters for the two transistors is achieved by the width relation of 1.5. Thus, $m_1 = 1.5$ was chosen. In addition, note that the TC of the N-well resistor varies across the temperature range over 10% for resistances lower than ≈1K.

The circuit parameters obtained by these steps for the two reference currents (80 nA and 800 nA) are summarized in the Table I. The total simulation time on the Intel Core i5-4670 3.4 GHz PC was only 11.6 minutes. Cadence Spectre simulator was used. The proposed simulation-based procedure gives near optimum circuit parameter values. Thus, the usually time consuming Cadence optimization process has very good starting point. For example, for the 800 nA reference it finds the optimum parameter values after 101 simulations, or 7.25 minutes on the considered PC configuration. The minimum TC over all process corners is set as the optimization goal. If the starting transistor widths had been shifted for 5 μm the optimization tool would need more than 5000 runs, or 6 hours.

IV. Simulation Results and Comparison to the State of the Art

For simulation the simple differential pair with the current mirror load was used as operational amplifier. All transistors used in the amplifier also operate in subthreshold. The operational amplifier is biased at 2 nA with the temperature stable current delivered from the same reference circuit.

The current variations across process corners for each circuit are shown in Fig.6. The process corners of NMOS, PMOS and N-well resistor were studied. The current value at the temperature $T_0 = 27$°C of the 800 nA reference varies from

TABLE I
Parameters of example circuits obtained by the proposed simulation-based design procedure and Cadence optimization

	80 nA [1]	80 nA[2]	800 nA[1]	800 nA[2]
$(W/L)_{MP0,1}$, $\mu m/\mu m$	32/1	32/1	32/1	32/1
$(W/L)_{MN0}$, $\mu m/\mu m$	60/4	59.7/4	60/4	60.5/4
$(W/L)_{MN1}$, $\mu m/\mu m$	90/4	89.3/4	90/4	90/4
$(W/L)_{MN2}$, $\mu m/\mu m$	86.8/4	85.7/4	85.5/4	84.9/4
$(W/L)_{MN3}$, $\mu m/\mu m$	60/4	59.5/4	60/4	60.1/4
R_0, Ω	8875	8871	1070	1212
I_{ref} †, nA	73	80	877	800
TC†	1300	193	304	48

[1] Values obtained by the proposed simulation-based design procedure.
[2] Optimum values obtained after running Cadence optimization tool.
† At nominal corner.

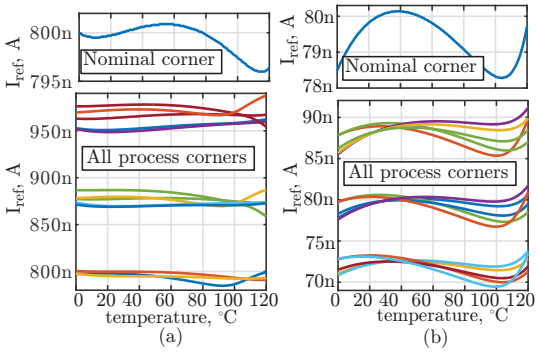

Fig. 6. Simulation Results. (a) 800 nA reference circuit. (b) 80 nA reference circuit.

799 nA up to 970 nA, while TC varies from 16 ppm/°C up to 113 ppm/°C, at the nominal corner TC value is equal to 48 ppm/°C. The value of TC at the nominal corner is not minimal, because the minimum TC across *all* corners was chosen as the optimization goal during the circuit design. For the 80 nA reference current varies from 72 nA up to 89 nA, the TC values are between 193 ppm/°C for the nominal corner and 400 ppm/°C for the worst case corner.

The results of 1000 Monte-Carlo runs for mismatch variation are shown in Fig.7. Both mismatches between current reference circuits transistors and transistors in the operational amplifier are taken into account. The supply voltage sensitivity simulation is provided in Fig.8.

Comparison of the example designs to the state of the art is given in Table II. Because of subthreshold operation of all transistors in the proposed circuit, the current references exhibit the possibility of low voltage operation. Furthermore, the supply variation sensitivity is one of the lowest among published for the current references without an extra bandgap circuit for the supply regulation (which complicates the system and brings additional regulation and calibration issues). For the 120°C temperature range, the TC of the circuits also looks competitive. The average Monte-Carlo simulation value of TC is given in the Table II. For the nominal corner the TCs of the example circuits are 48 ppm/°C and 193 ppm/°C for the the

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE OF THE ART.

	[5]	[6]	[7]	[8]	[9]	[10]	Example Design I	Example Design II
Year	2015	2016	2016	2016	2013	2005	2016	2016
Technology, μm	0.18	0.18	0.18	0.13	0.18	0.35	0.35	0.35
Supply voltage, V	2.4-3.0	0.6-1.8	1.25-1.8	1.2	1.0	2.5	**1.0-3.6**	**0.8-3.6**
I_{ref}, nA	10 000	20	92	27	1000	13 650	800	80
TC, ppm/°C	130	476	176	327	153	28[b]	93	197
Temperature range, °C	-40...+80	-40...+65	-40...+85	-30...+160	-40...+120	-30...+100	0...+120	0...+120
Line Regulation (VC), %/V	0.5[a]	8.3	7.5	-	6.5	4	**0.9**	**1.7**
Area, μm^2	5000	8000	1300	-	9600	4200	14 000	15 000
Verifification	Meas.	Meas.	Meas.	Sim.	Sim.	Sim.	Sim.	Sim.

[a] With extra bandgap voltage reference for the supply regulation
[b] The TC only for nominal corner provided, and not the average Monte-Carlo value as in the proposed designs.

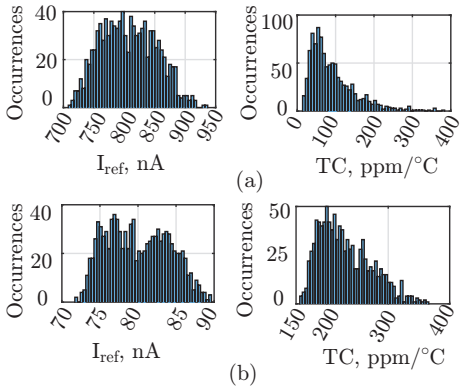

Fig. 7. Monte-Carlo simulation results for mismatch and process variations (1000 runs) of current at 27°C and temperature coefficient of (a) 800 nA reference circuit: Average I_{ref} = 800 nA, $\sigma_{I_{ref}}$ = 90 nA; Average TC = 93 ppm/°C, σ_{TC} = 62 ppm/°C. (b) 80 nA reference circuits: Average I_{ref} = 80 nA, $\sigma_{I_{ref}}$ = 4 nA; Average TC = 197 ppm/°C, σ_{TC} = 50 ppm/°C.

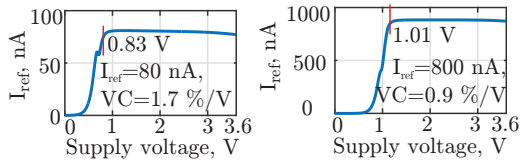

Fig. 8. Supply voltage variation sensitivity of example references.

800 nA and 80 nA circuits, respectively. The area estimation was done by automatic placement tools.

V. CONCLUSION

A new low supply current reference circuit and the simulation-based design procedure were presented. The procedure allows to define the circuit parameters of MOS transistors operating in the subthreshold region quickly and easily with a minimal number of simulations.

Due to verify the proposed design procedure, two example designs of 800 nA and 80 nA current references were developed in the 0.35 μm AMS CMOS process. According to the simulation results the example designs achieve a competitive TC over the temperature range from 0°C to 120°C and supply sensitivity, operating from the supply values up to 0.8-1.0 V.

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