DATE PhD FORUM 2017

The DATE PhD forum is part of the DATE Conference and hosted by the European Design Automation Association (EDAA), the ACM Special Interest Group on Design Automation (SIGDA), and the IEEE Council on Electronic Design Automation (CEDA). It offers the opportunity for PhD students to present their thesis work to a broad audience in the design, automation and test community from academia and industry. During the presentation at the DATE Conference, it helps students to establish contacts. Representatives from industry and academia get a glance of state-of-the-art research in design, automation and test. The review process resulted in the selection of the PhD students listed below. We thank EDAA, ACM SIGDA, CEDA and DATE for making this forum possible.

Cecilia Metra, University of Bologna, IT (Chair, DATE PhD Forum 2017)

PhD Forum Committee

Juergen Alt, Intel Corporation, DE
Davide Bertozzi, University of Ferrara, IT
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Viera Stopjakova, Slovak University of Technology, SK
Sander Stuijk, Eindhoven University of Technology, NL
Daniele Rossi, Westminster University, UK
Miroslav N. Velev, Aries Design Automation, US

Admitted Presentations

1. **Design and Optimization of Resilient Ultra-Low Power Circuits**
   Mohammad Saber Golanbari and Mehdi Tahoori, Karlsruhe Institute of Technology, DE

2. **1024-Channel Single 5W FPGA Towards High-quality Portable 3D Ultrasound Platform**
   Aya Ibrahim, William Simon, Ahmet Caner Yüzügüler, Federico Angiolini, Marcel Arditi, Jean-Philippe Thiran and Giovanni De Micheli, EPFL, CH

3. **ANALOG CIRCUIT DESIGN AUTOMATION AGAINST PROCESS VARIATIONS AND AGING PHENOMENA**
   Engin Afacan, Bogazici University, TR

4. **Design Methodologies and Tools for Vertically Integrated Circuits**
   Harry Kalargaris, University of Manchester, GB

5. **Evolutionary Design of Approximate Components for Deep Learning on a Chip**
   Vojtech Mrazek, Brno University of Technology, CZ

6. **System-level functional and extra-functional characterization of SoCs through assertion mining**
   Alessandro Danese, University of Verona, IT

7. **Reliability Analysis and Dependable Execution Techniques for Processors in Nano-Scale Technologies**
   Ali Azarpeyvand, University of Zanjan, IR

8. **Enabling Caches in Probabilistic Timing Analysis**
   Leonidas Kosmidis, Barcelona Supercomputing Center and Universitat Politècnica de Catalunya, ES

9. **Digital Processors with Alternative Number Systems Selected by Code Generation Mechanism**
   Saba Amanollahi and Ghassem Jaberipur, Shahid Beheshti University, IR

10. **NOMeS: Near-Optimal Metaheuristic Scheduling for MPSoCs**
    Amin Majd, University of Turku, FI

11. **Probabilistically Time-Analyzable Complex Processors in Hard Real-Time systems**
    Mladen Slijepcevic, Barcelona Supercomputing Center and Universitat Politecnica de Catalunya, ES; Carles Hernandez, Barcelona Supercomputing Center, ES; Jaume Abella, Barcelona Supercomputing Center (BSC-CNS), ES; and Francisco Cazorla, Barcelona Supercomputing Center and IIIA-CSIC, ES

12. **Analyzing the Impact of Radiation-induced Failures in All Programmable System-on-Chip Devices**
    Lucas Antunes Tambara and Fernanda Kastensmidt, Universidade Federal do Rio Grande do Sul (UFRGS), BR

13. **Programming Models and Tools for Heterogeneous Many-Core Platforms**
    Alessandro Capotondi, University of Bologna, IT

14. **Logic Synthesis for Majority based In-Memory Computing**
    Saeideh Shirinzadeh, University of Bremen, DE

15. **Analysis, Design, and Optimization of Embedded Control Systems**
    Amir Aminifar, Swiss Federal Institute of Technology in Lausanne (EPFL), CH

16. **Making the Case for Space-Division Multiplexing of Programmable Many-Core Accelerators**
    Marco Balboni, University of Ferrara, IT

17. **Towards Computer-Aided Design of Quantum Logic**
    Philipp Niemann, University of Bremen, DE

18. **Towards HW Platform for Real-Time Systems**
    Lukas Kohutka and Viera Stopjakova, Slovak University of Technology in Bratislava, SK

19. **High-level Modelling of OIN-based Systems with the Provision of a Low Latency Controller**
    Felipe Magalhaes, Ecole Polytechnique de Montreal, CA; Fabiano Hessel, PUCRS, BR; Odile Liboiron Ladouceur, McGill University, CA; Gabriela Nicolescu, Ecole Polytechnique de Montreal, CA

20. **Highly configurable place and route for analog and mixed-signal circuits**
    Eric Lao, Pierre and Marie Curie University (UPMC), FR

21. **Optimization Techniques for Parallel Programming of Embedded Many-core Computing Platforms**
    Giuseppe Tagliavini, University of Bologna, IT

22. **Analyzing and Supporting the Reliability Decision-making Process in Computing Systems with a Reliability Evaluation Framework**
    Maha Kooli, LIRMM-CNRS, FR; Giorgio Di Natale, LIRMM, FR

23. **Techniques for scenario prediction and switching in system scenario based designs**
    Yahya Hussain Yassin and Per Gunnar Kjeldsberg, Norwegian University of Science and Technology (NTNU), NO; Francky Catthoor, IMEC, BE

24. **Improving Processor Efficiency Through Phase Change Based Cooling**
    Fulya Kaplan, Boston University, US

25. **P2NoC: Power- and Performance-Aware Network-on-Chip Architecture for Multi-core Systems**
    Hemanta Kumar Mondal, IIIT Delhi, IN

26. **Ph.D Thesis Title: Bipolar Resistive Switching of Bi-Layered Pt/Ta2O5/TaOx/Pt RRAM-Physics-based Modelling, Circuit Design and Testing**
Firas Hatem, T. Nandha Kumar and Haider Almurib, The University of Nottingham Malaysia Campus, MY

27. **Edge Computing in Internet of Things (IoT)**
Farzad Samie and Lars Bauer, Karlsruhe Institute of Technology, DE; Joerg Henkel, KIT, DE

28. **A Low Power Heterogeneous SoC for CNN-Based Vision**
Francesco Conti, ETH Zurich & University of Bologna, CH

29. **Cross-Layer Dependability for Runtime Reconfigurable Architectures**
Hongyan Zhang and Lars Bauer, Karlsruhe Institute of Technology, DE; Joerg Henkel, KIT, DE

30. **Designing the Bateryless IoT**
Andres Gomez, ETH Zurich, CH; Luca Benini, ETH Zurich, University of Bologna, IT; Lothar Thiele, ETH Zurich, CH